FRONT-END ELECTRONICS FOR WFCTA

TIME MEASUREMENT & DAQ SYSTEM

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Outline

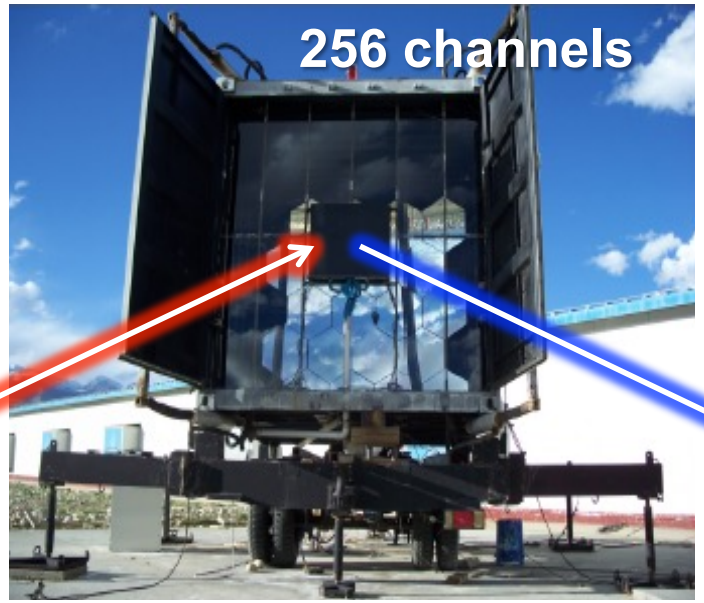
- FEE for WFCTA
- TDC calibration method for PARISROC 2
- New DAQ system based on user-defined protocols
- Conclusions

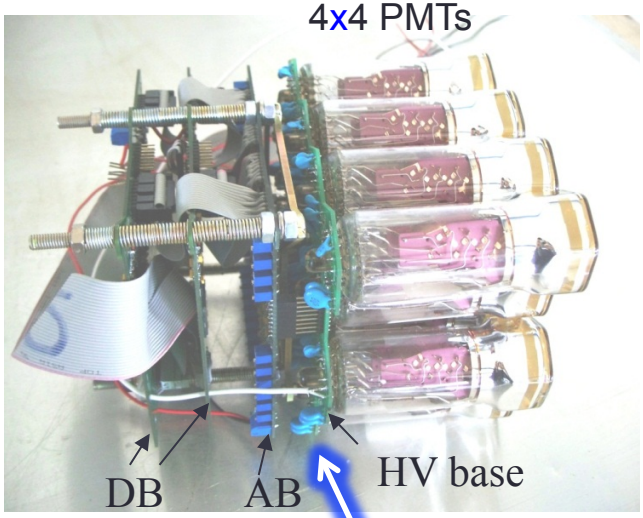
Electronics for WFCTA

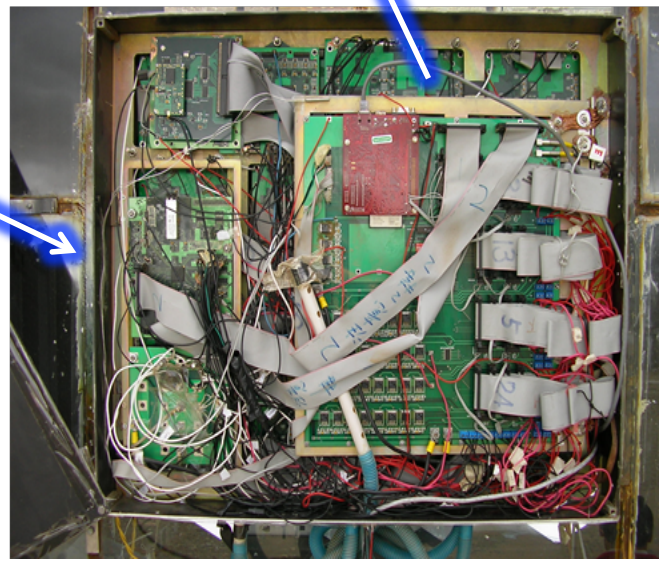
WFCTA prototype
- Classical FADC-based electronics
- Complex
- High power consumption

ASIC solution
- Compact design
- Low power cons.
- High stability
- High reliability
- Easy to maintain

We focused on WFCTA at first.







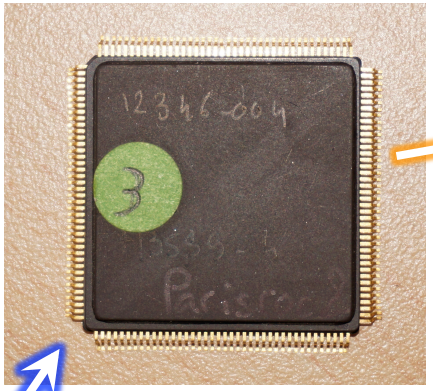
Prototypes in YBJ, Tibet

The ASICs can be used to simplify the electronics of LHAASO.

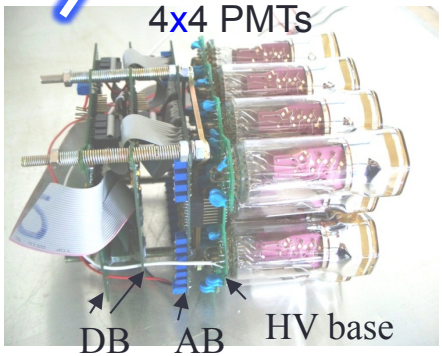
Simplified block diagram

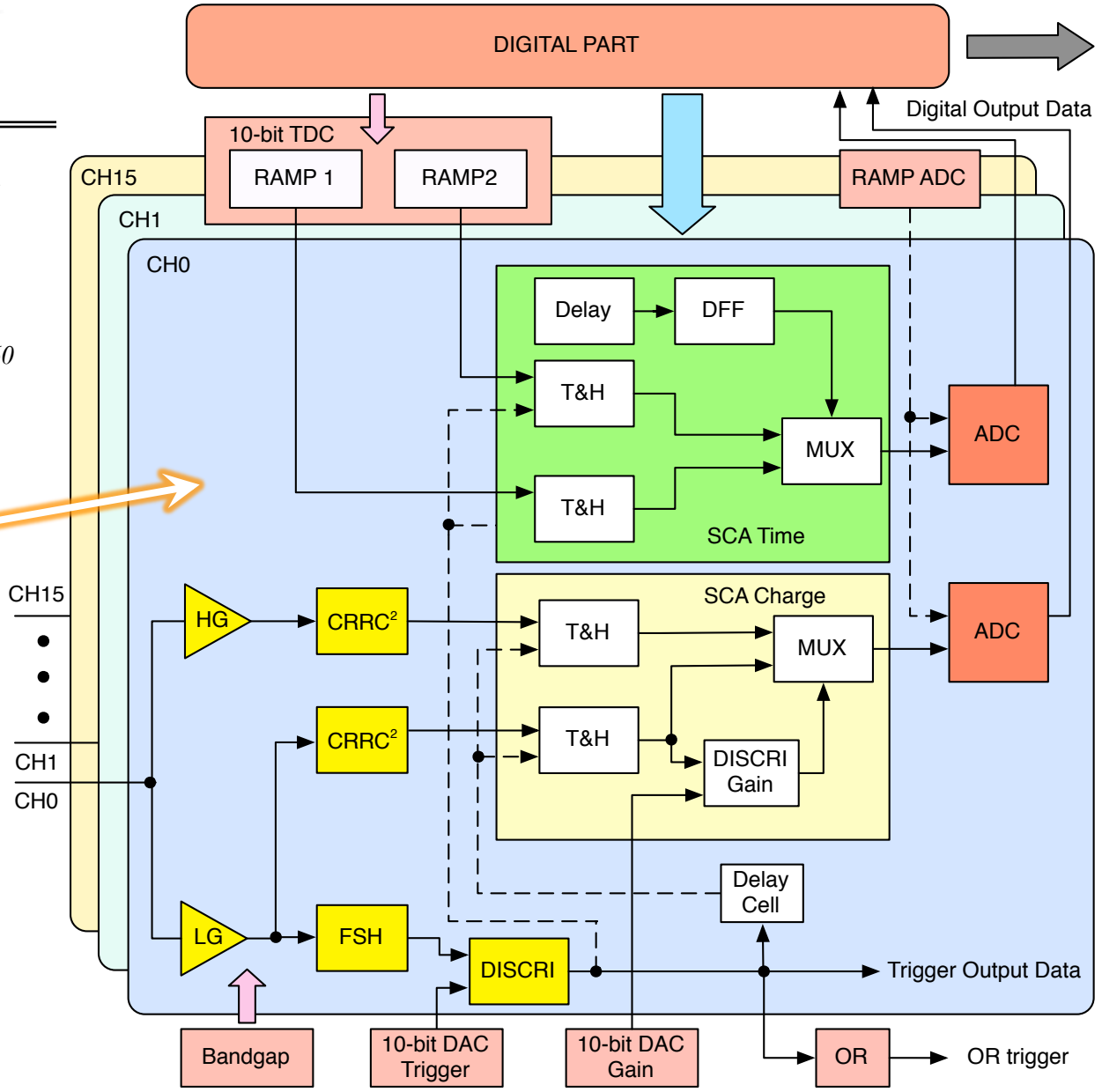
PARISROC 2

Property	Specification
Technology	*AMS 0.35µm SiGe*
Die dimensions	*5.034 mm × 3.42 mm*
Area	*17.21 mm²*
Channels	*16*
Power Supply	*3.3 V*
Power Consumption	*15 mW/channel*
Package	*CQFP-160/TQFP-160*

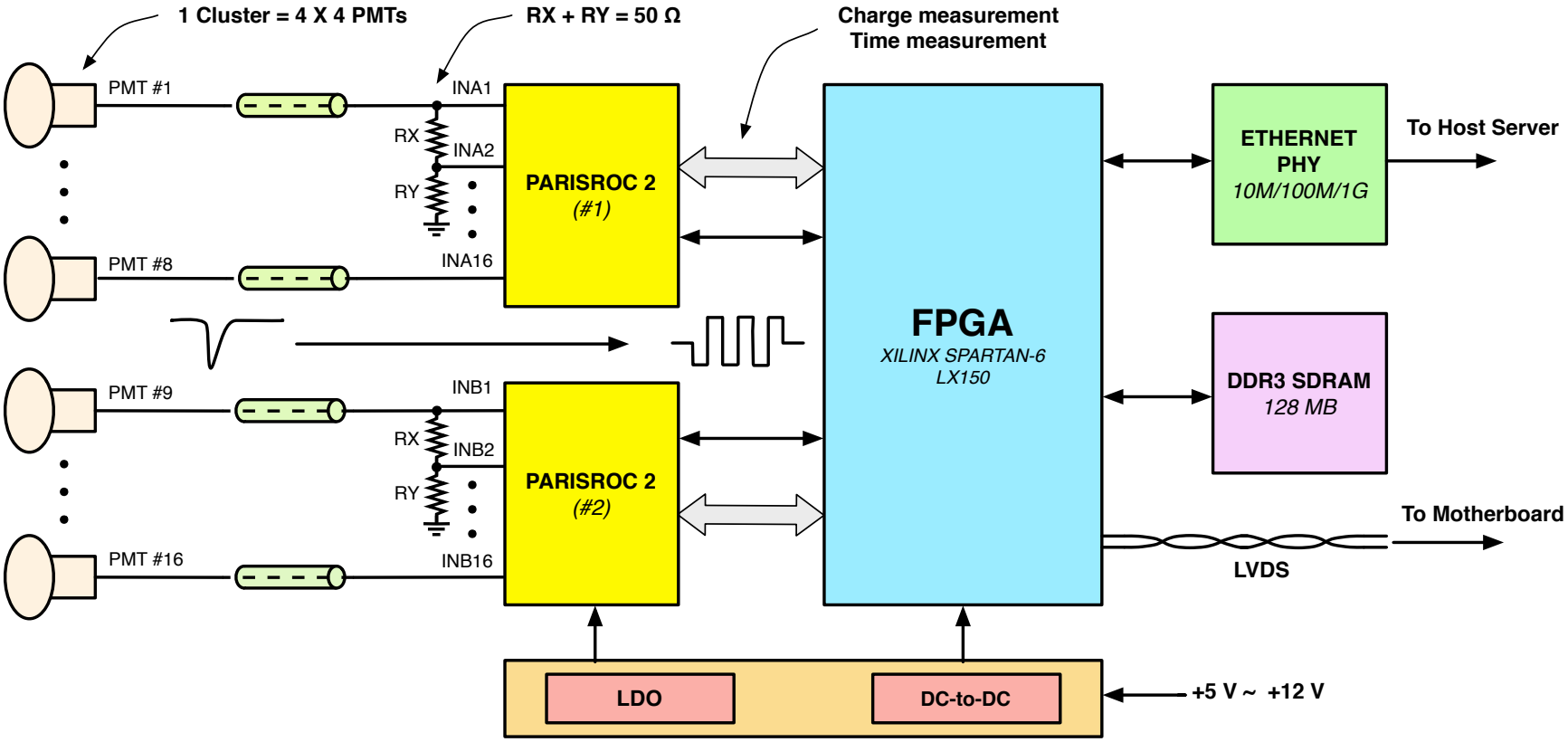


Die: 5 mm X 3.4 mm





System block of the new FEE



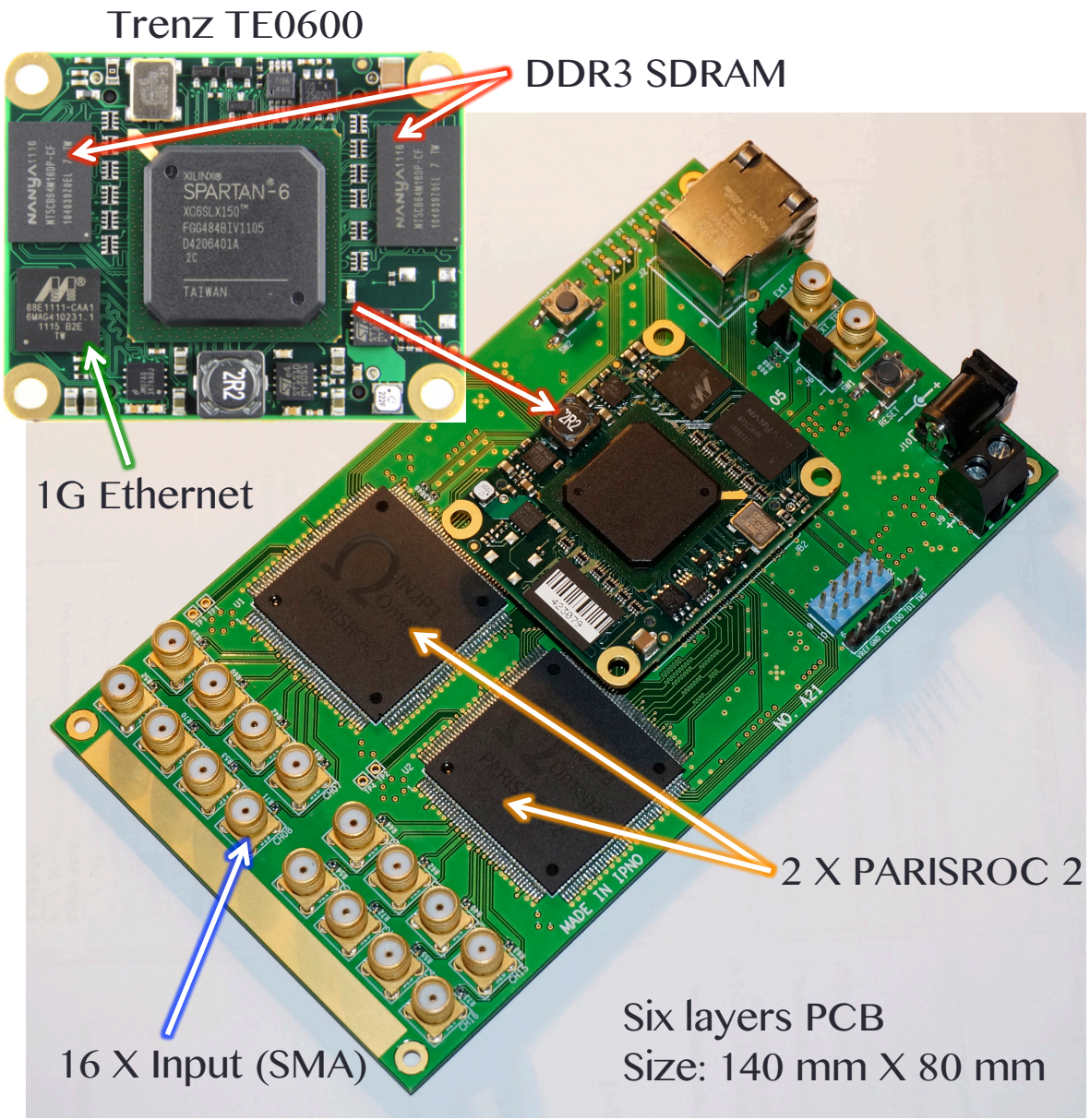
- Two PARISROC 2 chips with 2 groups of 16 inputs
- Voltage dividers at input to extend the dynamic range and keep nonlinearity low
- New powerful FPGA (Xilinx Spartan-6 LX150) as the central controller
- Multiple transferring protocols, such as 1G Ethernet, LVDS
- Power supply: +5 V to +12 V
- Can be easily adapted to any other experiment with similar requirements

Y.T. Chen et al., Front-end electronics based on an autonomous, trigger-less ASIC for LHAASO, 33rd ICRC, Rio de Janeiro, 2013

Picture of the FEE

New FEE

- 16 X SMA inputs
- 2 X PARISROC 2
- Ext. trigger supported
- Mezzanine board
  - Trenz TE0600-01
  - Spartan-6 LX150
  - 50 mm × 40 mm
  - Ethernet embedded
  - DDR3 SDRAM embedded
- Power: +5 V to +12 V



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- FEE for WFCTA
- TDC calibration method for PARISROC 2
- New DAQ system based on user-defined protocols
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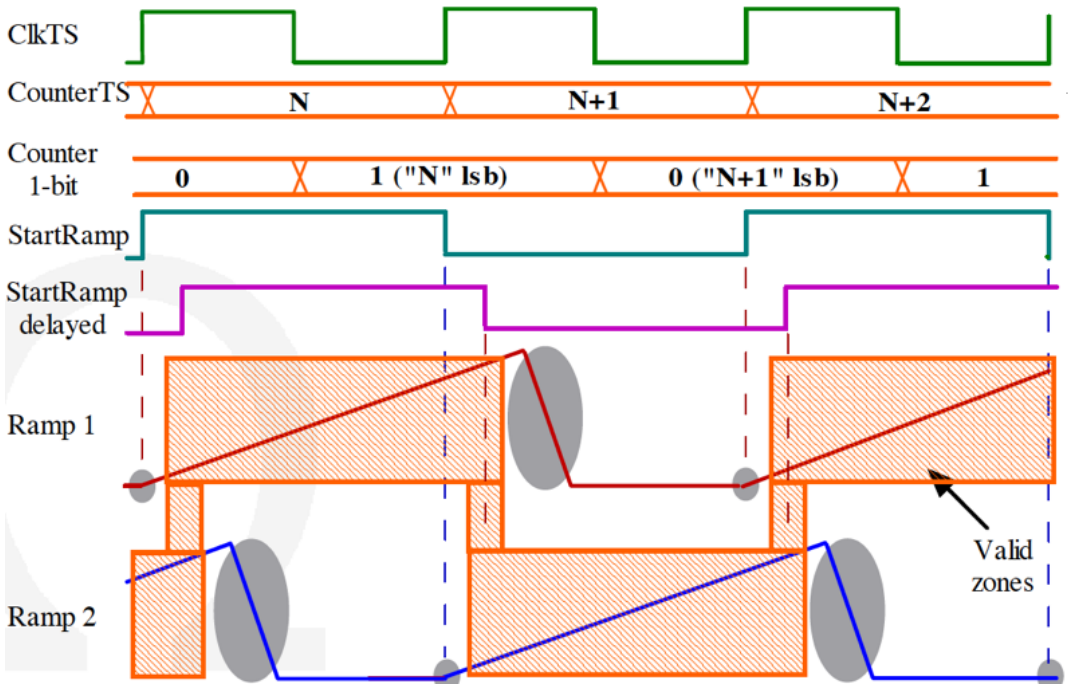
PARISROC 2: Time measurement

Absolute time = Coarse time + Fine time

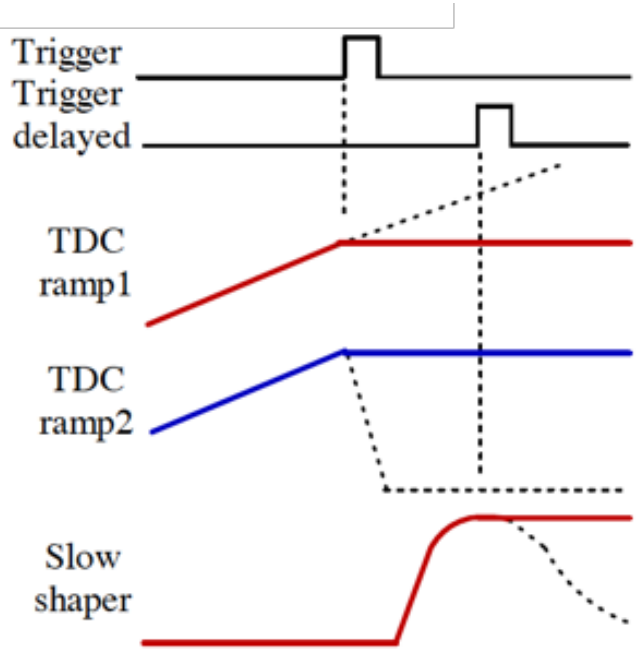
Coarse time:

- ClkTS: 10 MHz
- 24-bit gray code @ rising edge
- 1-bit @ falling edge

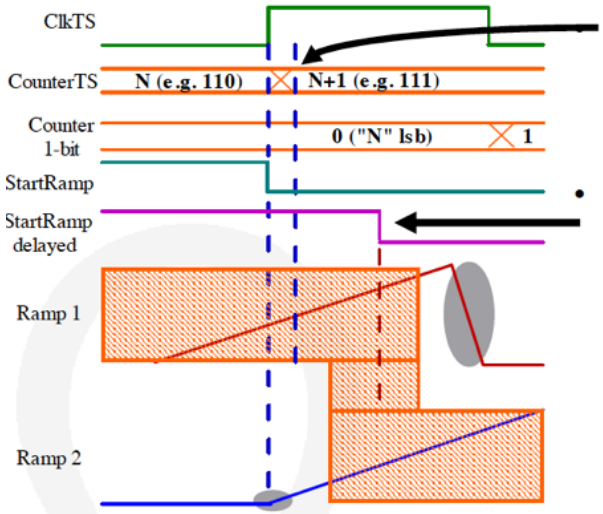


Fine time:

- ADC-type of TDC
- 2 ramps + 2 capacitors
- Ramp: 100 ns
- Ramp overlap: 40 ns
- StartRamp delayed: 20 ns
- Time tagging: < 1 ns



PARISROC 2: How to recover real time



For trigger synchronous with counter ➔
Data stored = (N or N+1), Cpt1Bit and Ttdc

- For trigger synchronous with StartDelayed ➔
  Data stored = N+1, Cpt1Bit and (TtdcRamp1 or TtdcRamp2)

- Recover real time ➔

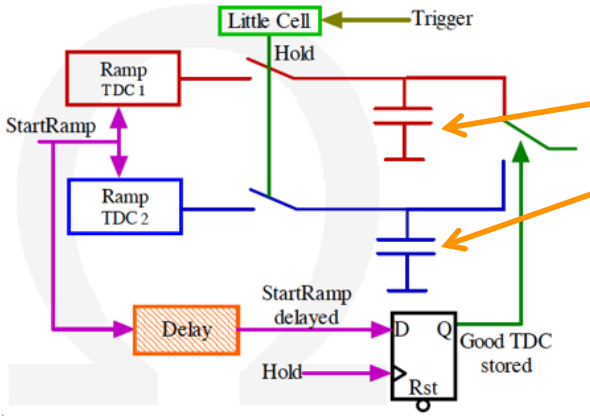
```
If (Ttdc > 90 ns) then
  If LSB(BIN(CptTS)) = (Cpt1Bit) then
        Time = CptTS + Ttdc
  else
        Time = (CptTS-1) +Ttdc
else
  Time = CptTS + Ttdc
```

The key point is to recover the "Ttdc" unit.

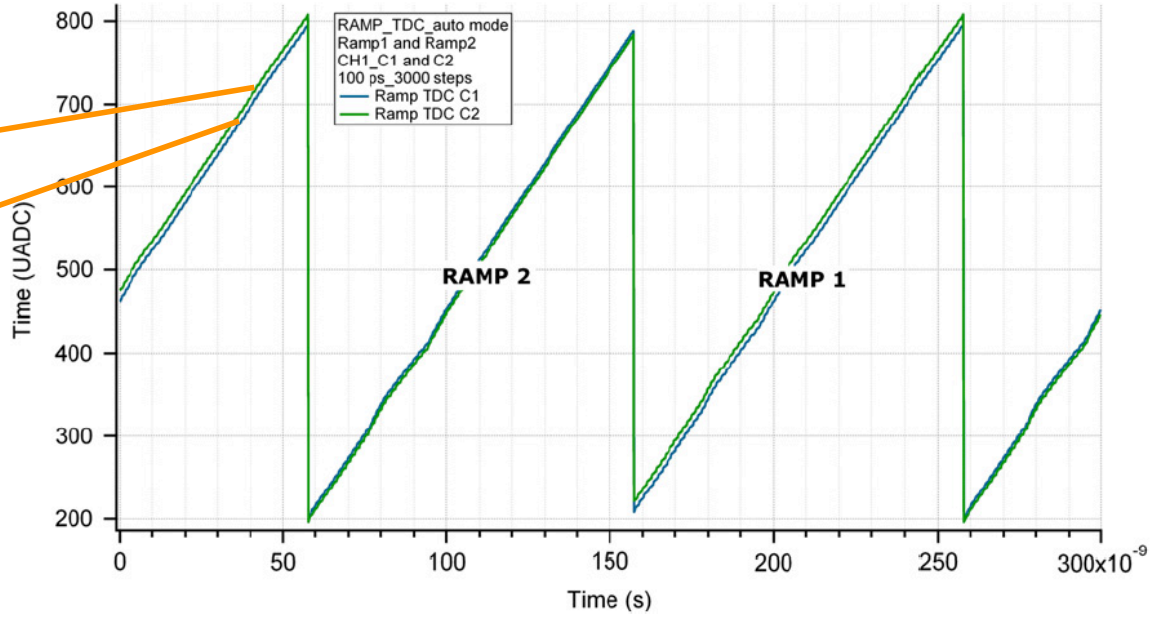
- Ramp is fixed to 100 ns
- Find out the output range

Typical way:

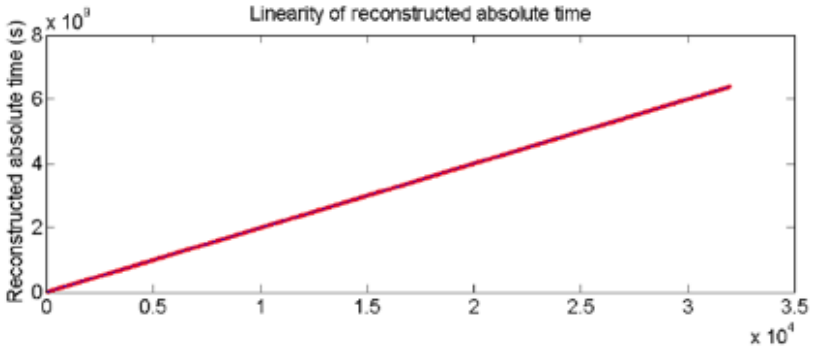
- Injecting a periodical pulse signal into a certain channel.
- The signal is synchronized to the rising edge of the "StartRamp".

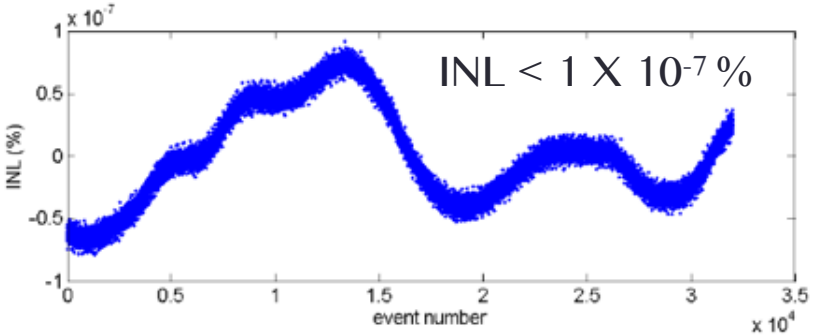


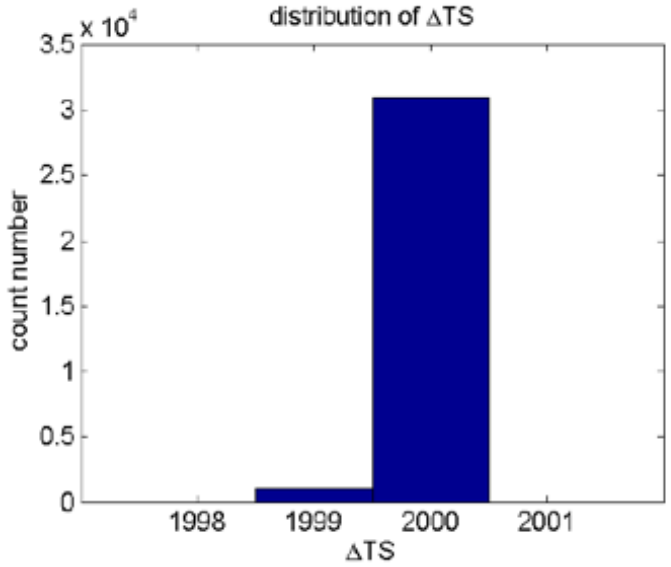
2 Ramps + 2 Capacitors



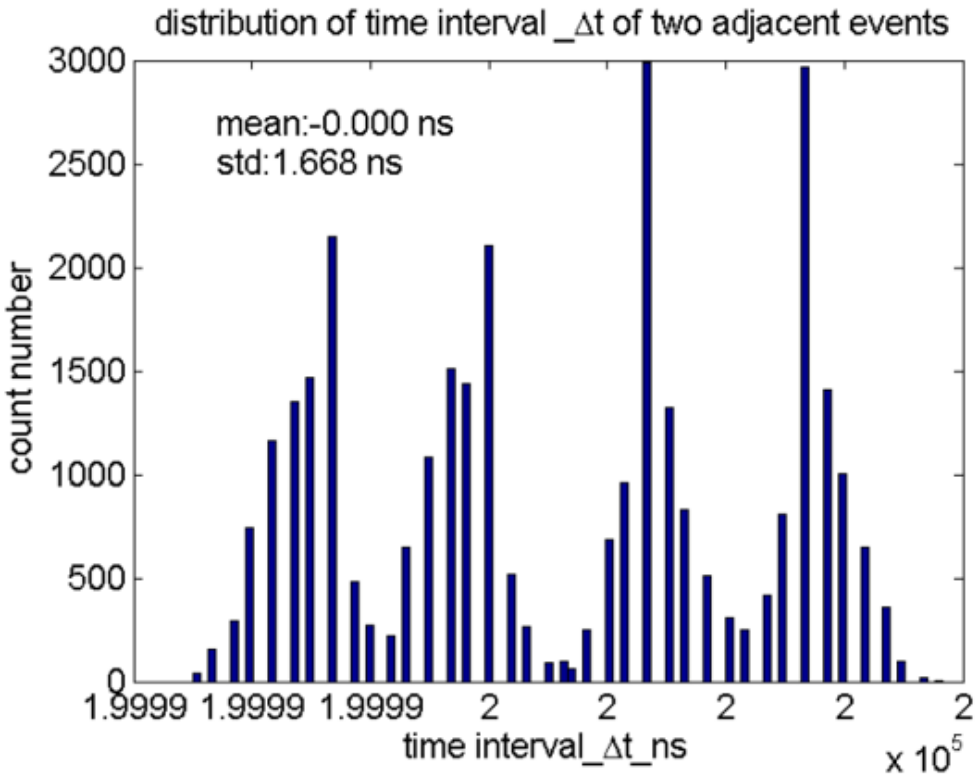
Recovered time without calibration







2 ramps + 2 capacitors
4 groups of outputs



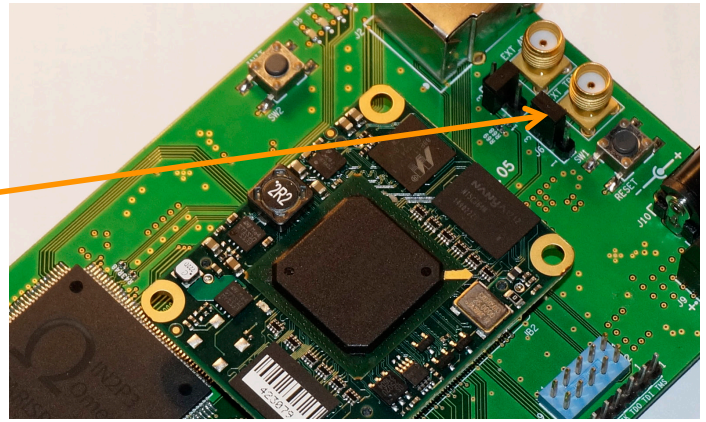
Frequency: 5 kHz; Interval: ~ 200 μs

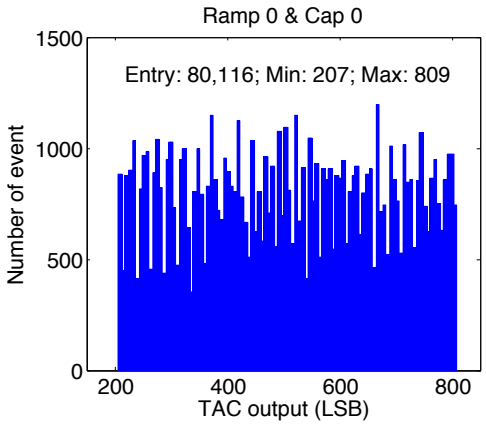
H.Y. Zhang, LHAASO-WFCTA-TECH-FR-IPNOLAL-20141211-02C, 2014.12

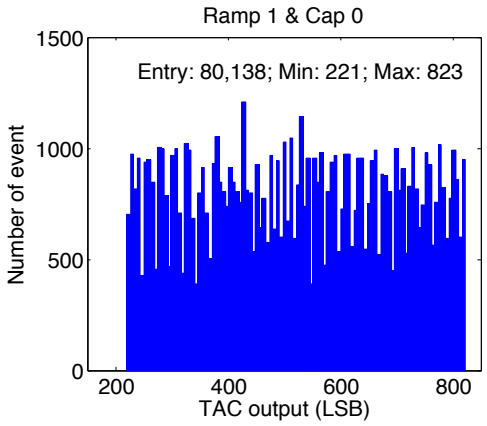
New calibration method

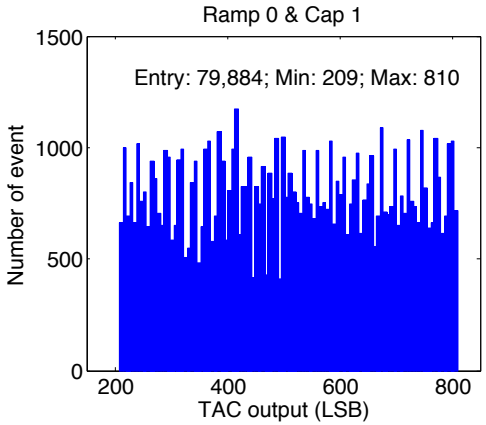
A calibration method for mass production

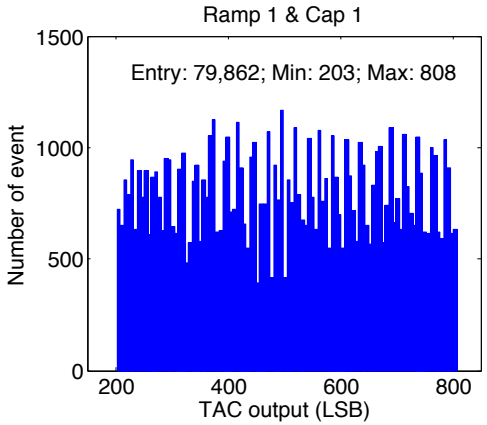
External trigger port
- FPGA
- Signal generator











Calibrate Range difference

Combination		Range (LSB)	TU_{TAC} (ps)
Ramp 0	Capacitor 0	602	166.113
	Capacitor 1	601	166.389
Ramp 1	Capacitor 0	602	166.113
	Capacitor 1	605	165.289

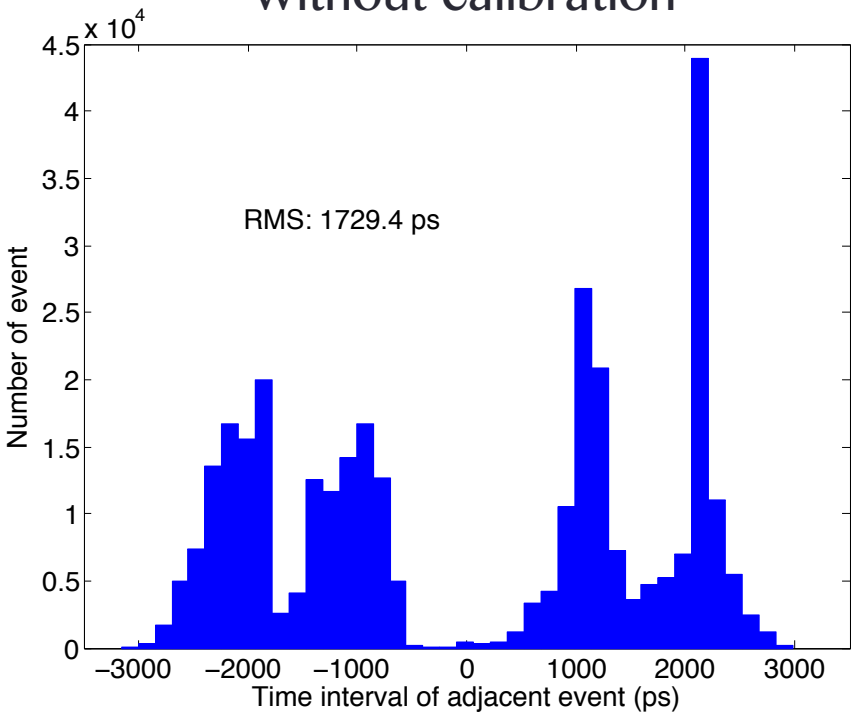
Calibrate Cap. difference

Combination		Mean (LSB)	Coefficient (LSB)
Ramp 0	Capacitor 0	509	0
	Capacitor 1	522	-13
Ramp 1	Capacitor 0	511	-2
	Capacitor 1	504	+5

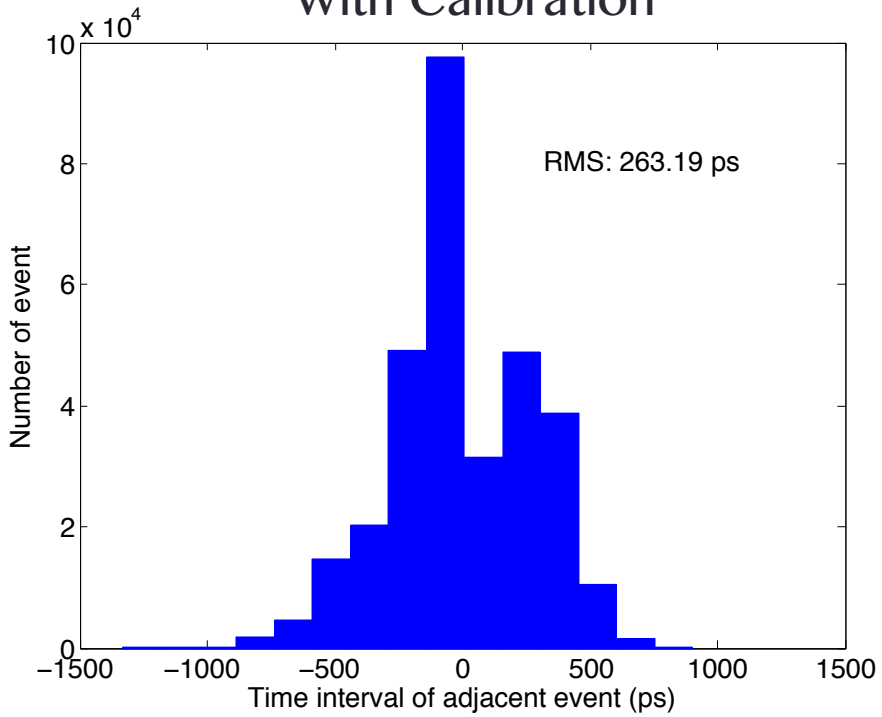
Recovered results with & without calibration

Best: ~ 263 ps; Worst: ~ 460 ps

Without calibration



With Calibration



(±450 ps) [S. Conforti Di Lorenzo et al., 2012]

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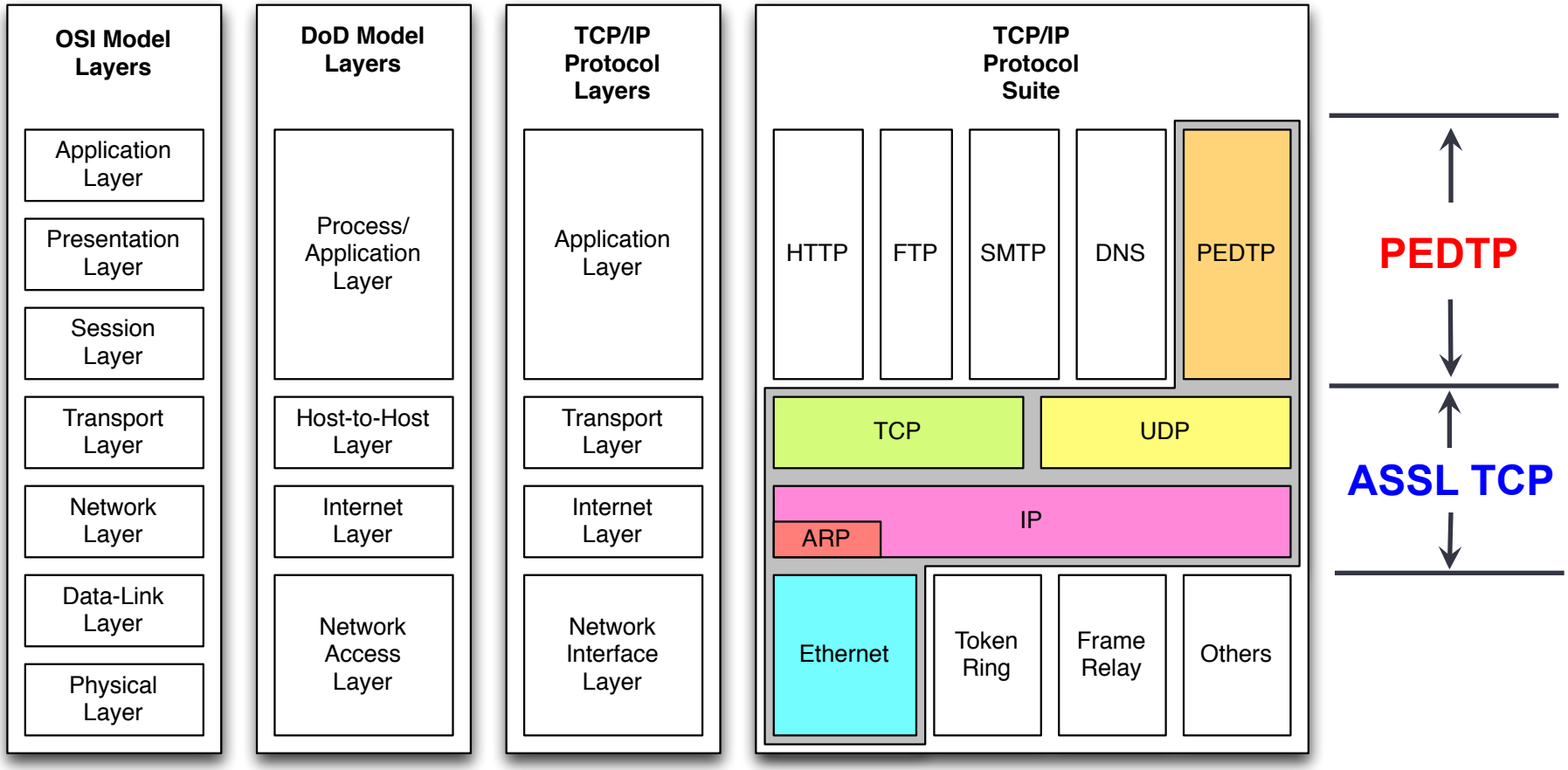
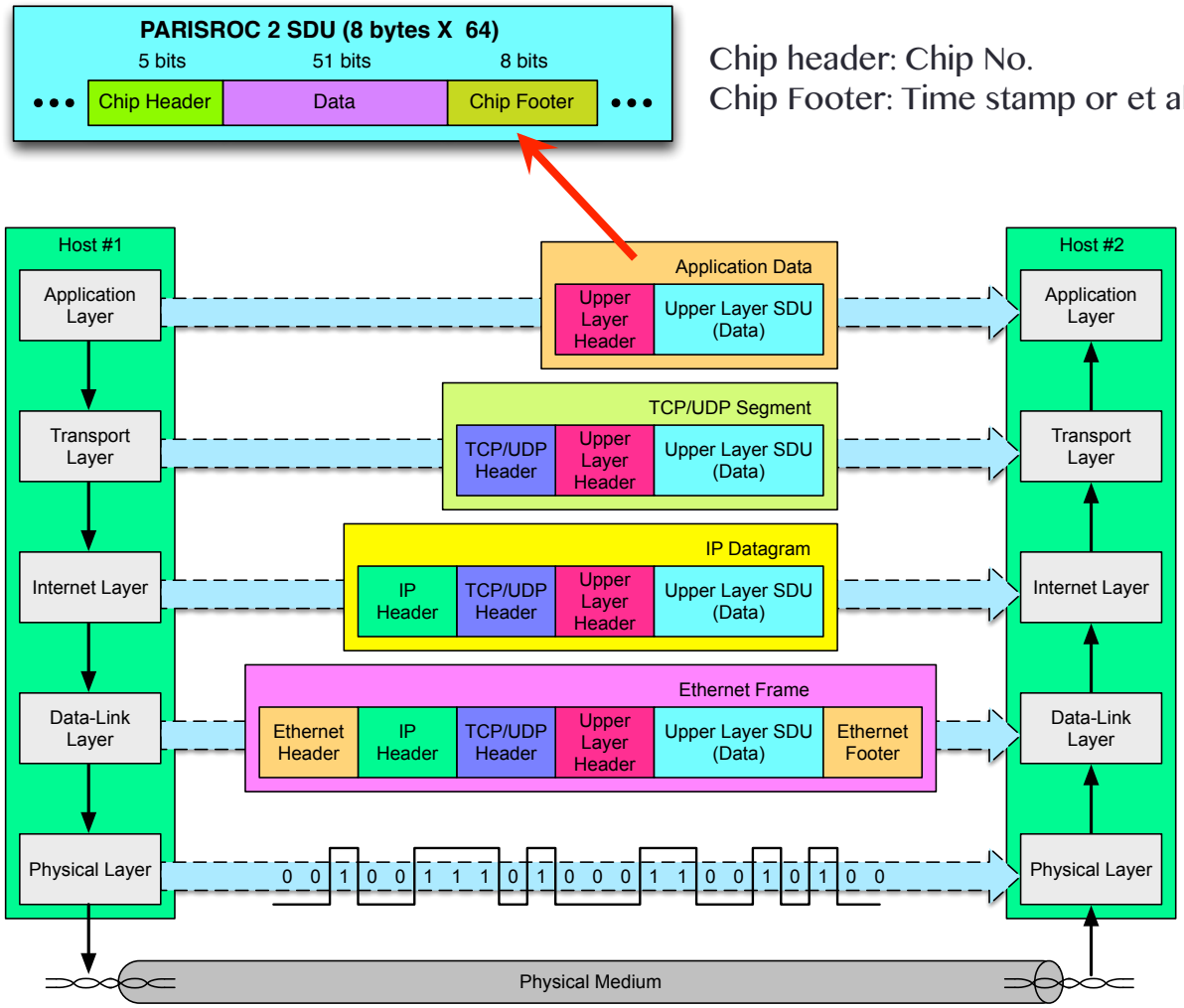
New DAQ system

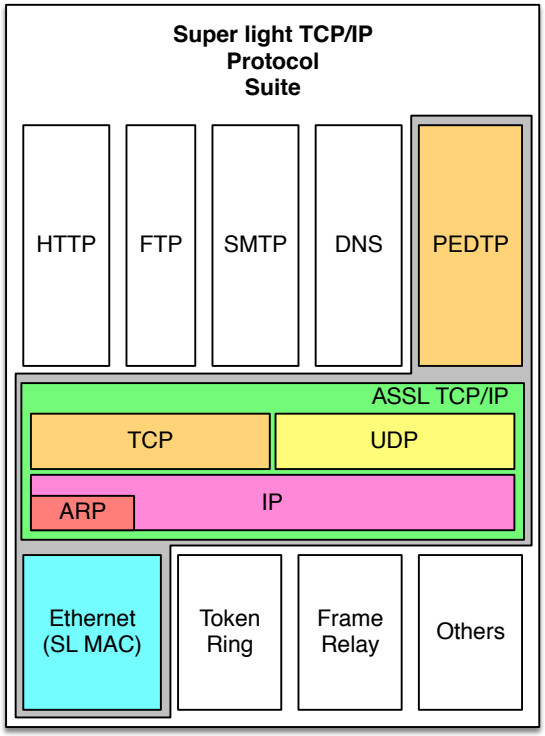
New DAQ system = ASSL TCP/IP + PEDTP

- ASSL TCP/IP (Application Specific Super Light TCP/IP Protocol)
- PEDTP (Physics Experiment Data Transferring Protocol)



Communication over Ethernet





Bandwidth test
FEE ➔Ethernet data logger
Highest bandwidth: 972 Mbit/s

Observed max. throughput:
> 80 Mbit/s (ASSL UDP)

Application Specific Super Light TCP/IP Protocol

- Internet Protocol Version 4 (IPv4) (RFC 791)
- User Datagram Protocol (UDP) (RFC 768)
- Transmission Control Protocol (TCP) (RFC 793 et al.)
- Support TCP options for High performance network (RFC 1323)
  - Max segment size (MSS)
  - Windows Scaling (WS)
  - Timestamp (TS): not yet
  - Selective Acknowledgment (SACK): not yet
- Scalable
- User-defined features for different purposes
- Standard program languages (C, C# ...)
- Modern Operating System supports TCP/IP (Windows, MAC OS, Linux···)

Host computer (as client: 192.168.0.5)

Establish connection

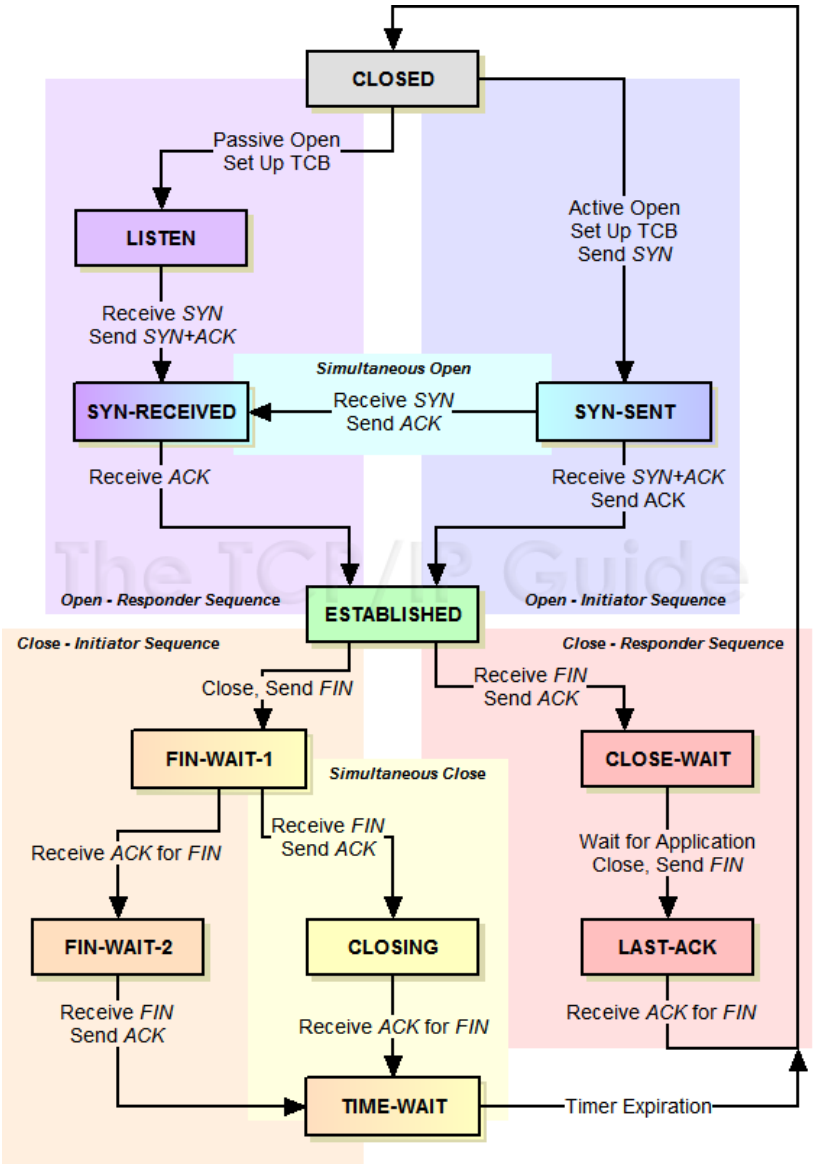
Get Temperature

No.	Time	Source	Destination	Protocol	Length	Info
6	11.131110000	192.168.0.5	192.168.0.25	TCP	78	owms > silhouette [SYN] Seq=0 Win=65535 Len=0 MSS=1460 WS=256 TSval=0 TSecr=0 SACK_PERM=1
7	11.131203000	192.168.0.25	192.168.0.5	TCP	62	silhouette > owms [SYN, ACK] Seq=0 Ack=1 Win=4095 Len=0 MSS=1460 WS=1
8	11.131222000	192.168.0.5	192.168.0.25	TCP	54	owms > silhouette [ACK] Seq=1 Ack=1 Win=16776960 Len=0
11	13.352793000	192.168.0.5	192.168.0.25	TCP	66	owms > silhouette [PSH, ACK] Seq=1 Ack=1 Win=16776960 Len=12
12	13.352884000	192.168.0.25	192.168.0.5	TCP	60	silhouette > owms [ACK] Seq=1 Ack=13 Win=4083 Len=0
13	13.352891000	192.168.0.25	192.168.0.5	TCP	68	silhouette > owms [PSH, ACK] Seq=1 Ack=13 Win=4095 Len=14
14	13.352899000	192.168.0.5	192.168.0.25	TCP	54	owms > silhouette [ACK] Seq=13 Ack=15 Win=16776704 Len=0
15	15.898011000	192.168.0.5	192.168.0.25	TCP	54	owms > silhouette [FIN, ACK] Seq=13 Ack=15 Win=16776704 Len=0
16	15.898221000	192.168.0.25	192.168.0.5	TCP	60	silhouette > owms [ACK] Seq=15 Ack=14 Win=4095 Len=0
17	15.898229000	192.168.0.25	192.168.0.5	TCP	60	silhouette > owms [FIN, ACK] Seq=15 Ack=14 Win=4095 Len=0
18	15.898236000	192.168.0.5	192.168.0.25	TCP	54	owms > silhouette [ACK] Seq=14 Ack=16 Win=16776704 Len=0

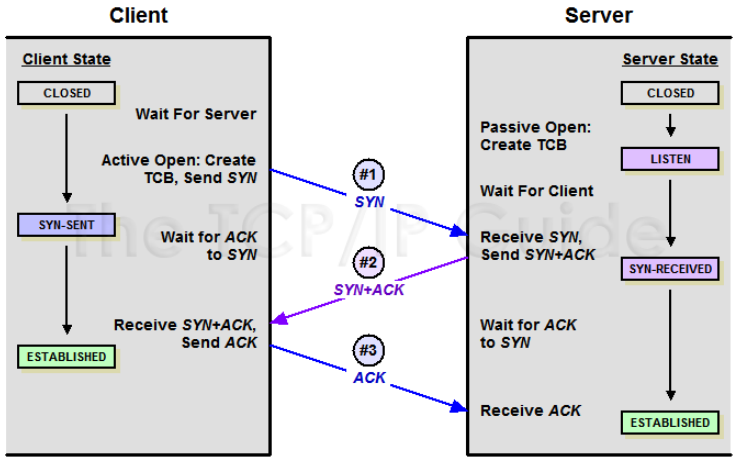
DPFEE FPGA (as server: 192.168.0.25)

Terminate connection

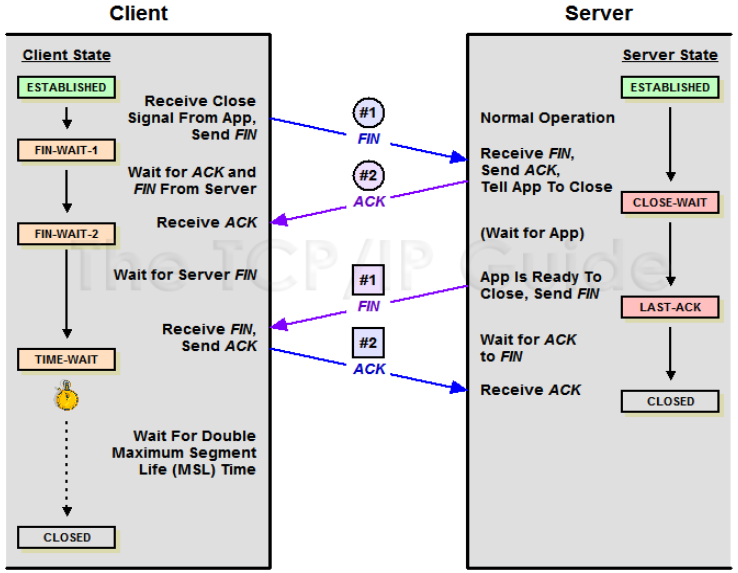
TCP establishment & termination



"Three-Way Handshake" establishment

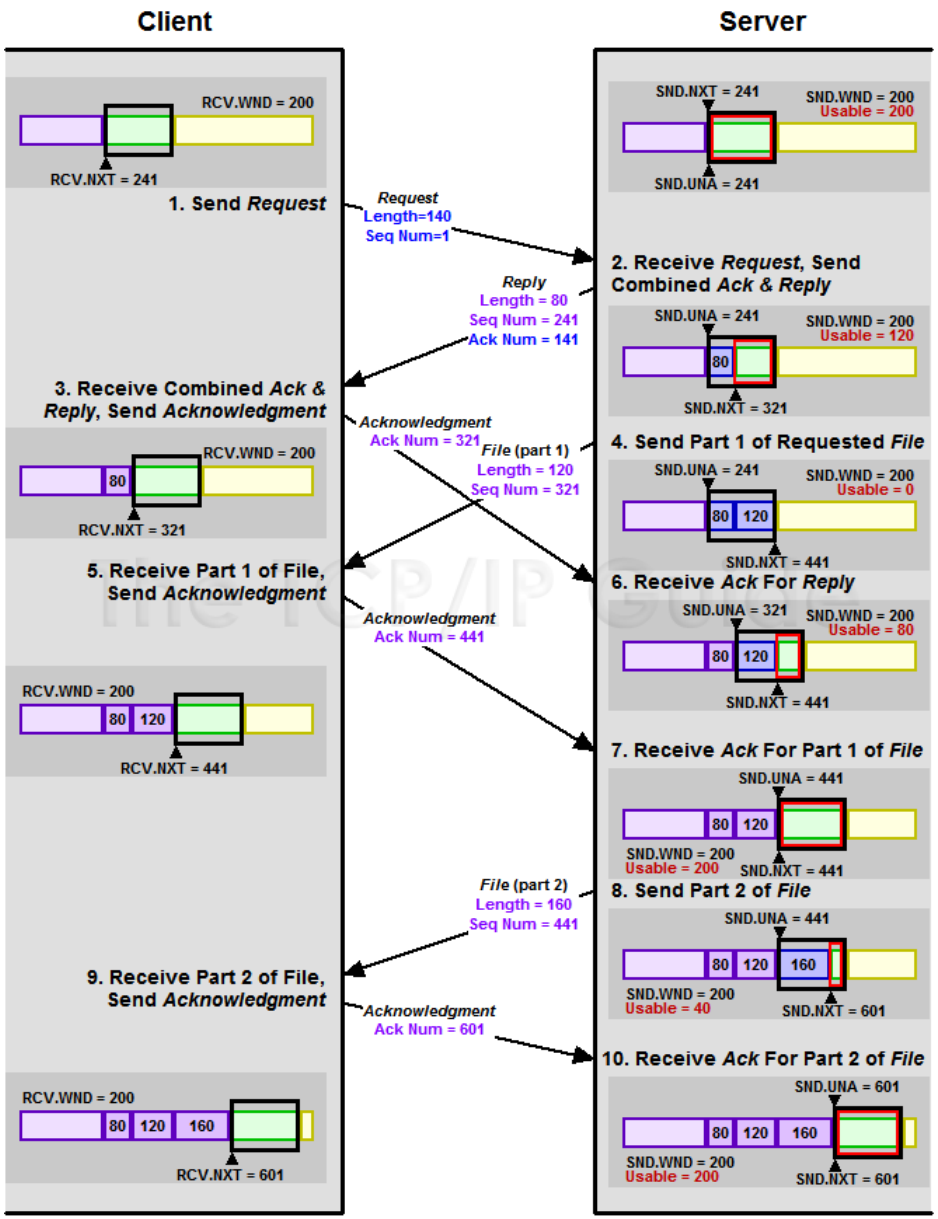


"Four Wave" termination



Kozierok, The TCP/IP Guide: A Comprehensive, Illustrated Internet Protocols Reference,2005

TCP data transferring



Variables:

- Sequence No.
- Acknowledgement No.
- Unacknowledged No.
- Next acknowledged No.
- Send Windows Size
- Receive Windows Size

Features:

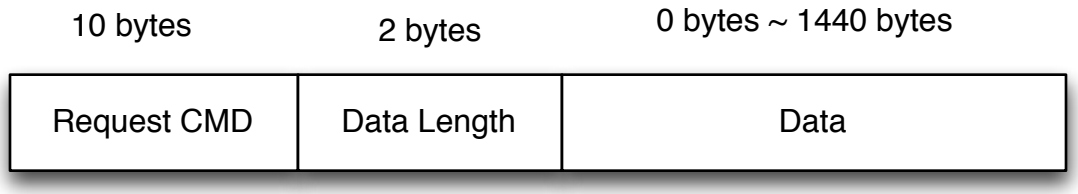
- ✓ Reliable delivery
- ✓ Flow Control
- ✓ Congestion Control

Kozierok, The TCP/IP Guide: A Comprehensive, Illustrated Internet Protocols Reference,2005

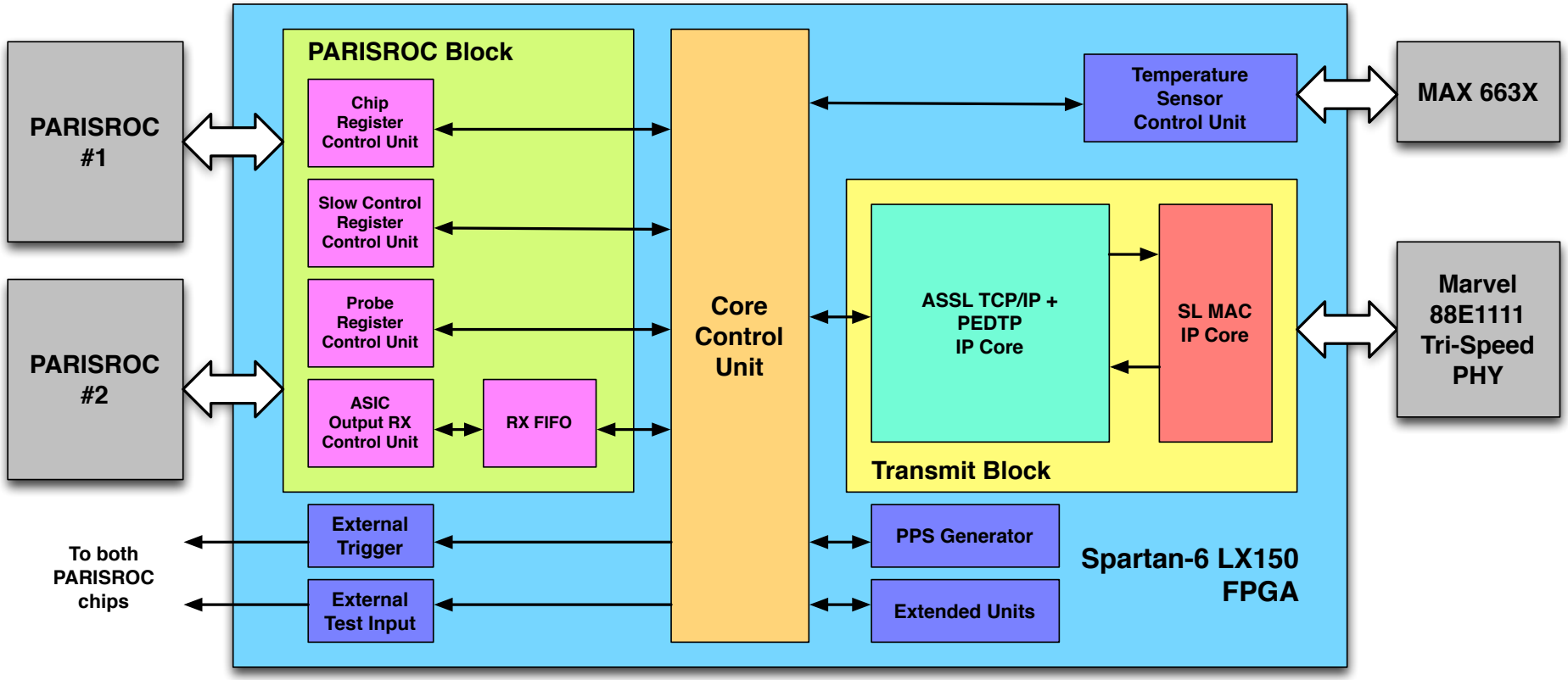
Physics Experiment Data Transferring Protocol

- Protocol based on ASSL TCP/IP for physics experiments or specific application (ROCs from OMEGA)
- User-defined protocol
- "Message" kind of protocol as HTTP (HyperText Transfer Protocol)
- Request commands
  - "SET": Set parameters ("/SET SLC /": setting slow control parameters)
  - "GET": Get parameters ("/GET TEMP/": get temperature sensor data)
  - "STA": Start operation ("/STA ACQU/": start data acquisition)
  - "STP": Stop operation ("/STP ACQU/": stop data acquisition)
  - "SND": Send data to host ("/SND TEMP/": send temp. data to host)

Message structure



FPGA Block with new protocol



- All HDL codes have been rewritten.
- Full synchronized circuit and better FSM structure.
- FPGA resources occupation: < 10% (XC6SLX150)

- Immediately acknowledgement
- 1506 bytes per frame
- 2K Sending Buffer

TCP/IP Examples

Observed max. throughput: ~ 40 Mbit/s

200 ms interval & packet resend

82	136.053592000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=3091 Ack=67 Win=4096 Len=513
83	136.254404000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=3604 Win=65022 Len=0
84	136.254567000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=3604 Ack=67 Win=4096 Len=513
85	136.455417000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=4117 Win=64509 Len=0
86	141.113048000	192.168.0.25	192.168.0.5	TCP	567 [TCP Retransmission] silhouette > owms [PSH, ACK] Seq=3604 Ack=67 Win=4096 Len=513
87	141.113065000	192.168.0.5	192.168.0.25	TCP	54 [TCP Dup ACK 85#1] owms > silhouette [ACK] Seq=67 Ack=4117 Win=64509 Len=0
88	141.113189000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=4117 Ack=67 Win=4096 Len=513
89	141.280537000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=4630 Win=65535 Len=0
90	141.280708000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=4630 Ack=67 Win=4096 Len=513
91	141.481561000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=5143 Win=65022 Len=0
92	141.481737000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=5143 Ack=67 Win=4096 Len=513
93	141.682579000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=5656 Win=64509 Len=0
94	141.682749000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=5656 Ack=67 Win=4096 Len=513
95	141.883681000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=6169 Win=65535 Len=0
96	141.883854000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=6169 Ack=67 Win=4096 Len=513
97	142.084679000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=67 Ack=6682 Win=65022 Len=0
98	146.112910000	192.168.0.25	192.168.0.5	TCP	567 [TCP Retransmission] silhouette > owms [PSH, ACK] Seq=6169 Ack=67 Win=4096 Len=513
99	146.112926000	192.168.0.5	192.168.0.25	TCP	54 [TCP Dup ACK 97#1] owms > silhouette [ACK] Seq=67 Ack=6682 Win=65022 Len=0
100	146.113063000	192.168.0.25	192.168.0.5	TCP	567 silhouette > owms [PSH, ACK] Seq=6682 Ack=67 Win=4096 Len=513

Immediate acknowledgement: no. 88 to 89: ~16 us; no. 90 to 89: ~182 us

80	32.617986000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=30568 Ack=116 Win=4095 Len=1452
81	32.617993000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=32020 Win=16752128 Len=0
82	32.618579000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=32020 Ack=116 Win=4095 Len=1452
83	32.618586000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=33472 Win=16750592 Len=0
84	32.619125000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=33472 Ack=116 Win=4095 Len=1452
85	32.619136000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=34924 Win=16749312 Len=0
86	32.634638000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=34924 Ack=116 Win=4095 Len=1452
87	32.634661000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=36376 Win=16747776 Len=0
88	32.634939000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=36376 Ack=116 Win=4095 Len=1452
89	32.634955000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=37828 Win=16746240 Len=0
90	32.635137000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=37828 Ack=116 Win=4095 Len=1452
91	32.635147000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=39280 Win=16744960 Len=0
92	32.635527000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=39280 Ack=116 Win=4095 Len=1452
93	32.635537000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=40732 Win=16743424 Len=0
94	32.635719000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=40732 Ack=116 Win=4095 Len=1452
95	32.635728000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=42184 Win=16741888 Len=0
96	32.636191000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=42184 Ack=116 Win=4095 Len=1452
97	32.636231000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=43636 Win=16740608 Len=0
98	32.636782000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=43636 Ack=116 Win=4095 Len=1452
99	32.636793000	192.168.0.5	192.168.0.25	TCP	54 owms > silhouette [ACK] Seq=116 Ack=45088 Win=16739072 Len=0
100	32.637372000	192.168.0.25	192.168.0.5	TCP	1506 silhouette > owms [PSH, ACK] Seq=45088 Ack=116 Win=4095 Len=1452

Performance of the protocol

- The performance of TCP/IP protocol are related to:
  - Quality of connection
    - Round-trip delay time (RTT)
    - Packet drop rate
  - Size of the Packet
    - Default: 1.5K
    - Jumbo frame: 9K;
  - Configuration at both sides (server and client)
    - Support RFC1323 option
    - Sending & Receiving window size
    - Acknowledgement strategy
      - Immediate acknowledgement
      - Delayed acknowledgement (RFC1122, Windows XP: 200 ms)
    - User Application
  - Resources at both sides
    - RAMs in FPGA (Send buffer: 2K; Receive buffer: 4K)

Conclusions

- A new prototype front-end electronics was designed, implemented and fabricated to fit the requirements of WFCTA.
- A new calibration method for mass verification was proposed and verified.
- It proved that the time measurement of PARISROC 2 could reach ~ 260 ps.
- Two new communication protocols, which are ASSL TCP/IP and PEDTP were proposed, implemented and tested.
- The throughout of the protocols are > 80 Mbit/s (ASSL UDP/IP) and ~ 40 Mbit/s (ASSL TCP/IP) for this version.
- The performance of the protocol will be improved in future.
- The PARISROC 3 is being fabricated in AMS. The new prototype front-end based on it will be ready in July.

Thank you
for your attention!