CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

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REVIEW OF THE ATLAS SILICON DETECTOR R&D PROJECT WORK

FCPPL 2015 — Heife, CHINA

Patrick Pangaud — CPPM

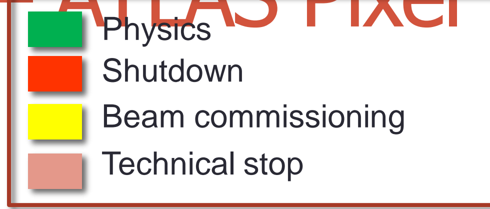
8 April 2015

On behalf of the Silicon detector FCPPL project

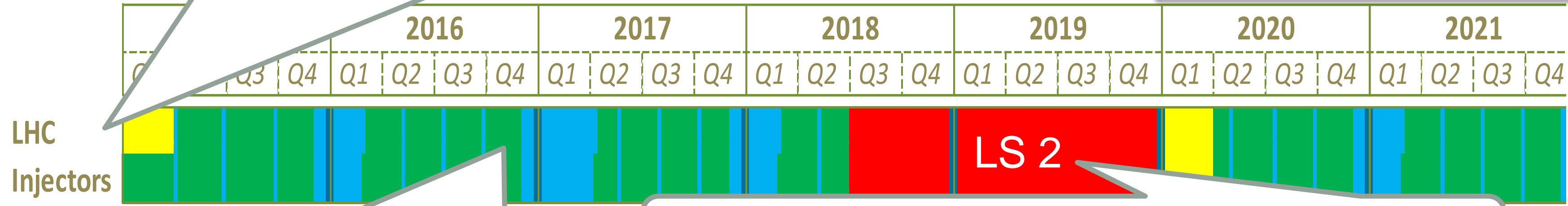
CPPM / Atlas Chinese Cluster Collaboration

- CPPM / ACC collaboration for design and test of Front-End pixel electronics for ATLAS phase II upgrade.
- Scientific cooperation supervised by Pr. Xinchou LOU, Dr. Zheng WANG and Dr. Alexander ROZANOV, derived from ATLAS CPPM / ACC project (Pr. Shan JIN / Dr. Emmanuel MONNIER).
- Co-PhD Jian Liu (SDU – Pr. Meng WANG / CPPM – Pr. Marlon BARBERO & Dr. Alexander ROZANOV).
- The last development topics involve:
  - The investigation of technology access via SMIC foundry in China. Wei WEI (IHEP) .
  - The tests and simulation in several HV CMOS technology. Jian Liu (SDU /CPPM).

LHC Upgrade Schedule Beyond LS1 – ATLAS Pixel P



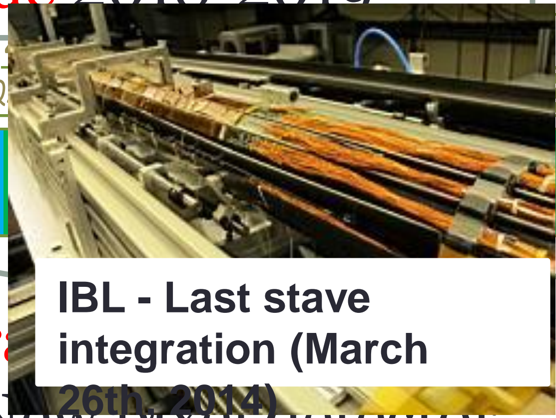
Phase 0 upgrade
2013-2014: IBL building and IBL insertion.



Phase 1 upgrade 2018-2019

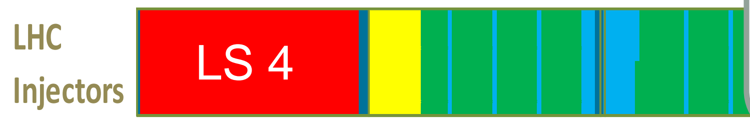
2015-2018: IBL + the current 3-layer pixel detector system

LHC
Injectors
LS 3



2020-2022: 2x nominal

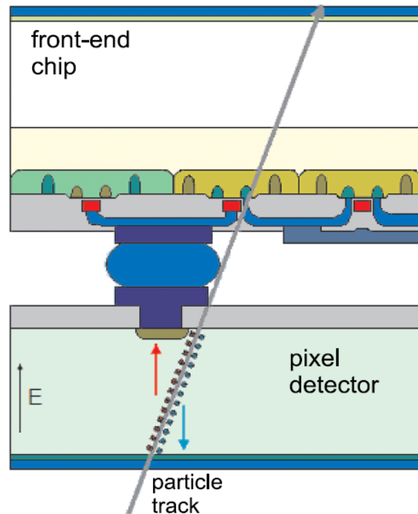
Phase 2 upgrade
2022-2025: New pixel detector → new technology

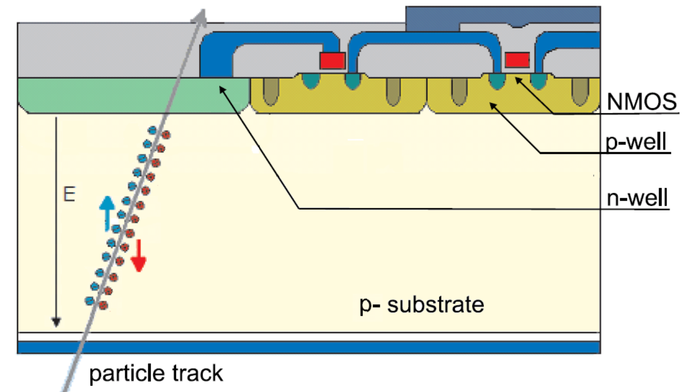


LS: Long Shutdown

LHC schedule approved by CERN management and LHC experiments spokespersons and technical coordinators (December 2013)

From Hybrid to Monolithic HVCMOS pixel





Hybrid Pixel Detectors Properties:

fine pitch flip-chip assembly of:

CMOS R/O chips (CSA + DSP per pixel)

Si (planar or 3D) or Diamond detectors

+ high density electronics

+ moderate - good SNR

- high material budget

- high cost (chip + sensor + hybridization)

Depleted MAPS for HL-LHC

large depletion depth d ~$(\rho V)^{1/2}$

AND full CMOS

AND low power

AND low cost

Questions:

→Radiation hardness (sensor / transistors).

→Signal to Noise Ratio / Efficiency.

courtesy of Bonn University

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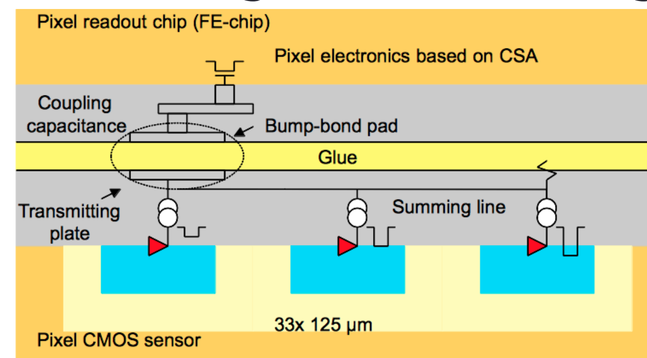
Why HVCMOS pixels for HEP ?

- Commercial process in large 8 or 12 inch wafers and potentially much cheaper than customer HEP sensors.
- Potentially much cheaper bonding processes available. (capacitive coupling gluing, oxide/Cu-Cu bonding)
- Smaller pitch due separation between CMOS sensor/analog tier and digital tier: sub-pixels in CMOS tier.
- Thin sensor (15-100 µm) reduce clusters at large η. (improve cluster size, two tracks resolution, sensor radiation hardness).
- For initial prototypes, FE-I4 digital tier is available, for final FE-RD53 will be suitable.
- Low occupancy layers (outer pixel, even strips) can be made in one tier with classical column or periphery readout architecture reducing the cost for large areas.



HVCMOS Demonstrator Working Group

- R&D started by Heidelberg-Berkley-Bonn-CERN-Geneva-Marseille since 2012.
- From June 2014 in the framework of ITK Pixel Module under chair of Norbert Wermes (Bonn) with many institutes :
  Karlsruhe-Berkley-Bonn-CERN-Geneva-Marseille-Gottingen-Prague-IRFU-Glasgow-Oxford-Liverpool-INFN-Genova-Milan-SLAC-UCSC-…….
- Address the development of Demonstrator Pixel module at end of 2015.
- Goal of preparing CMOS pixel option in the ITK Pixel TDR in 2017.
- Two main technology are explored for creating depletion region:
  HV (10-20 ohms.cm substrate and 30-90 V applied) or HR (0.1-3.0 Kohms. cm substrate) or both

Specification of CMOS Pixel (CPIX) Demonstrator

- Design Task Force (chair Maurice Garcia) Nov 2014
- Pixel module of 1-2 cm^2
- Radiation tolerance more than 50 MRads TID and 10^{15} neq.cm^{-2} NIEL
- Readout by the FE-I4 chip
- When possible also standalone readout
- Power less than 20 µA/pixel
- In-time efficiency more 95% after irradiation
- Bondable either by bumps or glue to FE-I4 with capacitive coupling
- Pin-out compatibility of demonstrators in different technologies for test by many groups

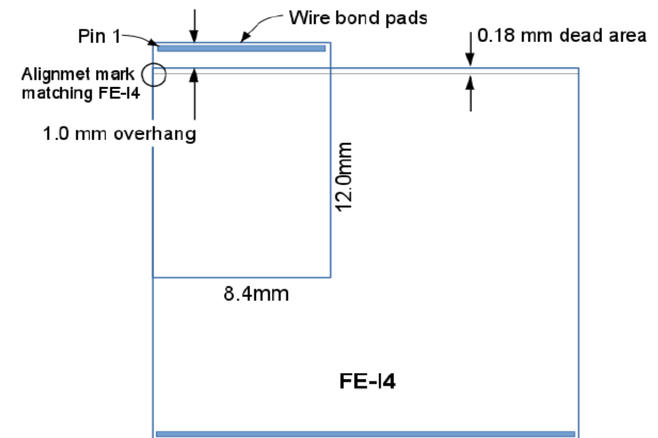


Fig. 1: Alignment of demonstrator to FE-I4 chip

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Planning for Demonstrator

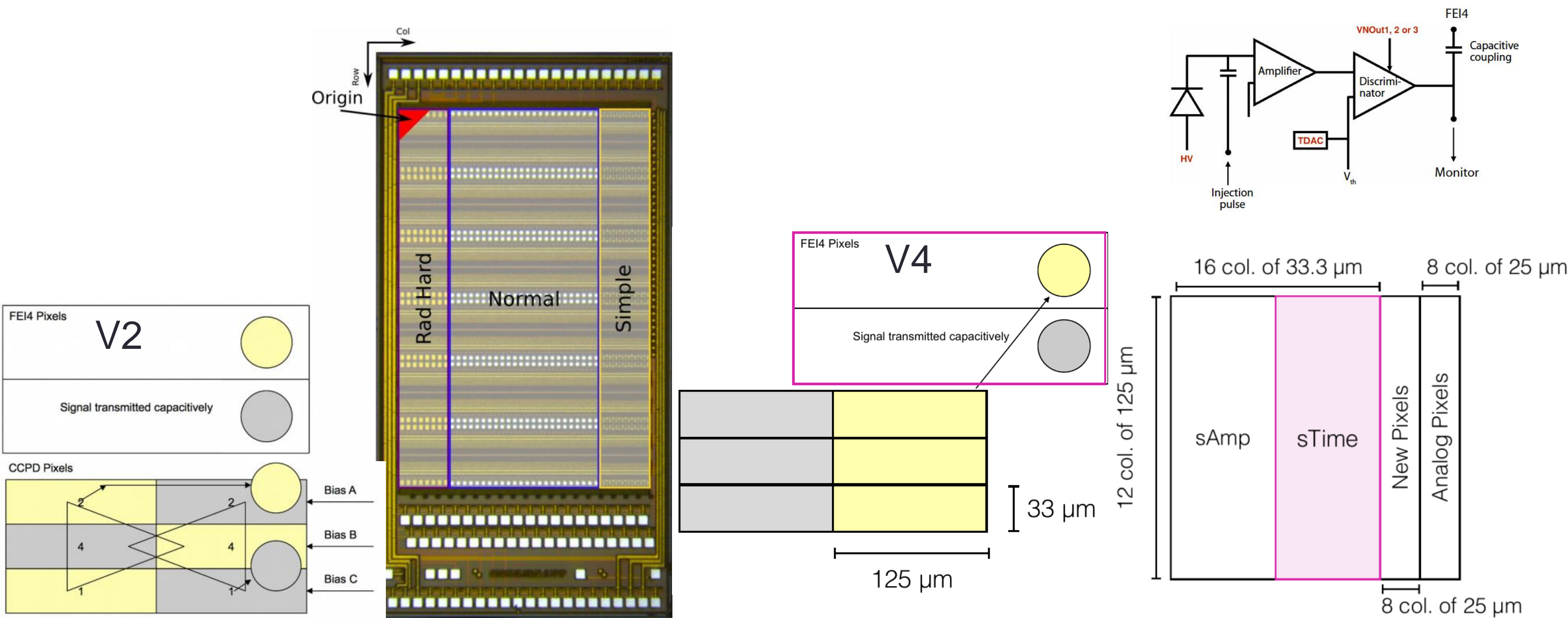
- Aug-Nov 2014 Prototypes, test results, Task Force specifications and recommendations
- Feb-June 2015 design and submission in 2-3 technologies
- Sep-Oct 2015 Characterization in the Labs
- End 2015 Demonstration in test beams and irradiations

Target Demonstrator submissions

Technology	Prototype	Demo design	Reticule (Full/MLM)	Submission Goal
Fab B 350nm	KA, CPPM,GVA,CERN Also strips	KA(Peric) DESY, SLAC/UCSC,…	Engineering run Full reticule	March 2015
FabA 180nm	KA, CPPM,GVA,BN, CERN	KA(Peric) CPPM	Engineering run Full reticule	Fall 2015
FabH 130nm	CPPM	CPPM (Pangaud) IRFU, KA	Full reticule	Fall 2015 ?
Fab G 150nm	BN, CPPM,KA	BN(Kruger) SLAC/LBL CPPM	MLM4->MLM2	June 2015
FabD SOI 180nm	BN, CERN	BN(Hemperek)	MLM4	August 2015

AMS-180nm CCPD prototypes

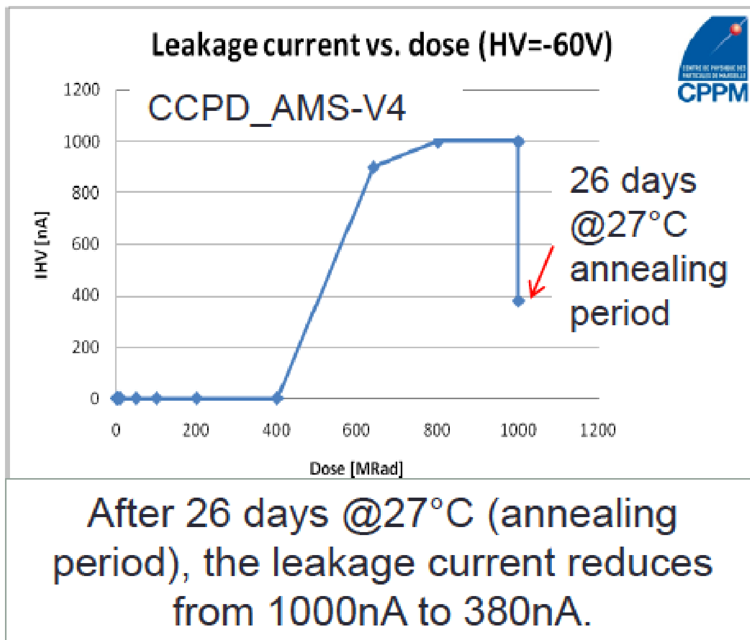
- Four versions tested standalone and glued on FE-I4.
- HV with 10 ohm wafer now.
  Prospect of HR ~100 ohms or 2k ohms in fall 2015
- 3 CMOS sub-pixels 33x125 um readout by one FE-I4 pixel of 50x250 um



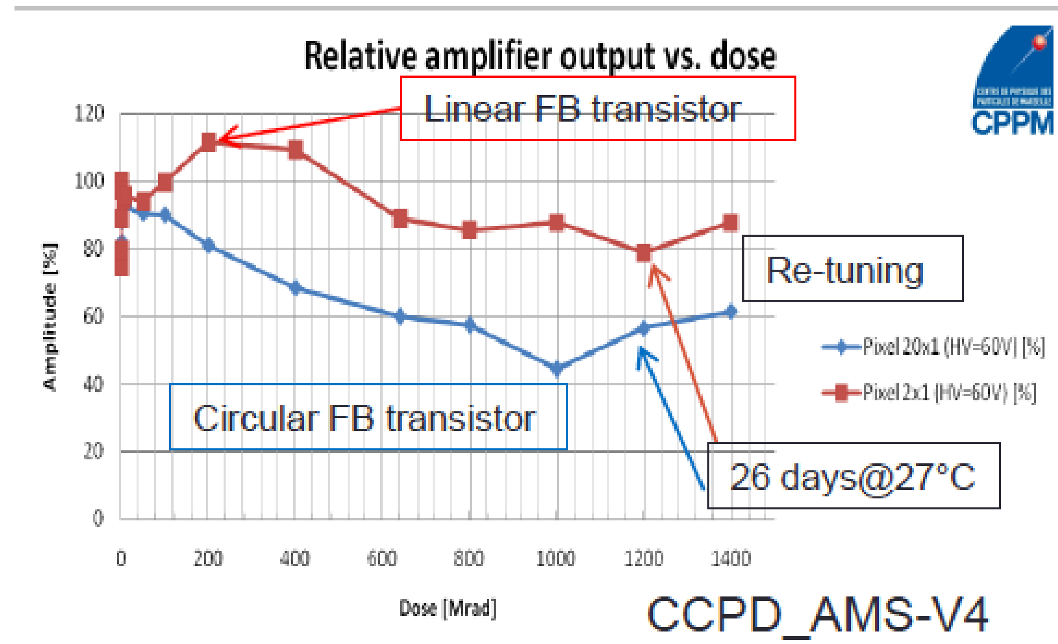
CCPD-AMS_V4 X-ray irradiation

Jian Liu (CPPM/SDU)

- Stand-alone CCPD-AMS_V4 irradiated up to 1000 MRads in X-rays
- Increase of leakage current only after 400 MRads
- After 26 days room temperature annealing drop to 380 nA, no need for high temperature annealing as for V2
- Amplifier with linear FB transistor stable (+-15%) up to 1 Grads, but noisy after 100 MRads



After 26 days @27°C (annealing period), the leakage current reduces from 1000nA to 380nA.



CPPM — Centre de Physique des Particules de Marseille

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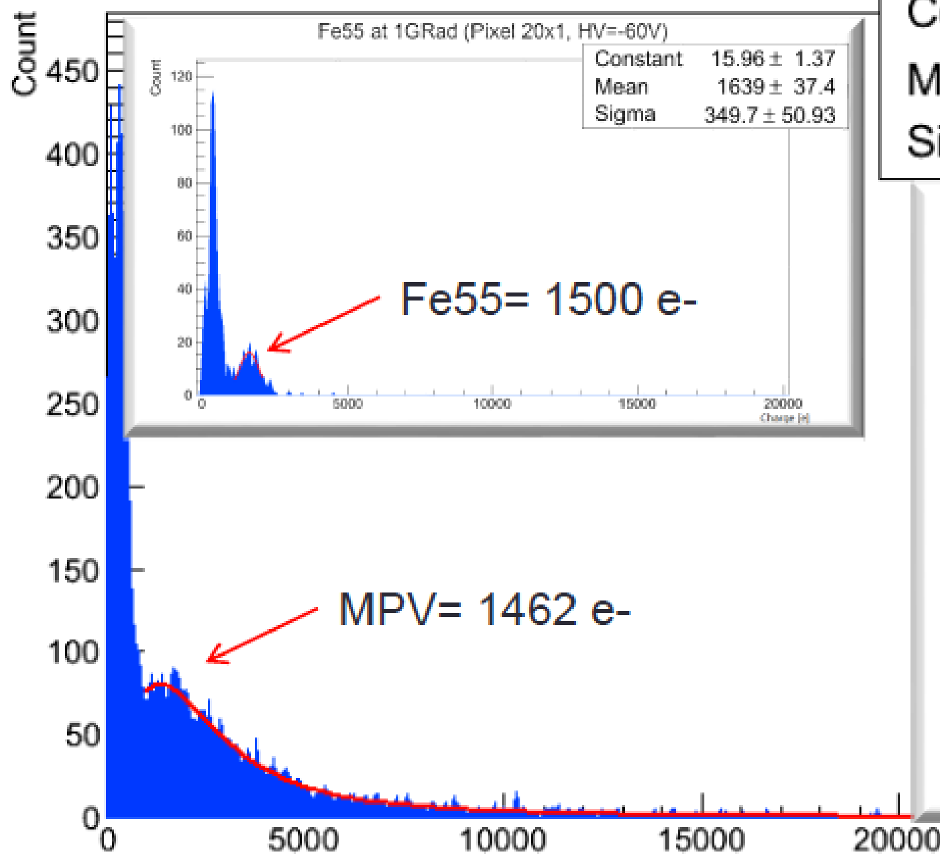
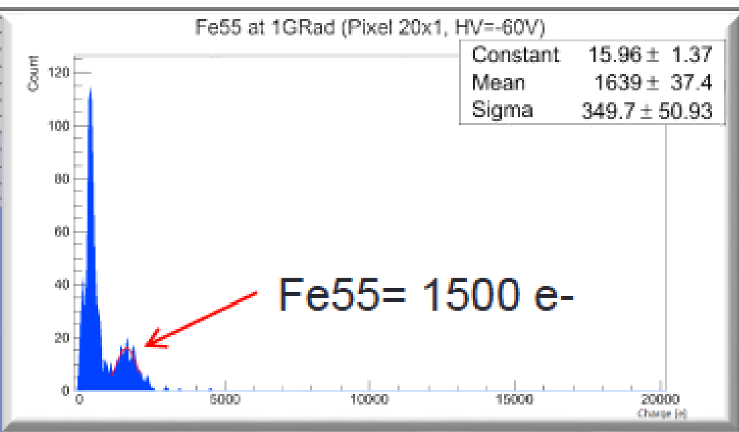
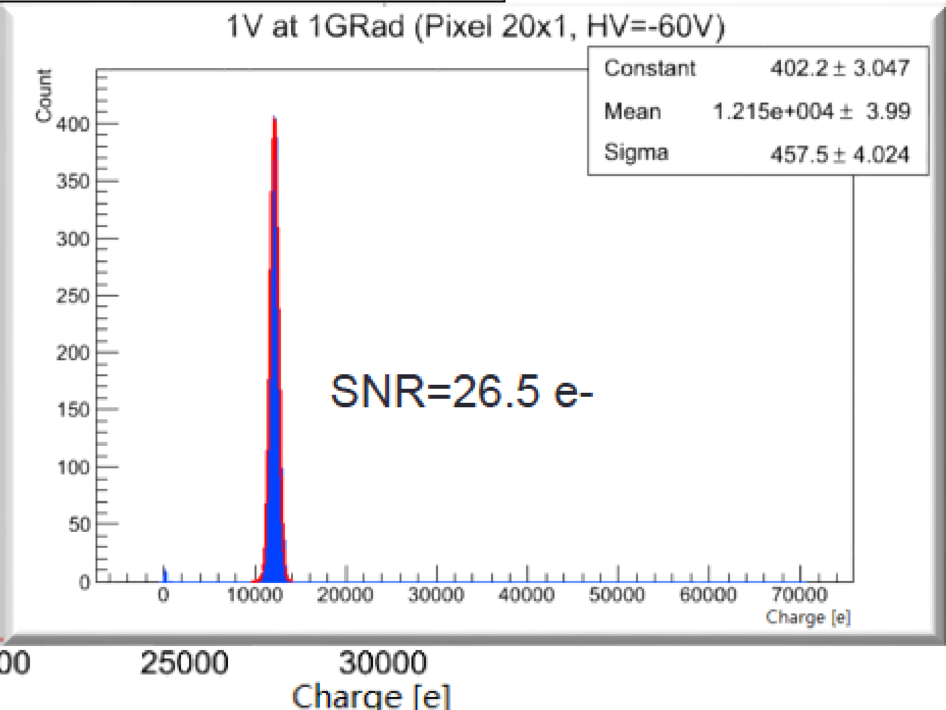
CCPD-AMS_V4 after 1 Grads in X-rays

Jian Liu (CPPM/SDU)

- Pixels with circular feedback transistors keep low noise up to 1 Grads, but more variation of gain.

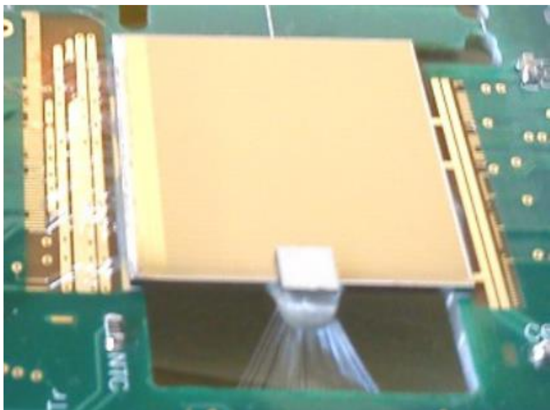


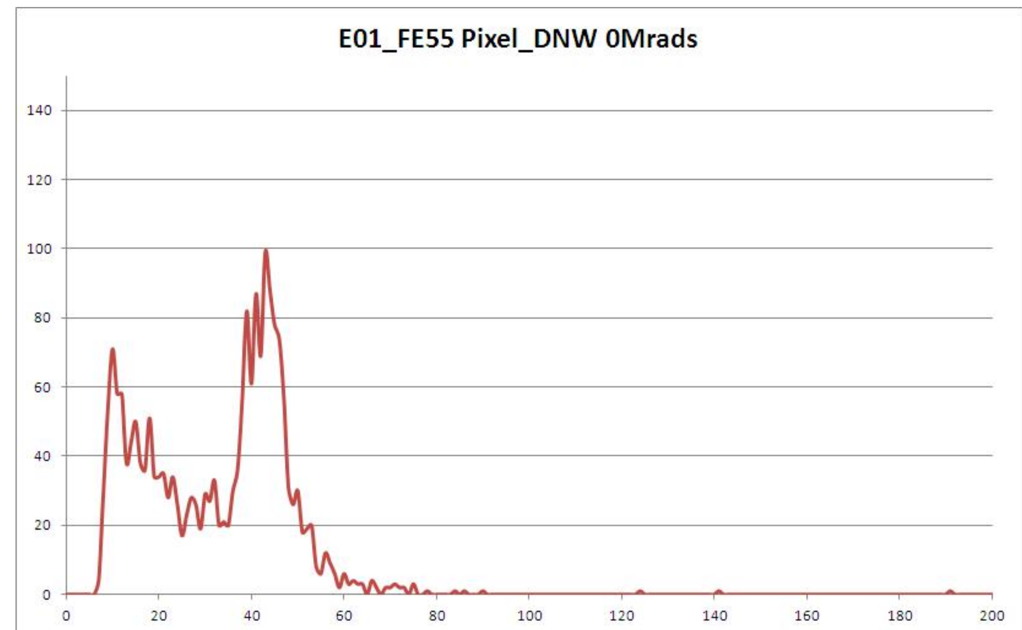




GF BCDLITE 130nm CCPD prototype

- Architecture similar to AMS CCPD 180nm pixel of 33x125 um, prototype with 10 ohm cm wafer
- Tested alone and glued on FE-I4
- ^{55}Fe and ^{90}Sr spectra measured
- Irradiated up to 1 Grad X-ray, the chip was alive
- For next prototype waiting the final decision on HR wafer usage





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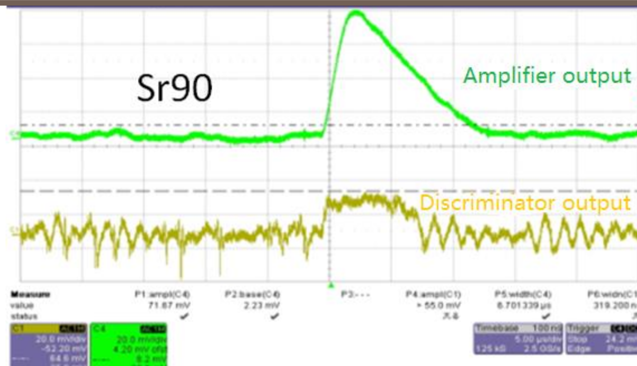
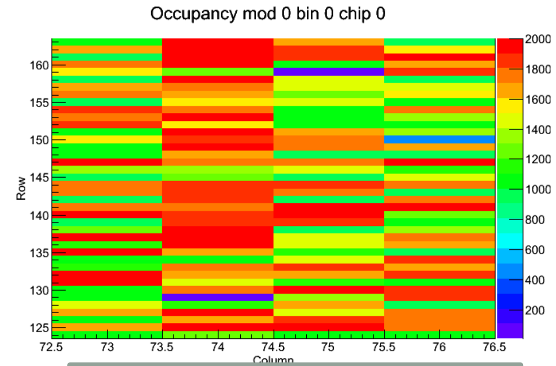
CCPD-GF Chip : Lab Test and General Functioning

Jian Liu (CPPM/SDU)

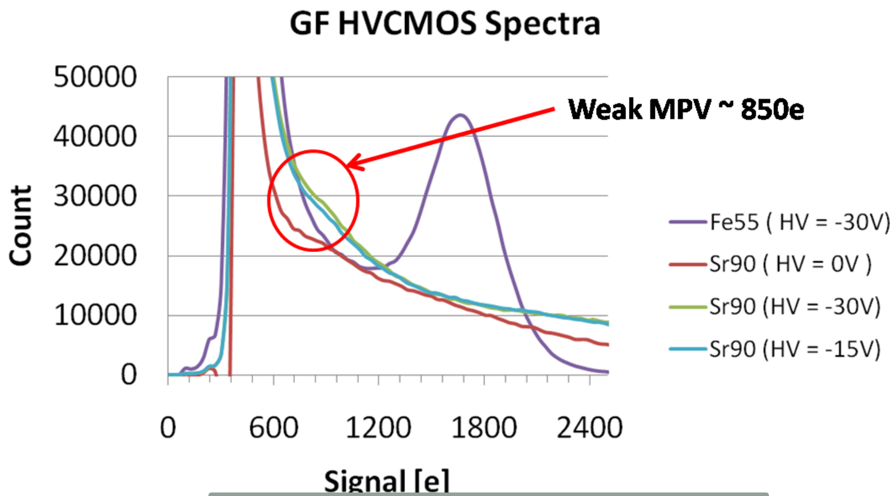
The chip works well with a HV of -30V.



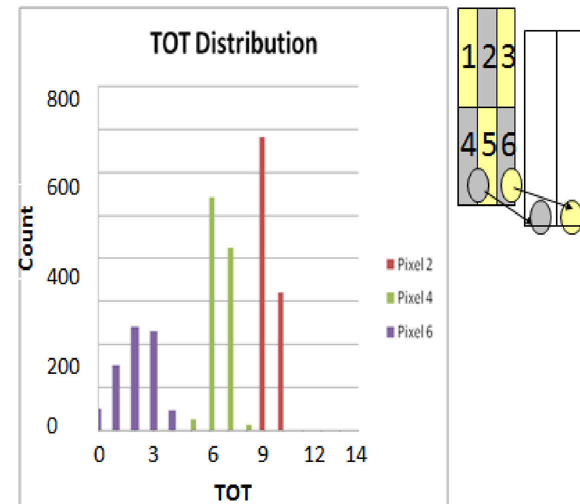
Amplifier and Comparator output



Occupancy of FE-I4



Spectra of amplifier output



CCPD pixel "2", "4" and "6" are read with weighted outputs to a single FE-I4 pixel.

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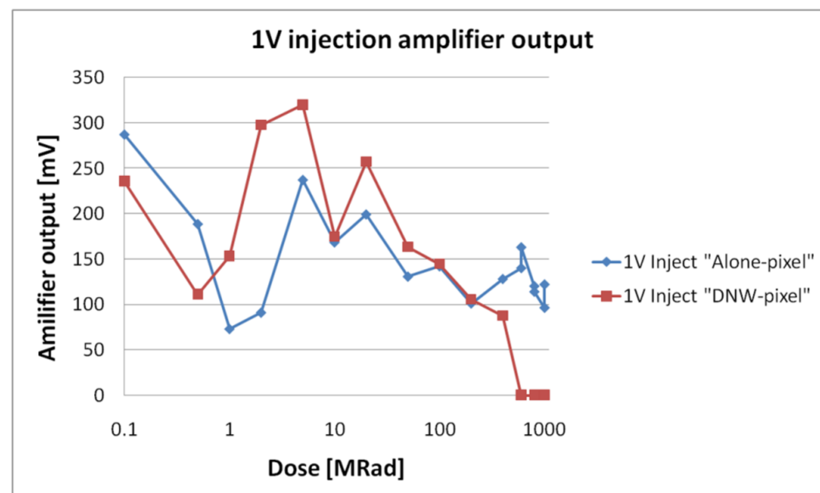
CCPD_GF Chip: Results under X-Rays

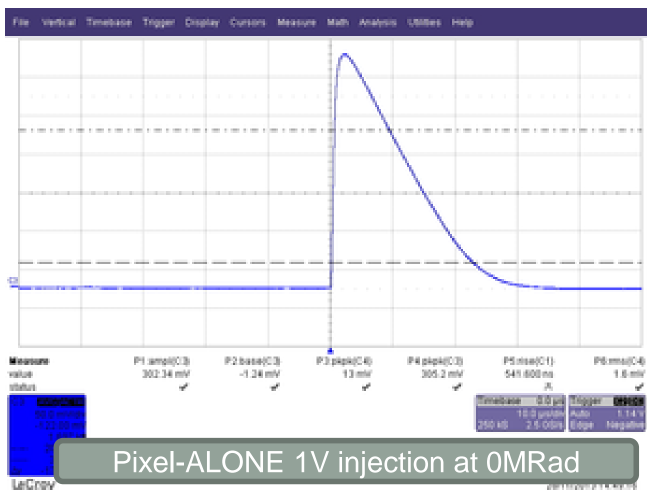
Jian Liu (CPPM/SDU)

After 1GRad irradiation, the amplifier of “Alone-pixel” is still alive. “DNW-pixel” is dead after 600MRads

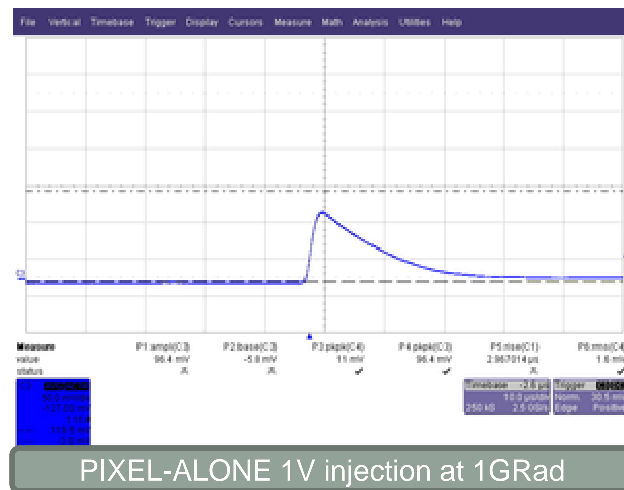
The "Alone-pixel" has the same footprint as the pixels used in the matrix, but contains only the preamplifier part (no discriminator).
The "DNW-pixel" also has the same footprint as the pixels used in the matrix, but it contains a sensor without electronics inside the DNW, and an additional preamplifier beside the sensor.



Amplifier output vs. Dose



Pixel-ALONE 1V injection at 0MRad



PIXEL-ALONE 1V injection at 1GRad

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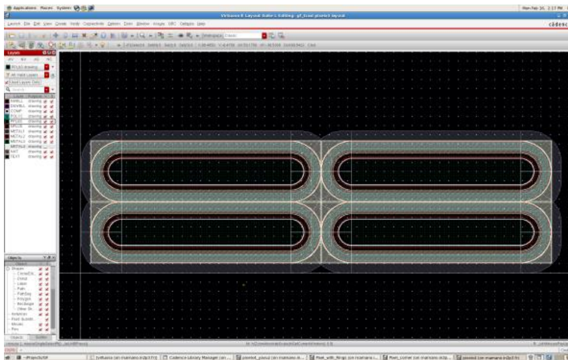
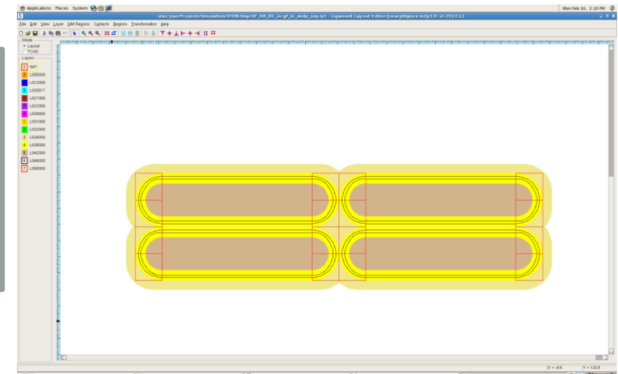
GF HR simulation procedures

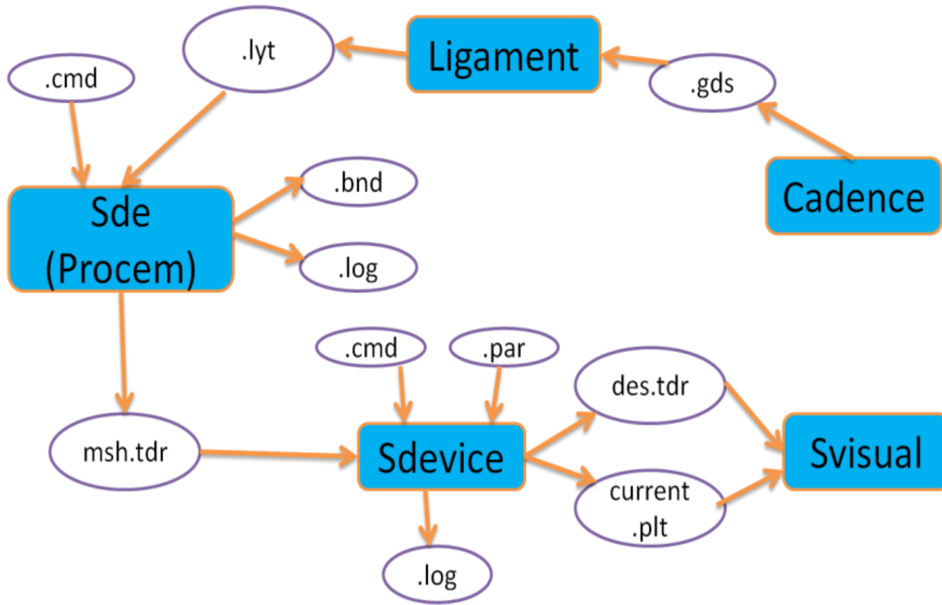
Jian Liu (CPPM/SDU)



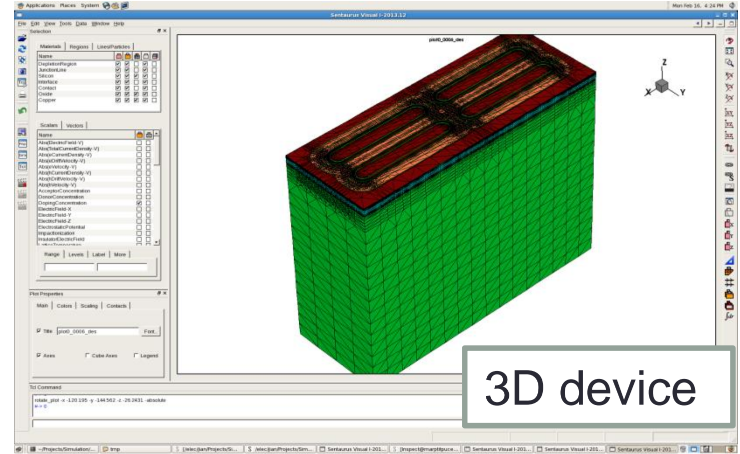


The round corners in .gds are converted to broken lines in .lyt.

Layout in Cadence → Transport to Sentaurus Ligament



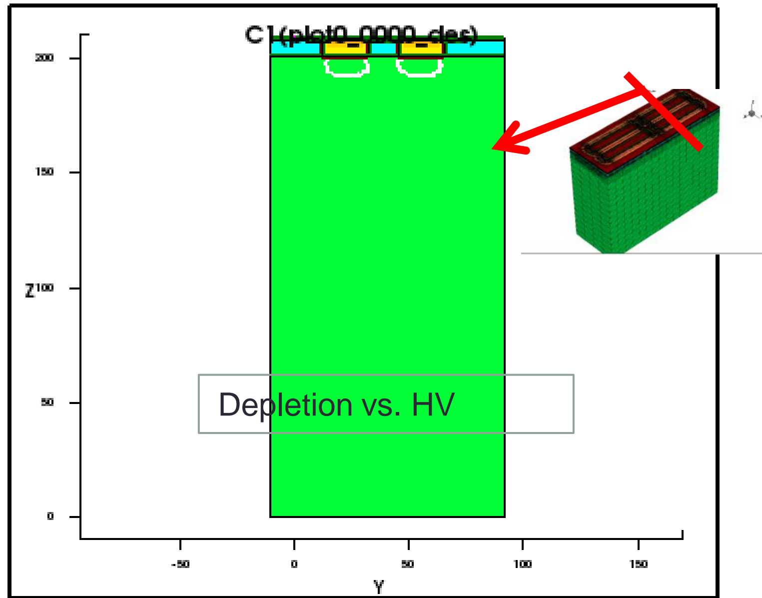
2x2 pixel array with standard DNW size.
7 um epi-layer.
200 um substrate (1kohm.cm).

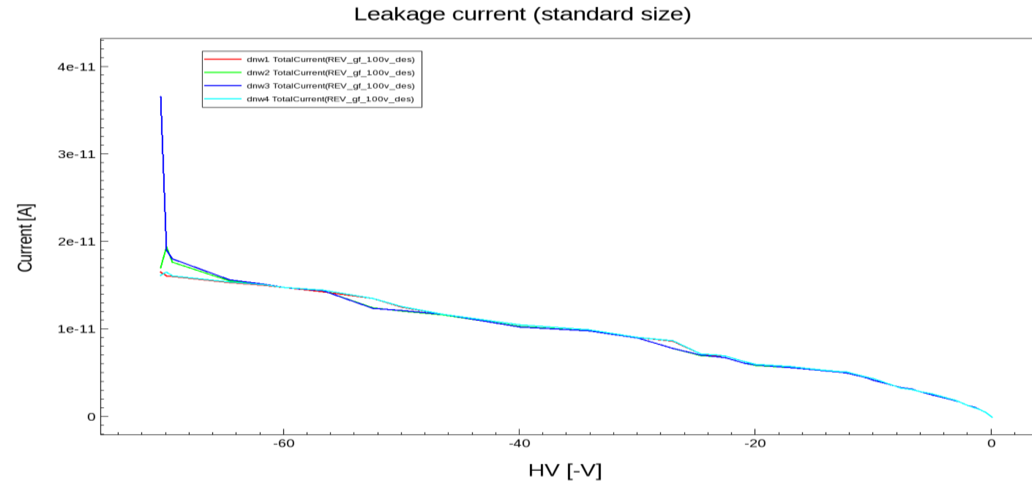


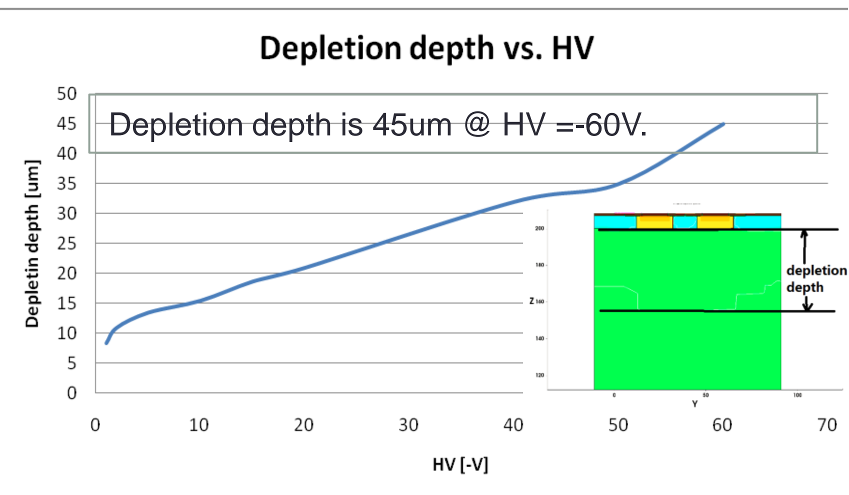
3D device

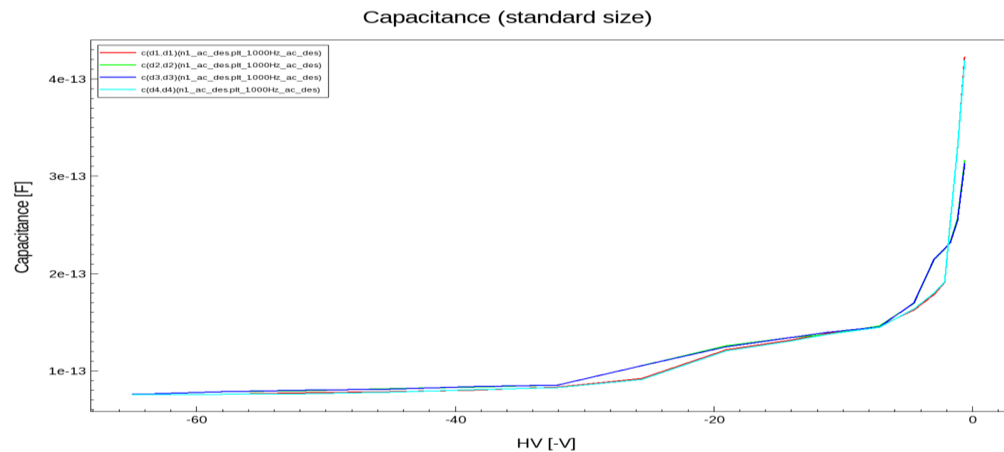
GF HR technology DC and AC simulations

Jian Liu (CPPM/SDU)









Breakdown ~70V.
Leakage current ~9.1 pA @ HV=30V
Capacitance ~85fF @ HV=30V

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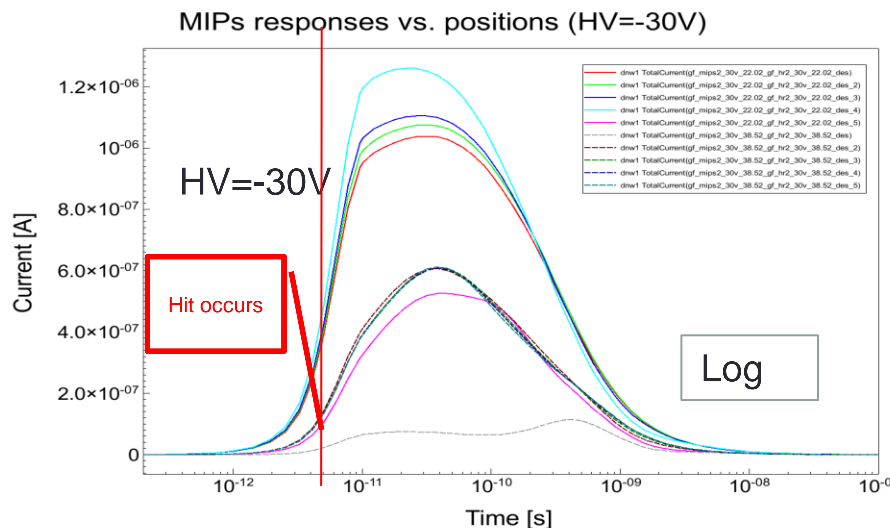
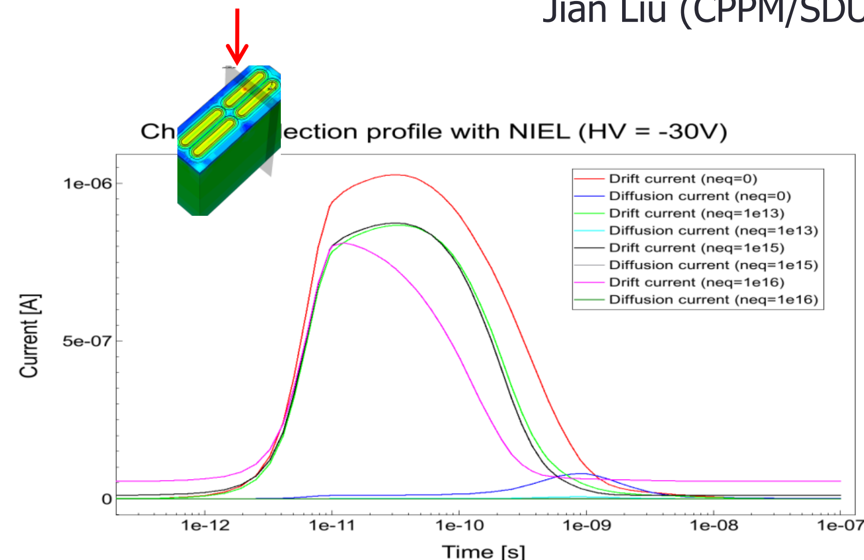
GF HR technology MIPs detection simulation

Jian Liu (CPPM/SDU)





Charge collection profiles with NIEL effect (impinging in the center of pixel).

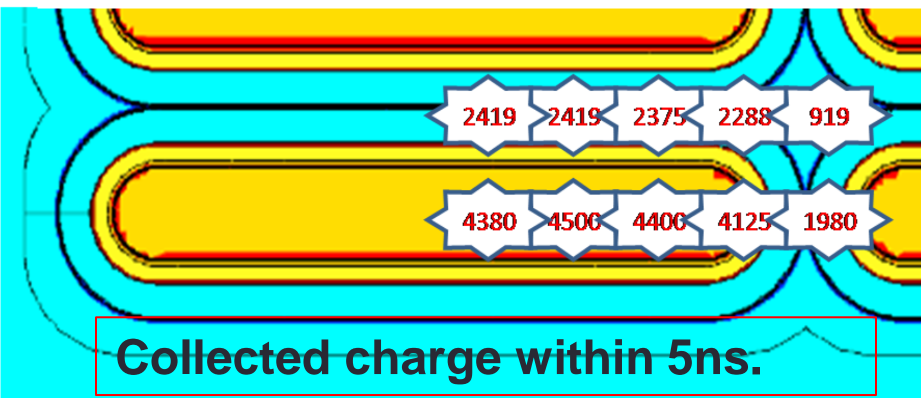


Table 3.4 – Charge collection profiles with NIEL effect (HV=-30V)

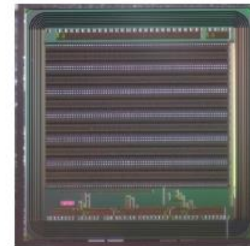
Fluence ($n_{eq} \cdot cm^{-2}$)	Drift charge (e-)	Diffusion charge (e-)	Total charge (e-)
0	3250	1130	4380
1×10^{13}	1981	81	2062
1×10^{15}	1125	31	1156
1×10^{16}	918	0	918

4380 electrons can be collected before irradiation.
Drift charge reduces due to decreasing depletion region after irradiation.
Diffusion charge killed after $10E^{13}$neq.cm^{-2} (~4MRads)

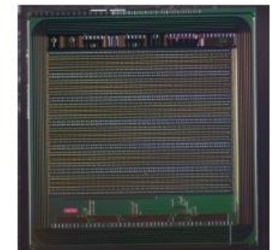
CCPD-LF 150 nm prototype

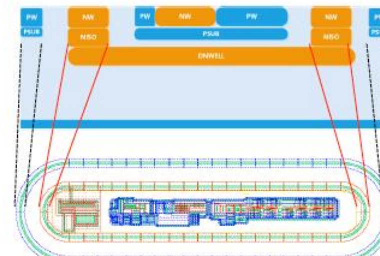
- Large fill factor for radiation hardness and charge collection
- Full CMOS , isolation via deep p-well (PSUB), wafer 2k ohms.cm
- 24x114 pixels of 33x125 um
- 3 CCPD pixels connected to one FE-I4 pixel
- First wafer arrived, chips under wire-bonding
- One passive sensor IV curve measured with 2nA/50V and breakdown at 120 V
- 5 wafers in thinning and backside implant processing

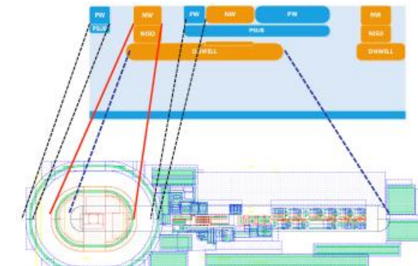
- CCPD_LF ver. A
  - CMOS inside collection electrode
  - Test structures: NMOS and PMOS transistors
- CCPD_LF ver. B
  - Smaller collection electrode
  - Test structure: diodes



Design: Bonn, CPPM, Heidelberg







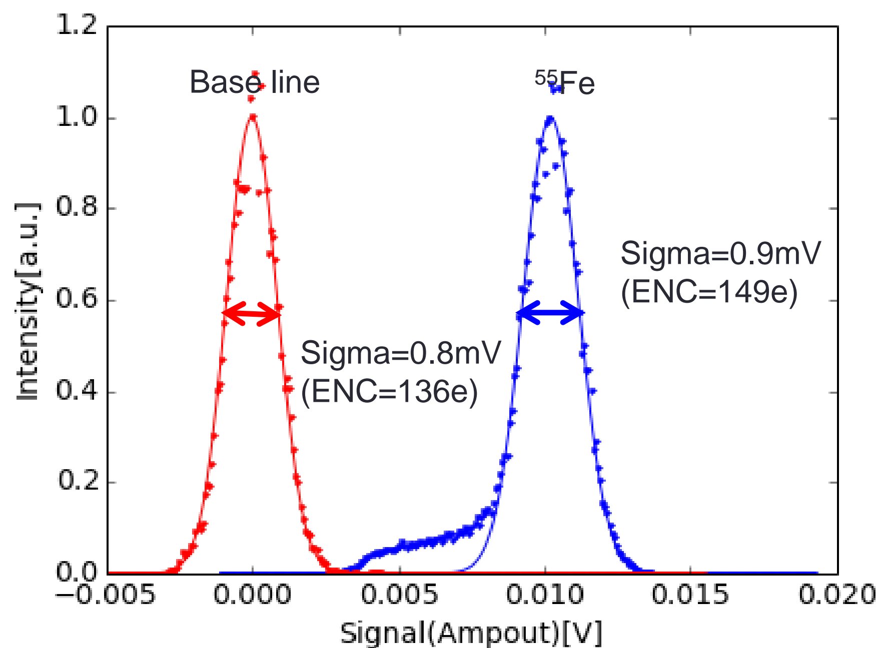
CCPD-LF 150 nm : ^{55}Fe spectrum

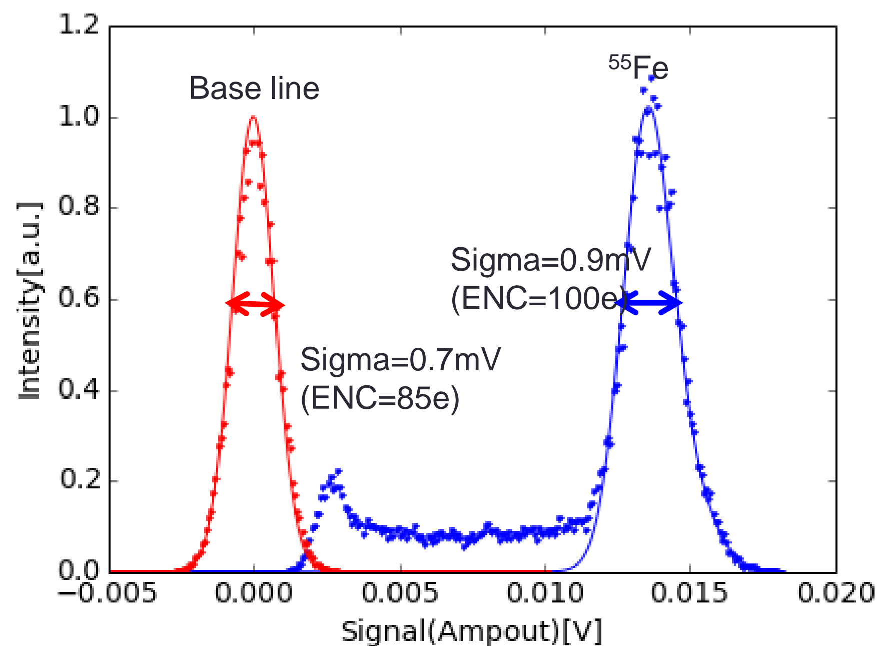
Version A

Bias: -110V (4nA)
Pixel: [6,10] CSA ELT
Global DACs: default except VN=12
Source: ^{55}Fe
Signal: Ampout

Version B

Bias:20V (39nA)
Pixel: [14,14] HV connection Diode, CSA ELT, PSUB everywhere
Global DACs: default
Source: ^{55}Fe
Signal: Ampout





Conclusions and future plans

- HVCMOS pixel prototypes produced in 8 different technologies. We have the choice…
- Most advanced CCPD test beam results in AMS 180 nm technologies results 99.7% efficiency before radiations.
  The CCPD_AMS_V4 chip is still alive after radiations up to 1Grads.
  Timing to be improved (lower thresholds, higher signals with HR, time slewing corrections).
- Very promising results with the LFoundry technology.
- TCAD simulation, a very good help addressed to the HVCMOS project. Thanks for the Jian Lu (CPPM/SDU) contribution and work through his Co-PhD.
- CMOS Demonstrator program started with the goal to produce 2-3 demonstrator types for test beam in the fall of 2015.
- The IHEP and CPPM have a very strong collaboration since many years, on ATLAS developments. We are expanding the partnership between Chinese institutes and CPPM on HVCMOS development by adding the SMIC foundry for the evaluation and testing.

BACKUP

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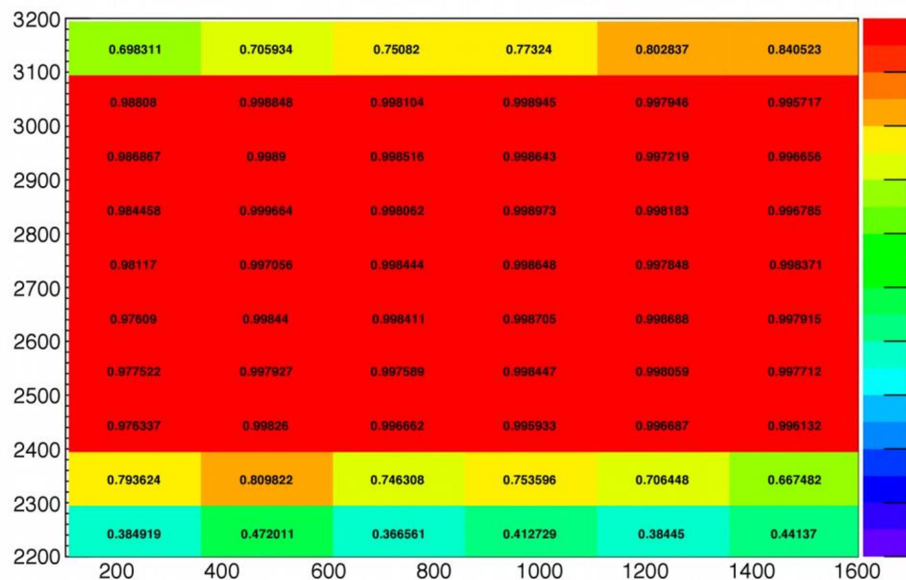
CPIX Demonstrator Design issues

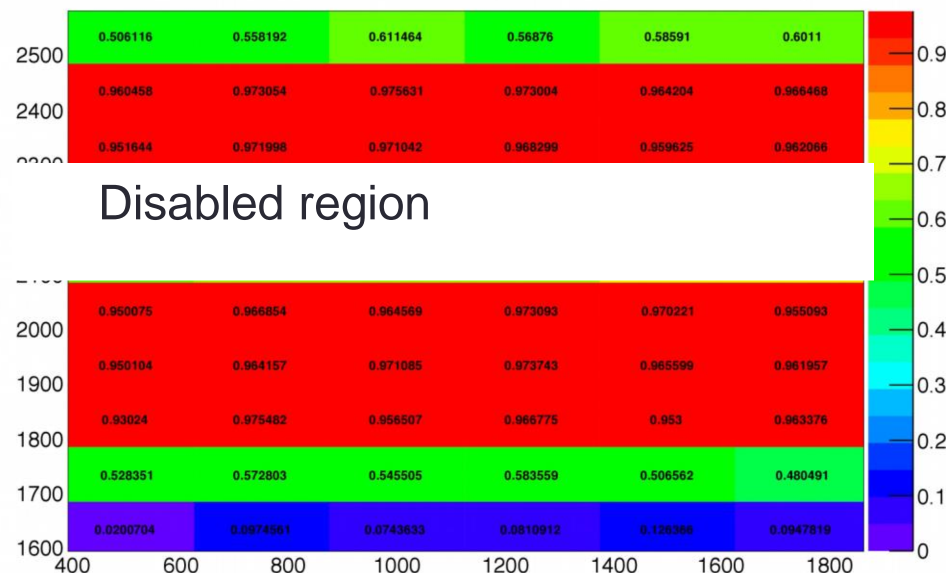
- Minimize input capacitance to amplifier to reduce noise: critical for HV as signal low, many transistors (complex architecture) increase significantly the capacitance
- Homogeneous charge collection to avoid zones with low efficiency
- Fast amplifier/discriminator and time slewing corrections to reach one BC readout
- Enough shielding/field shaping with 3-4 deep implants offered in the technology
- Compromise on the depletion depth: small is good for radiation hardness and cluster size, bigger is needed for efficiency and reduced time slewing => 15-100 μm range $d \sim \sqrt{(\rho V)}$
- Radiation tolerance (for example circular transistors in critical places, high fill factor of collecting electrode etc.)
- Coupling to FE-I4: gluing or SnAg bumps to be evaluated

Test beam efficiency CCPD-AMS_V4

- Non-irradiated
- HV=-12V
- Vth=0.84V
- Efficiency=99.7%

- Neutron irradiated 10^{15} neqcm^{-2}
- HV=-30V
- Vth=0.84V
- Efficiency=96.2%



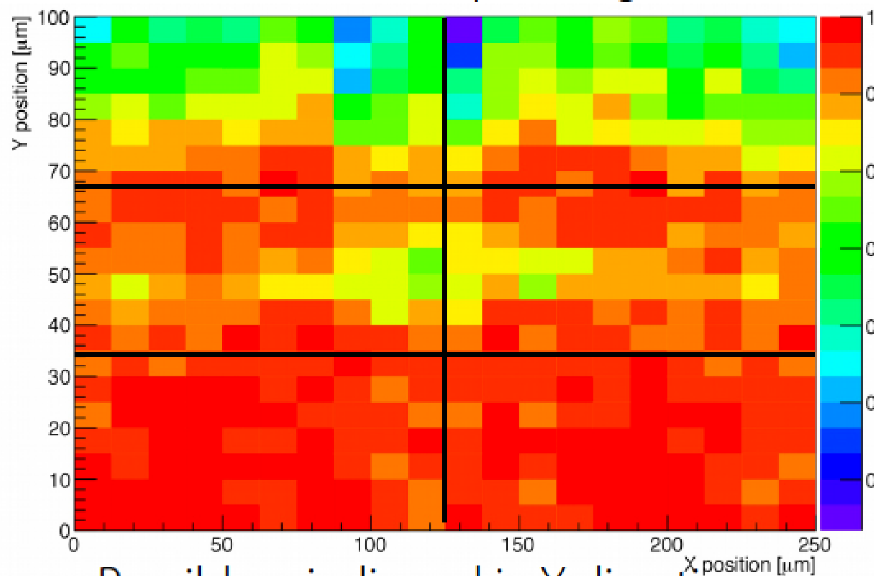


In pixel efficiency CCPD-AMS_V4

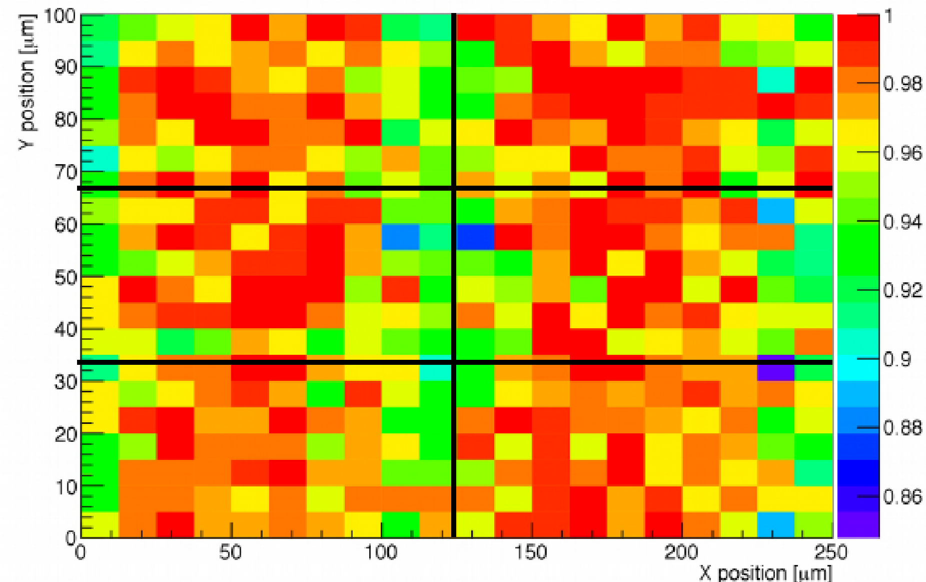
- Non-irradiated
- HV=-12V
- Vth=0.84V
- Efficiency=99.7%
- Efficiency close to specification

- Neutron irradiated 10^{15} neqcm^{-2}
- HV=-30V
- Vth=0.84V
- Efficiency=96.2%
- Inter-pixel regions to be optimized to increase efficiency

- Inefficiencies in inter-pixel regions

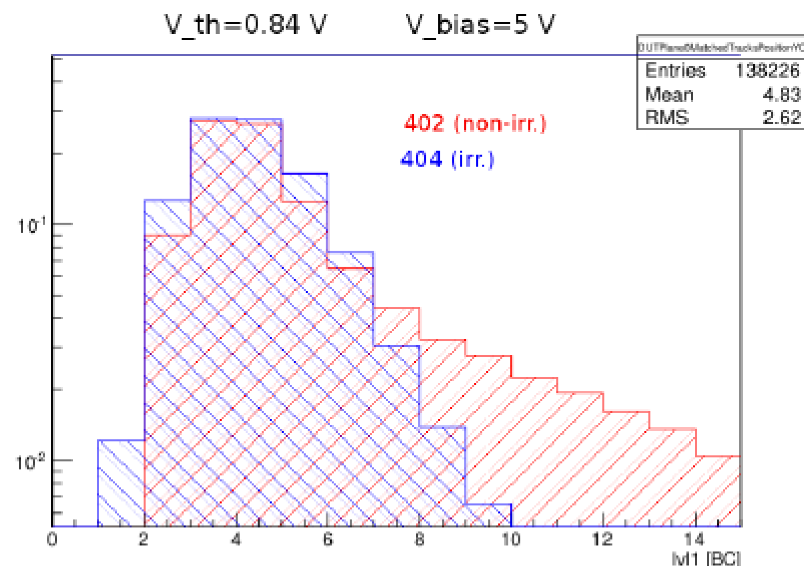


- Possibly misaligned in Y direction

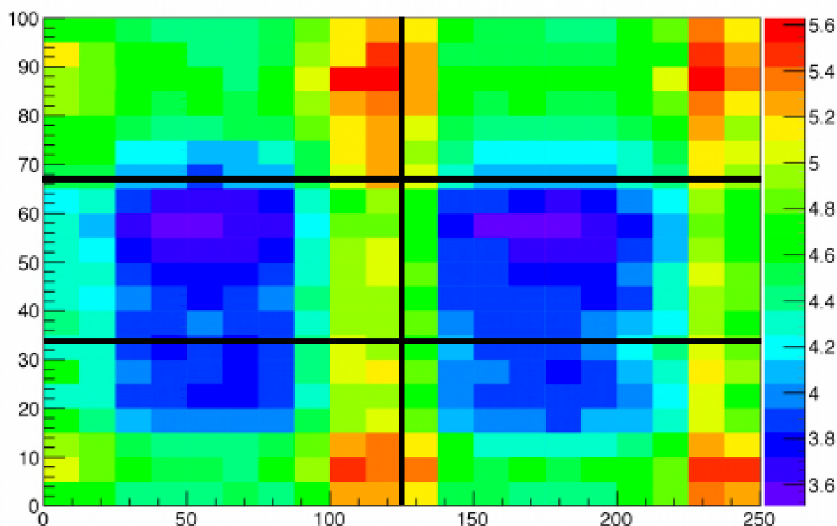


In-Pixel Timing CCPD-AMS_V4

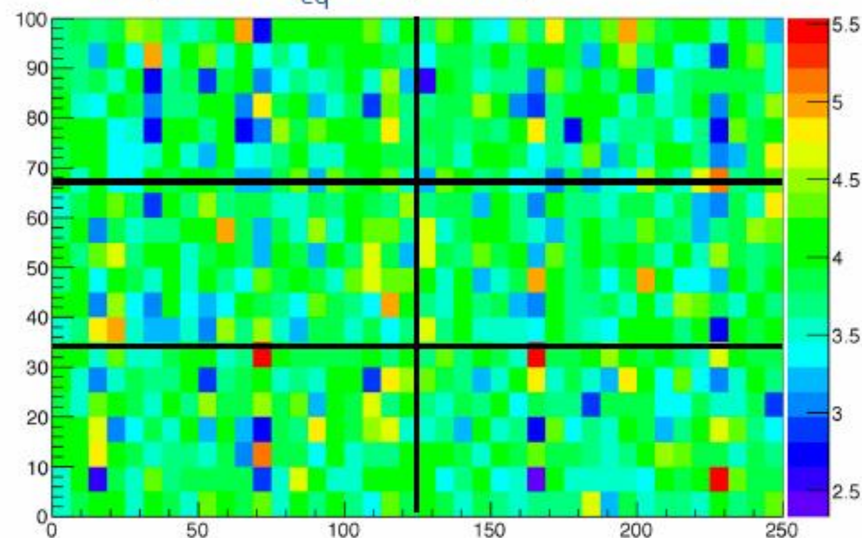
- Spatial dependence of timing disappears after irradiation due to the killing of diffusion
- Time width of 5 BC is still far from specification. In future: smaller thresholds, HR increase of signal and time slewing corrections



402 (unirradiated, -12V)



404 ($1x10^{15}n_{eq}cm^{-2}$, -30V)



CMOS demonstrator time-walk

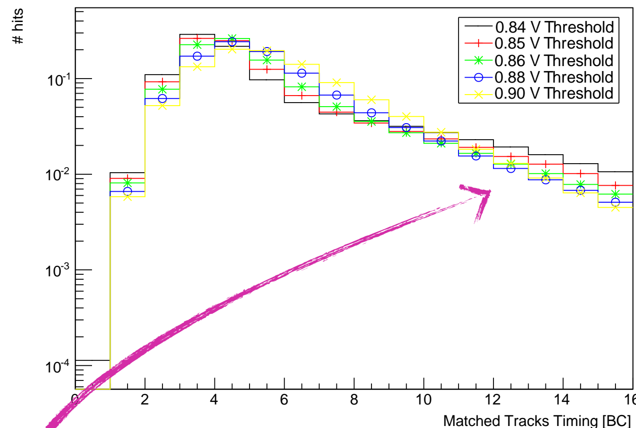
- Specification to 1 BC efficiency
- Present AMS 180nm prototypes ~ 5BC
- How to improve ?
- Fast amplifiers (price of high consumption)
- Higher signal (price by HR, thicker depletion region)
- Ttime-slewing compensation circuits (price more complicated circuits: higher capacitance-noise, space)
- Lower thresholds (price of potential noise problems and difficult tuning for low threshold)

BCID distributions AMS 180 nm

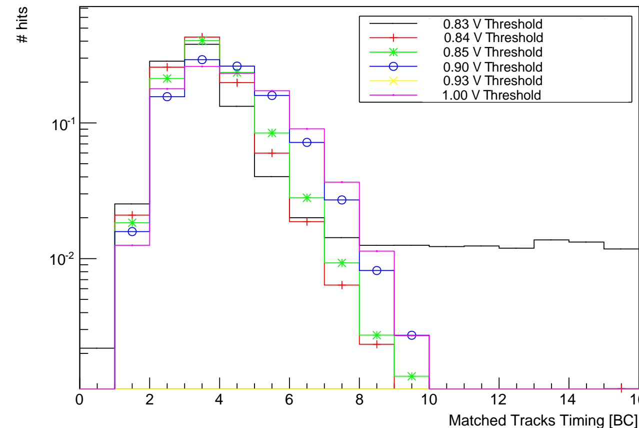
- sample CCPD-AMS_V4 sn404, bias -30V, 10^{15} neq/cm^2

v4 Timing vs Threshold.

402, unIrradiated
Th 0.84 V



404, 10^{15} n_{eq}/cm^2, Bias 30 V



Low threshold show smaller tails, indication of a time-walk effect.
High threshold reduces the diffusion contribution (low Amplitude).

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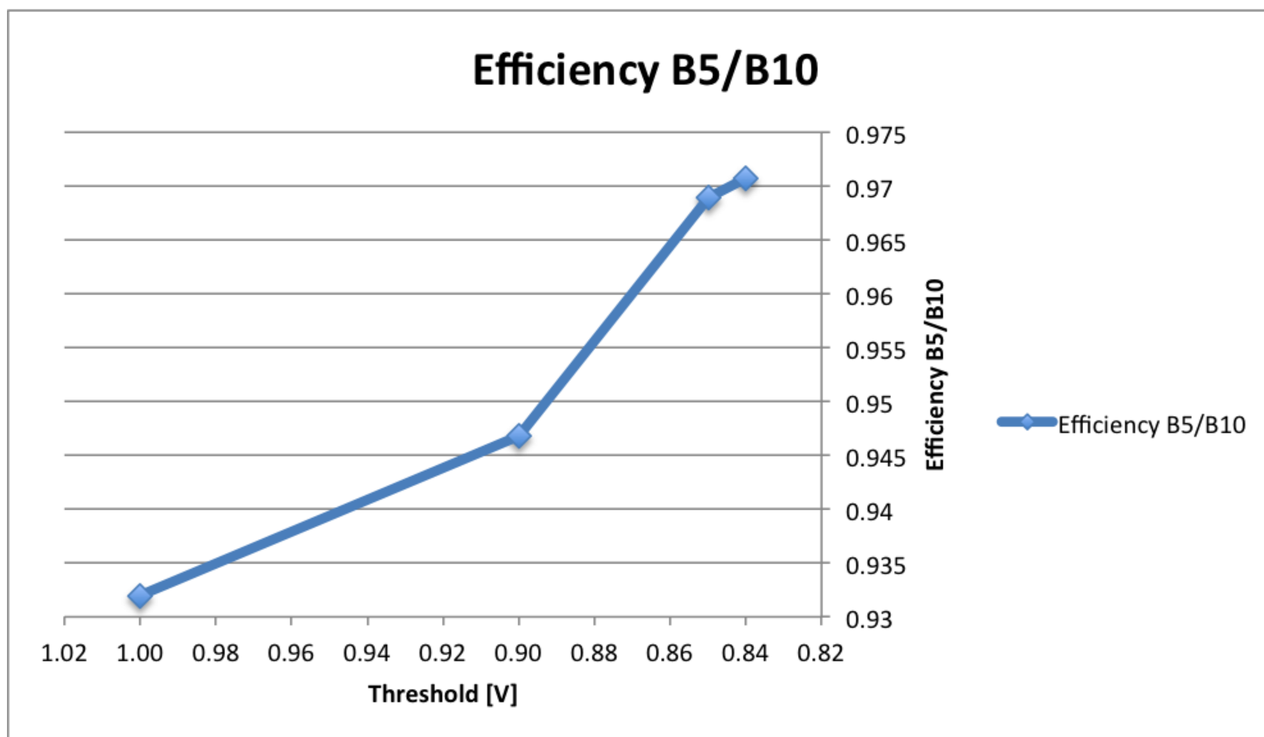
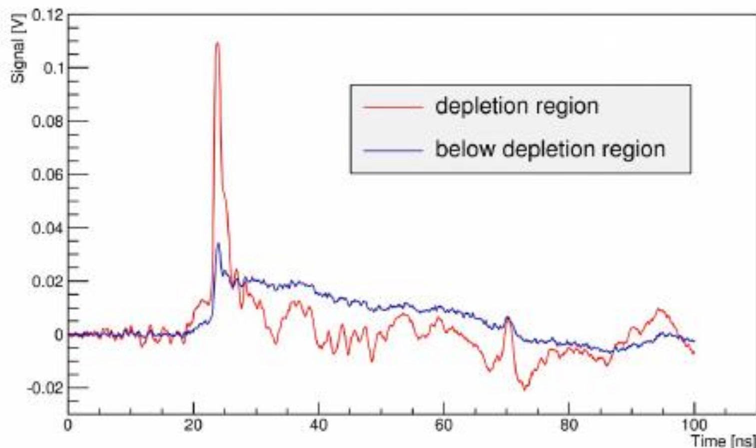
Time-slewing vs Threshold

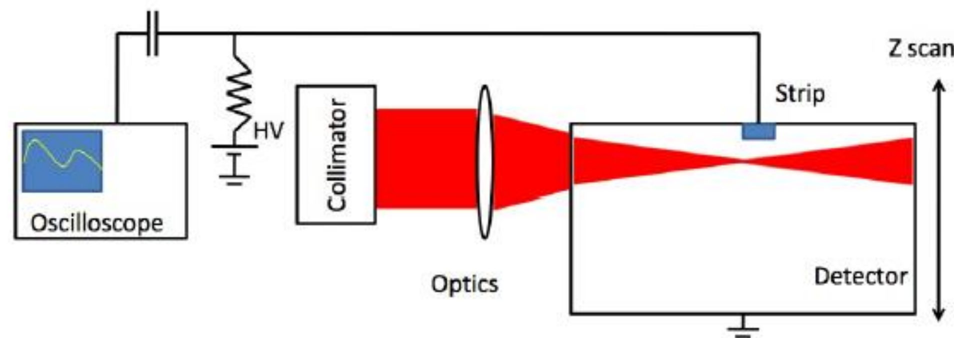
- In time efficiency (B5/B10) improves with low threshold (except very low where noise start to dominate the tails)
- So for AMS 180 design time-slewing is smaller for low threshold



Edge TCT results on depletion zone

- Measure charge from special 100x100 um diode on the edge
- Clearly see timing difference between depleted and diffusion regions





U_{bias} [V]

t<2.5ns

t>2.5ns

~20µm

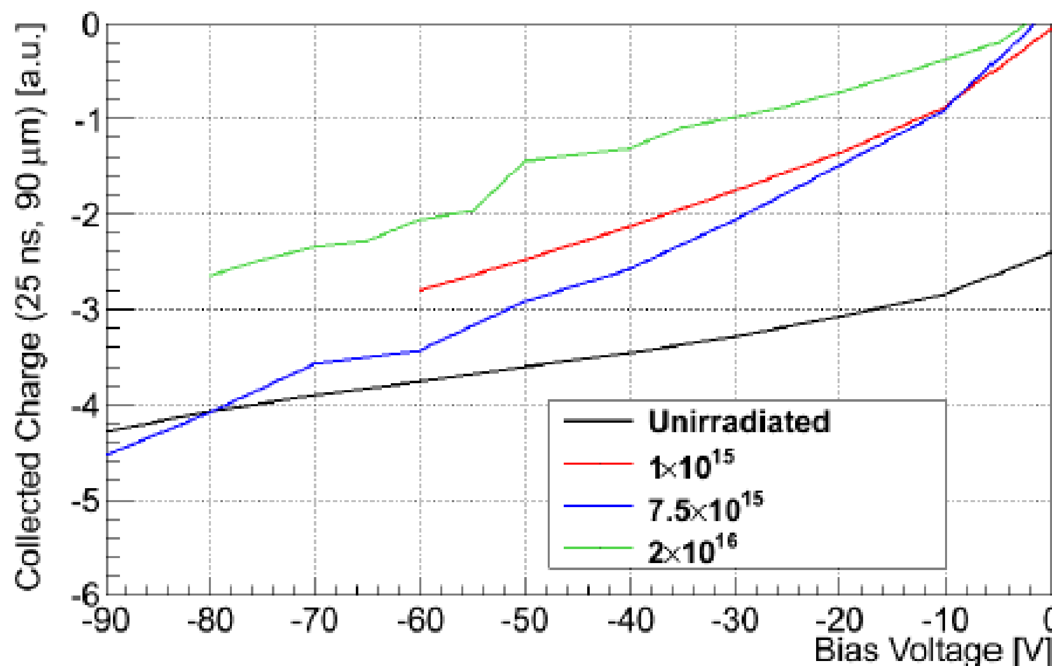
-z [mm]

x [mm]

Collected charge [a.u.]

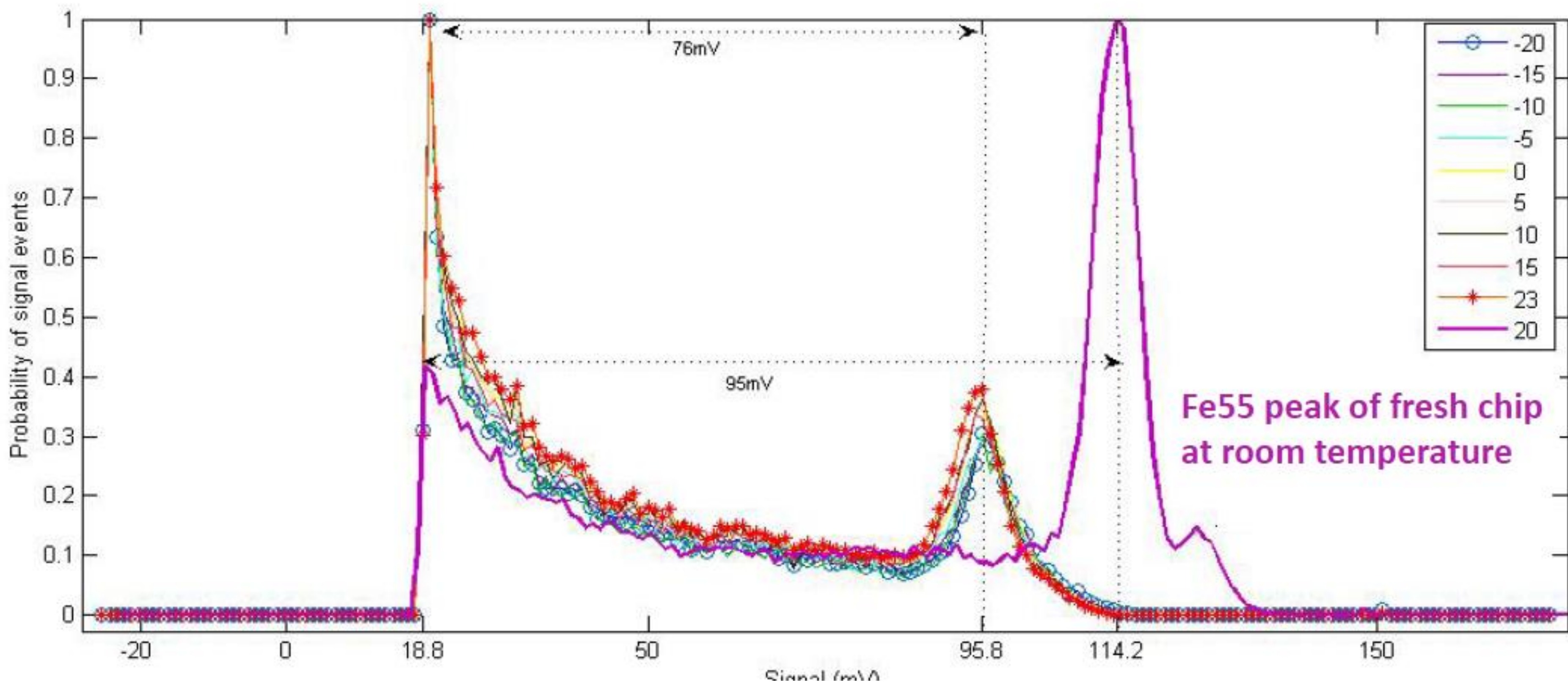
High dose Edge TCT measurements

- 7.5 10^{15} neqcm^{-2} sample deliver higher signal at -90V than non-irradiated sample. Probably acceptor removal effect.
- Would it be the same for proton irradiation ?
- Would it be the same for HR substrate ?



AMS 350 nm chip

- CAPSENSE chip with 55x55 um pixels
- To be glued on CAPIX readout chip
- Irradiated at KIT with protons 10^{14} neqcm^{-2}



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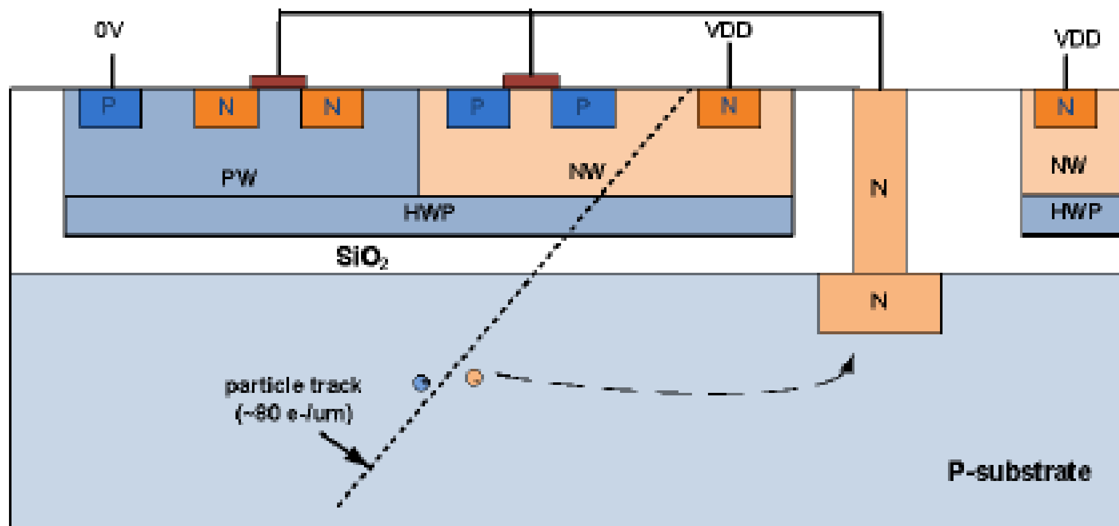
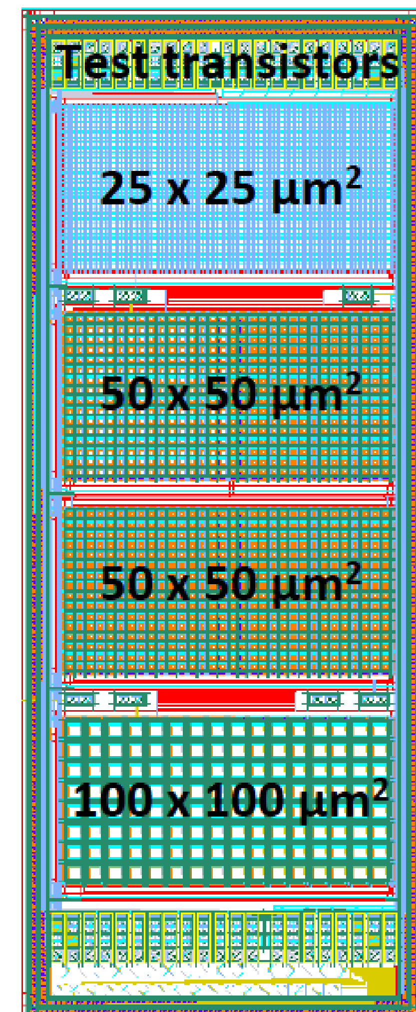
XFAB SOI 180 nm prototype

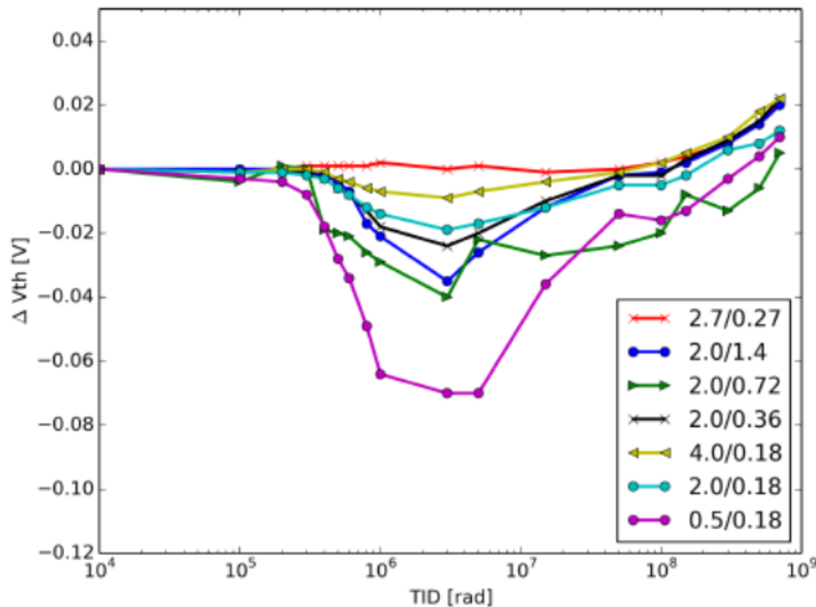
- Small charge collecting well (to be extended by design rule violation)
- Full CMOS , isolation via deep p-well +BOX
- HV technology + HR substrate
- Wafer 100 ohm cm
- No backside implant

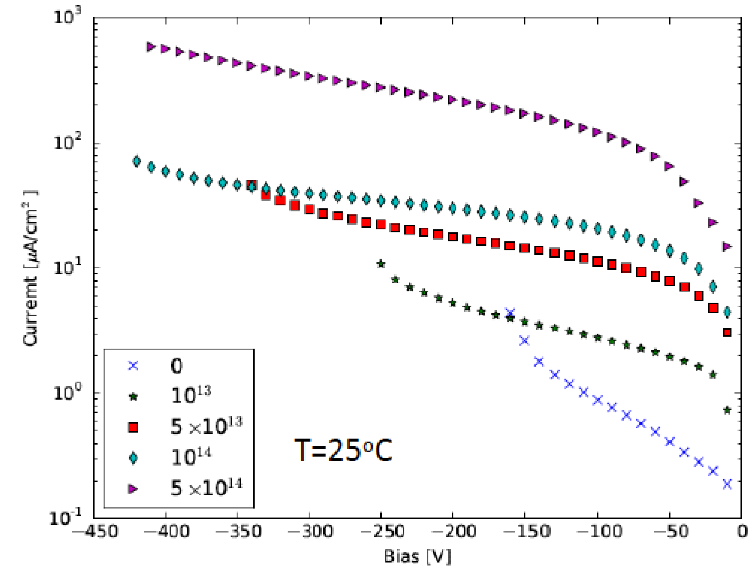




XFAB SOI 180 nm irradiation

- Test transistors irradiated up to 700 MRads X-ray, radiation hardness as for non-SOI CMOS
- High leakage current after neutron and X-ray irradiation due to surface current, can be corrected in future by process change





XFAB source and test beam spectra

- Spectra of Fe55 and Sr90 measured after 5 1014 neqcm-2 . Better for high fill factor in 25 um pixels.
- Test beam MIP Landau measured