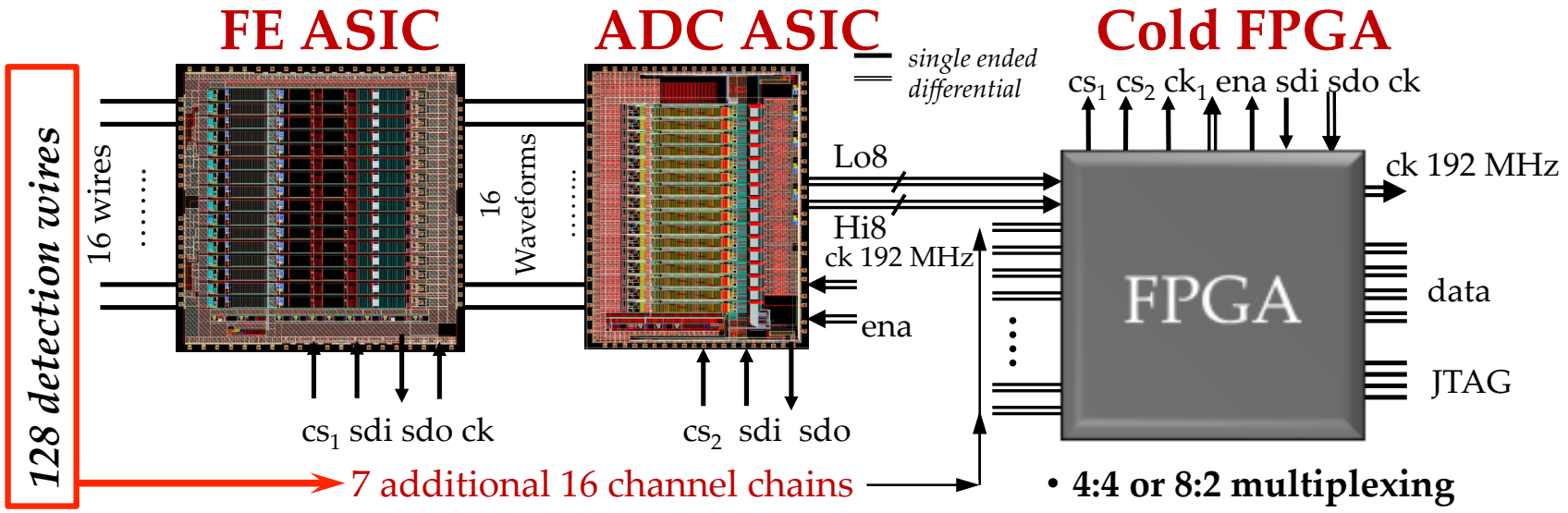
# Readout Electronics for LArTPC

NOVEMBER 6TH, 2014

# Outline

- TPC Front End
- Light Collection Front End
- Back End
- Signal Feed-through

# TPC Front End Cold Electronics

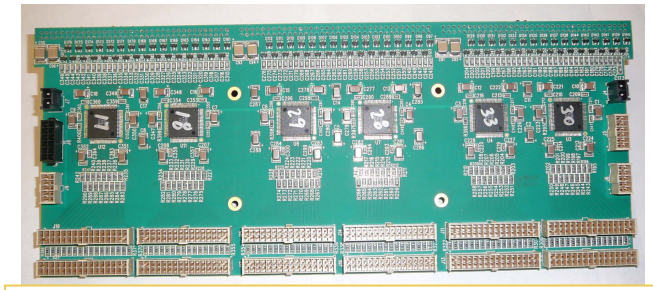



- low-noise analog amplification
- programmable gain, shaping, coupling, …
- charge calibration over all chips, channels and temperatures to 1%

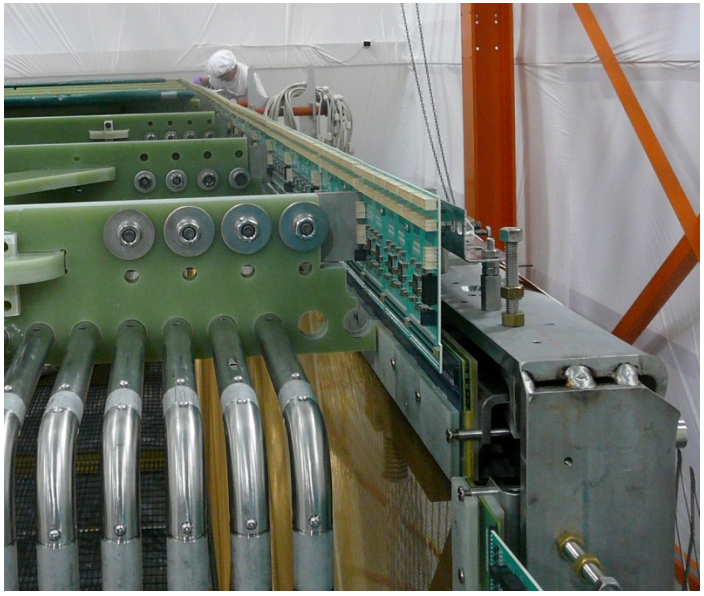
- ADC 12-bit 2MS/s sampling rate
- built-in FIFO
- serialized outputs
- 2 x **8:1 multiplexing**

- **4:4 or 8:2 multiplexing** (total 32:4 or 64:2)
- timestamp
- compression
- zero suppression
- neighbor triggering
- ***support non-reduction transparent mode***
- ***max output data rate 960Mbit/s or 1.92Gbit/s with overhead of 8B/10B***

# FE ASIC

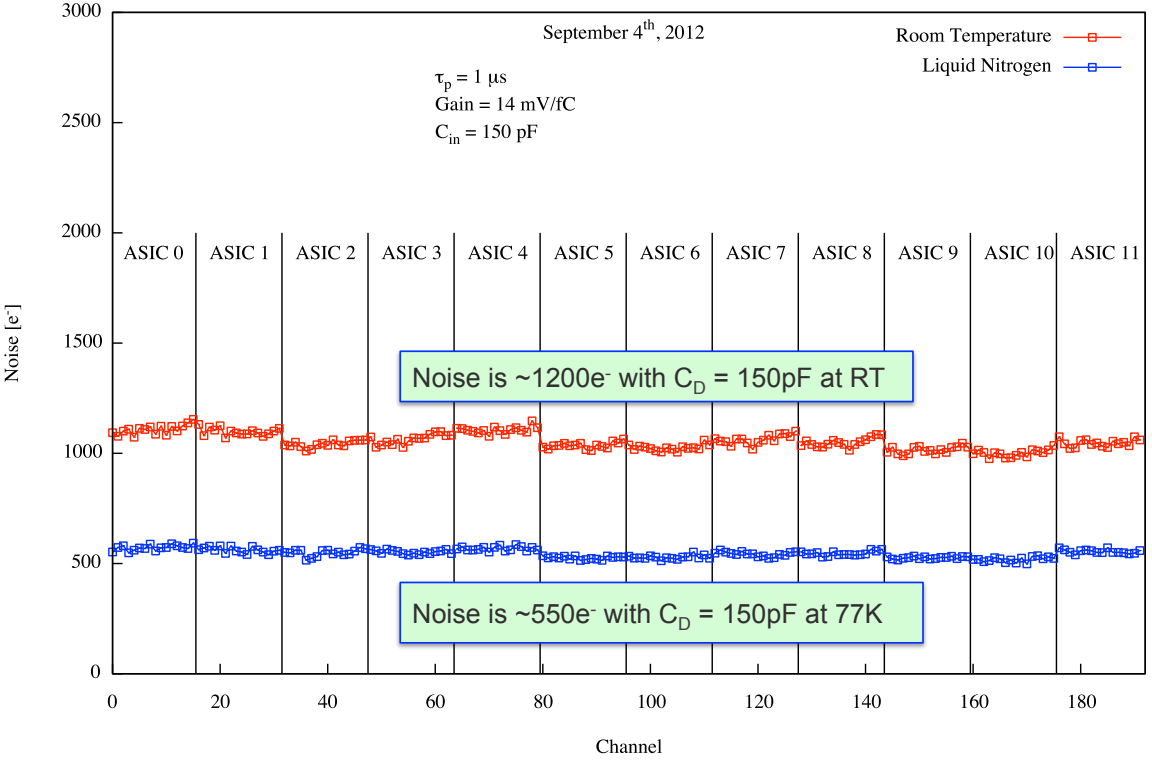


MicroBooNE cold mother board with 12 analog FE ASICs (192 channels)



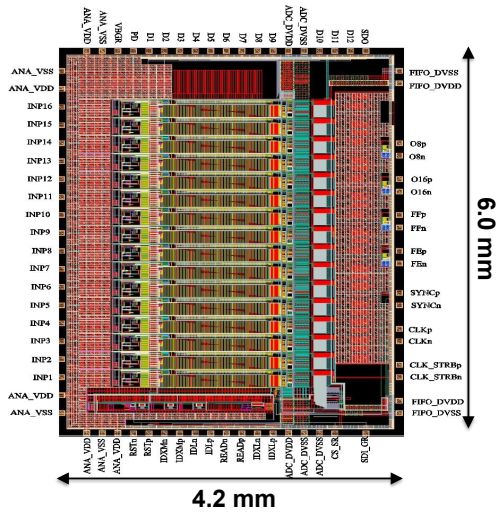
**50 cold mother boards (8,256 channels)** are installed on MicroBooNE TPC

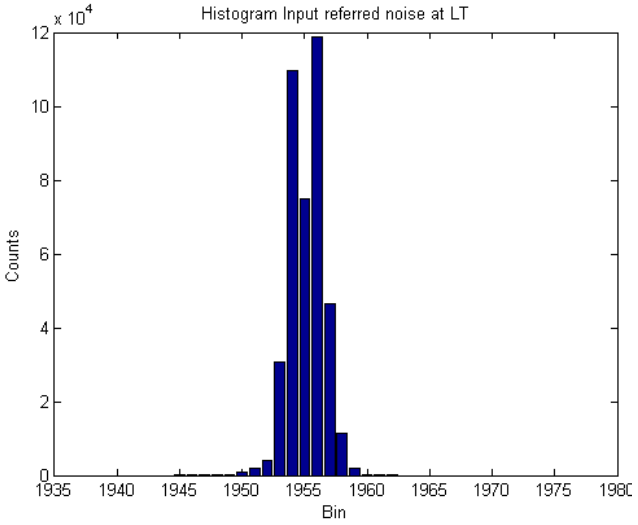
## Noise *vs.* Temperature: 12 ASICs (192 channels)

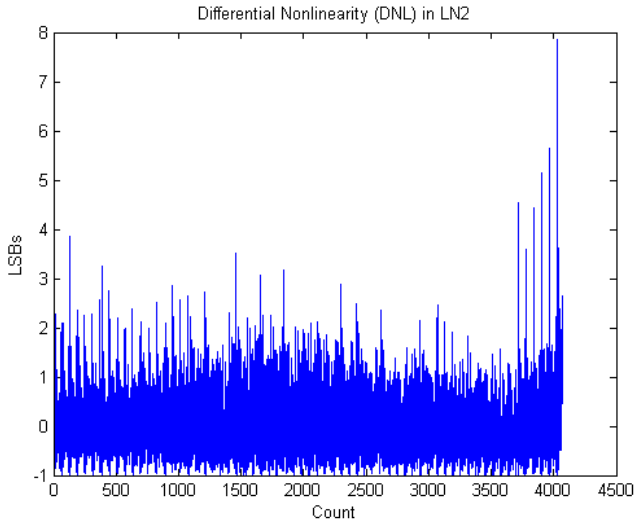


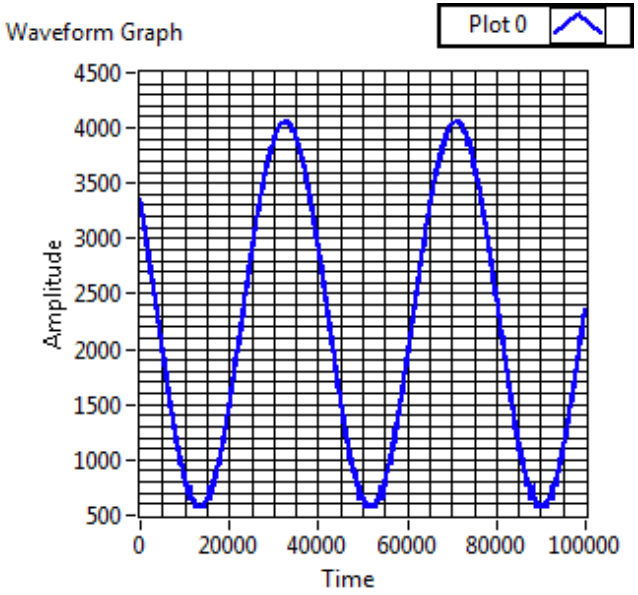

- 16-channel FE ASIC with programmable gain and peaking time
- Low power consumption ~ 6 mW/ch without buffer
- FE ASIC is ready to use for TPC readout
  - ***Plan to revise the design to include build-in pulse generator***

# ADC ASIC



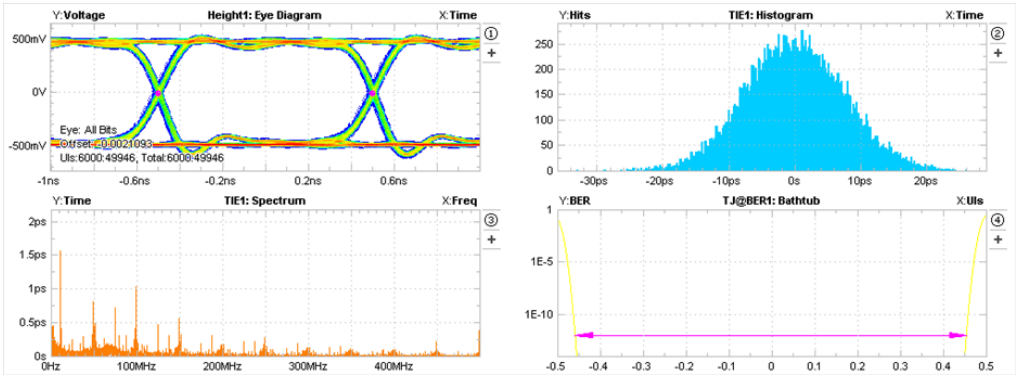



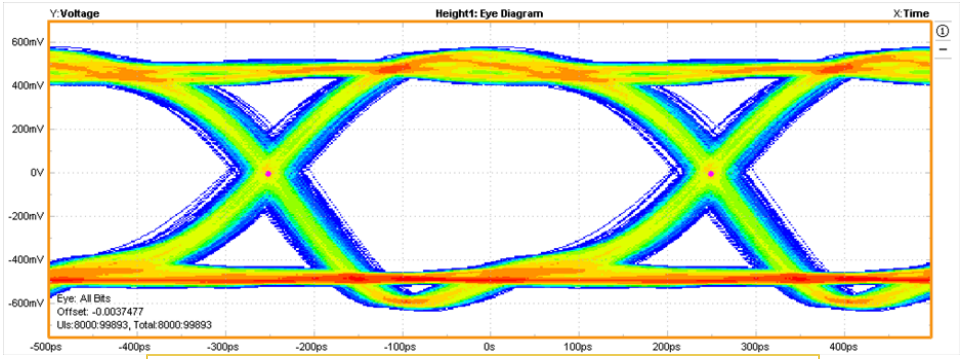




- 16-channel ADC with built-in FIFO
- Low power consumption < 5 mW/ch
  - ADC ~ 4.8 mW/ch and FIFO ~ 1 mW for 16 channels
- Very good results have been obtained from prototype design
  - Effective resolution w.r.t. input referred noise is ~11.6 bits at both 300 K and 77 K
  - Differential non-linearity (DNL) is less than 4 LSBs for 99% ADC bins at both 300 K and 77 K
- ADC ASIC is ready to use for TPC readout
  - ***Plan to revise the design to include default power on configuration***

# Cold FPGA



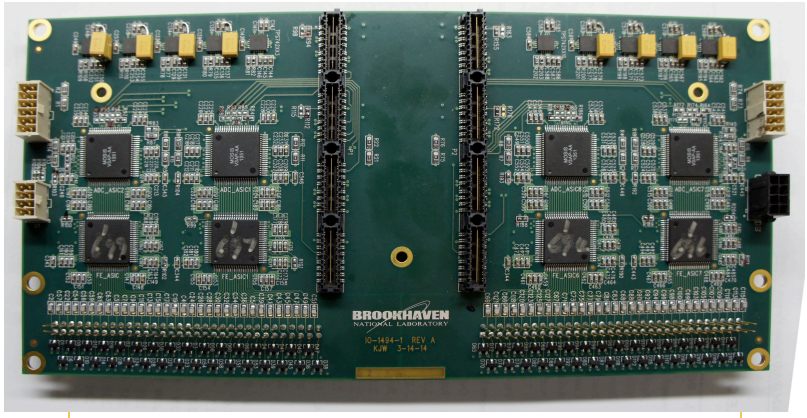

Measurement plots @ 1 Gb/s



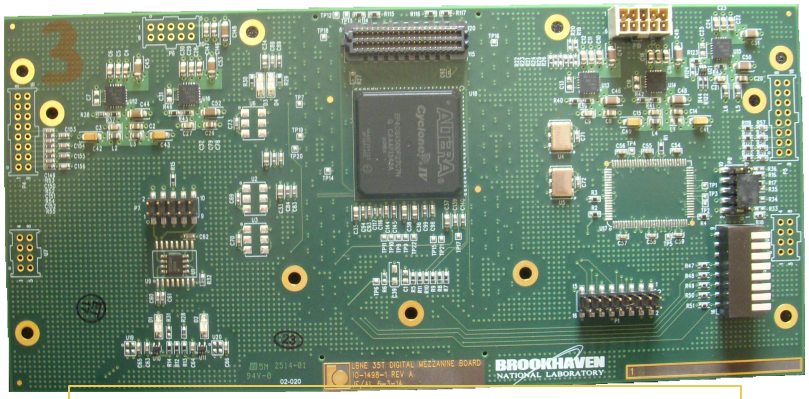

Eye diagram @ 2 Gb/s

- Test of Cyclone IV GX Transceiver Starter Board in $LN_2$
  - ***Transceiver works well at both 1Gbit/s and 2Gbit/s***
  - Height
    - 839mV @ 1Gbit/s
    - 823mV @ 2Gbit/s
  - Eye Width
    - 914ps @ 1Gbit/s
    - 357ps @ 2Gbit/s
  - ***On board SRAM works with BIST***
    - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
    - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

# Front End Mother Board for 35 Ton




Analog Mother Board



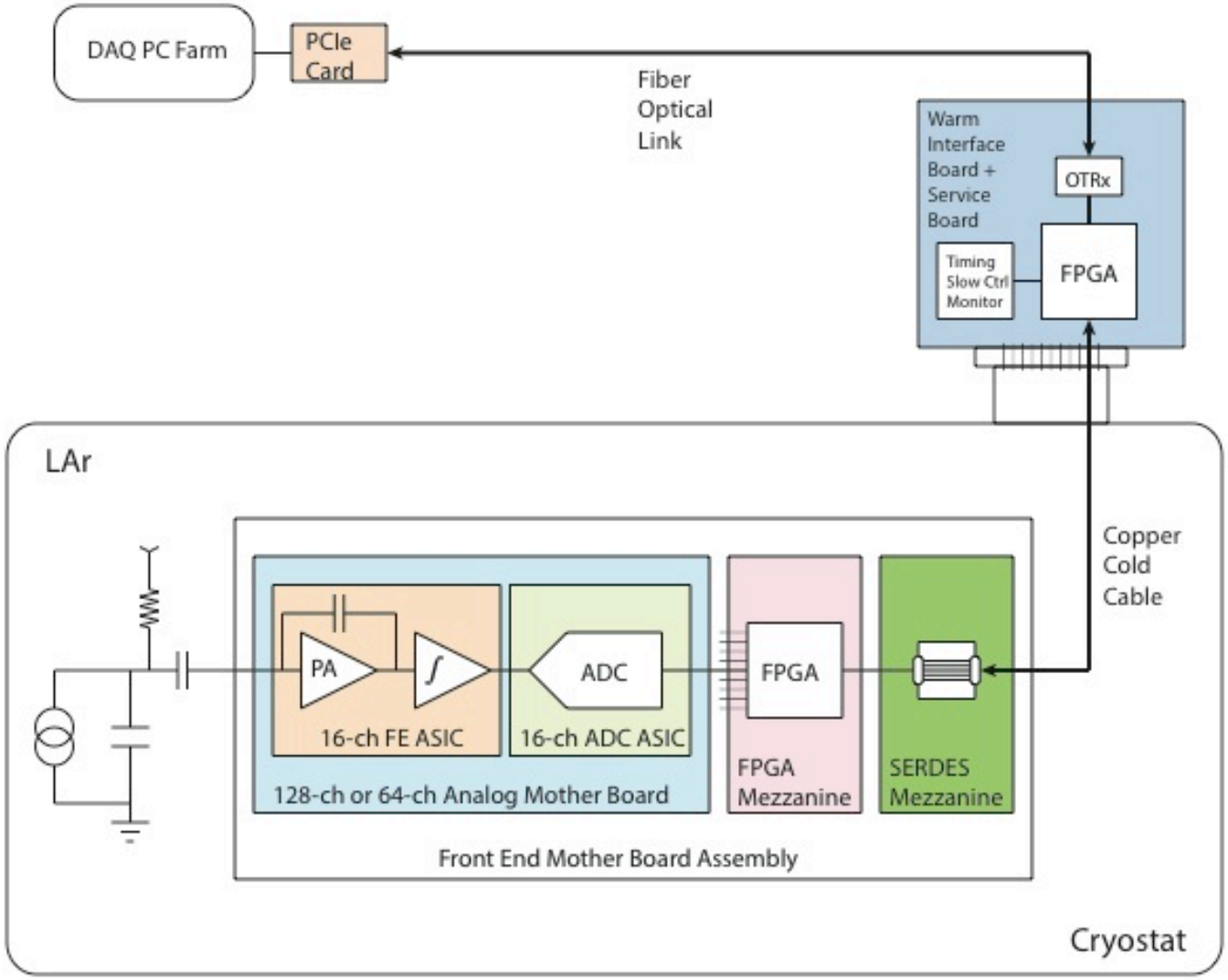

FPGA Mezzanine

- 128 channels
- 8 Analog FE ASICs
- 8 ADC ASICs
- Altera Cyclone IV GX FPGA
- Voltage regulator
  - TI TPS74201: 1.5A, adjustable output (0.8V to 3.6V)
- ***Front End Mother Board could be revised for TPC anode design***

# Light Collection Front End

- BNL is working on the R&D of low noise cryogenic front end for SiPM readout of nEXO experiment
  - 16 channel front end ASIC, ~500 chips, 40 W
    - Preamplifier and shaper
    - Peaking time: 250 ns – 1 us
  - Peak/hold and timing flag
    - Timing at peak of shaped pulse (~10 ns res.)
    - Timing flag width 10 ns – 50 ns
    - Peak/hold autoreset 1 – 10 us
  - Coincidence logic on flag
    - Coincidence window 50 – 200 ns
    - Coincidence number 1 – 8
    - Adjustable output flag width
    - Channel mask
  - Digitization, control logics and DAQ is in the warm
- Could be applicable to LArTPC light collection readout

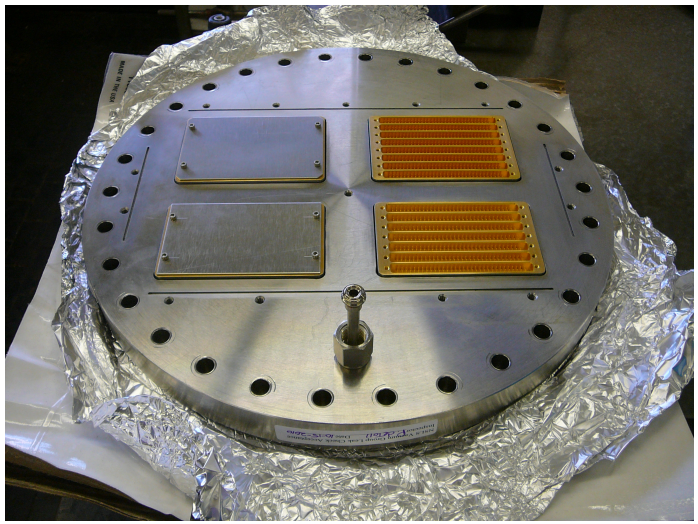
# Back End

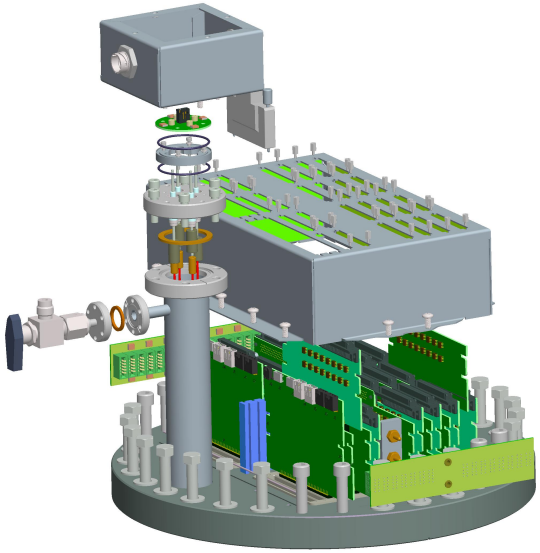

DAQ PC Farm
PCIe Card
Fiber Optical Link
Warm Interface Board + Service Board
OTRx
Timing Slow Ctrl Monitor
FPGA
LAr
Copper Cold Cable
PA
ADC
16-ch FE ASIC
16-ch ADC ASIC
FPGA
FPGA Mezzanine
SERDES Mezzanine
128-ch or 64-ch Analog Mother Board
Front End Mother Board Assembly
Cryostat

# Back End

- Warm interface electronics
  - Warm interface board is to receive serial data from TPC front end and send to DAQ system
  - Service board is to provide power distribution, timing, slow control and monitoring
  - Both will be developed for LAr1-ND
- A PCIe Gen3 x8 card is being developed for ATLAS Phase-I upgrade
  - Virtex-7 FPGA is the core processor
  - 48-ch optical transceivers running at 10 Gb/s per channel
  - DDR3 on board memory for event buffer
  - Receiving data from, and distributing timing, trigger and control information to the front end

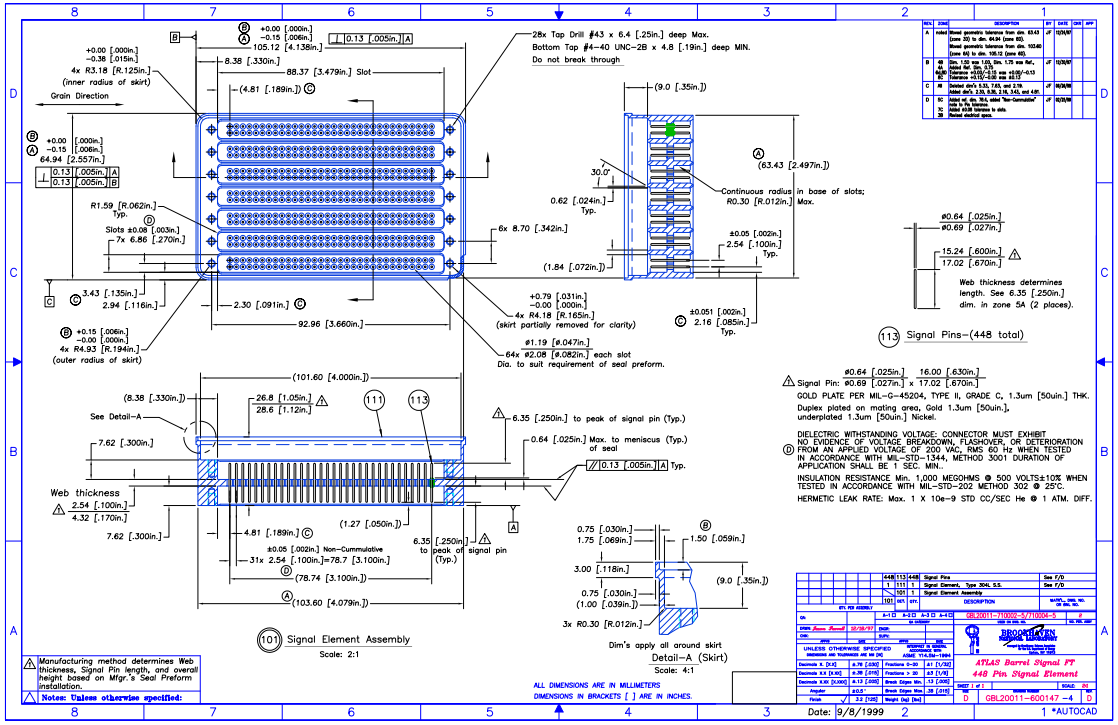
# Signal Feed-through





- ATLAS LAr Calorimeter Feed-through
  - Pin carrier weled on flange: 100% hermetic
  - 2x8 + 2x7 rows pin carrier: high signal density 1920-pin/FT
  - Designed for both warm and cold flanges
- MicroBooNE adopted same pin carrier design for 11 warm signal feed-throughs
- Technology exist: no development required
- Pin carrier has been tested to be capable of running at 2 Gb/s

# Signal Feed-through




- Original manufacture Glasseal, part of AMETEK HCC Industries Inc., has been contacted
  - Quote is available, ~$5k per pin carrier for small quantity of order