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BRUNO KESSLER

Development of a new technology for the next generation of 3D Pixel Sensors for HL-LHC within the INFN (ATLAS-CMS) R&D program in collaboration with FBK

Sabina Ronchin

Introduction

A lot of experiments require thin detectors, but are thin 3D feasible?

- Key point:

Too thin (or thinned) 6-inch wafers are not suitable to process

from double sided process to **single side process** on **“special” wafers**...

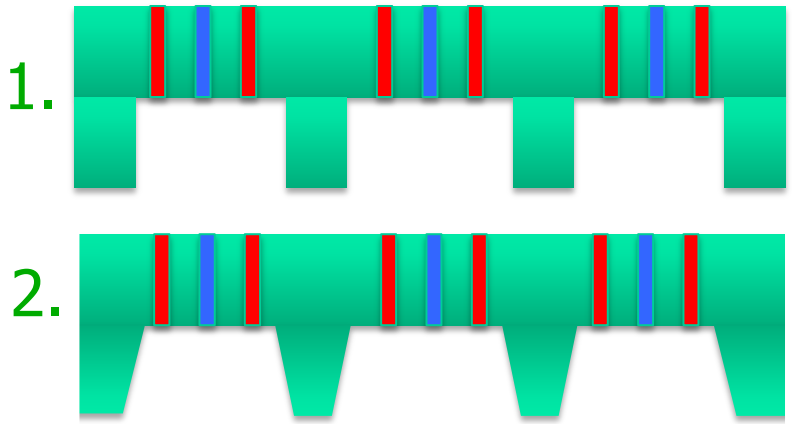
Are thin 3D feasible ?

Two possible technological approaches

Local thinning

- Single side
- Processing thicker wafers with local thinning of sensor active areas by DRIE (1) or TMAH (2) could be done

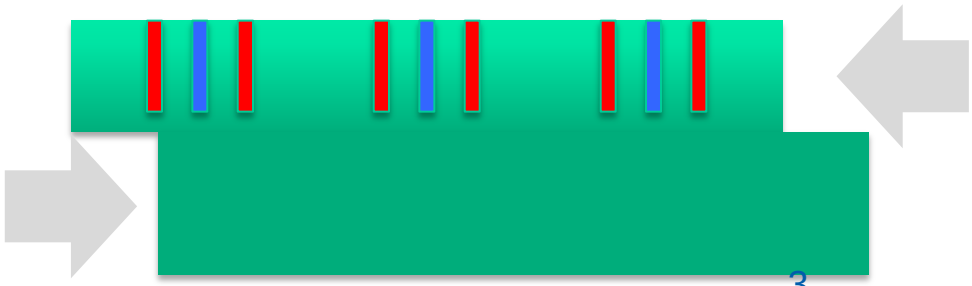
G. Pellegrini et al., NIMA 604 (2009) 115



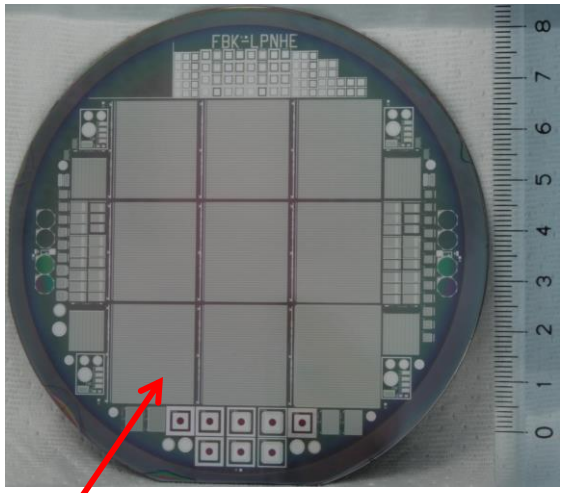
Back end process:

thinning the processed wafers

- Single side
- "special" wafers: Epi, SOI, Si-Si…
- After bump

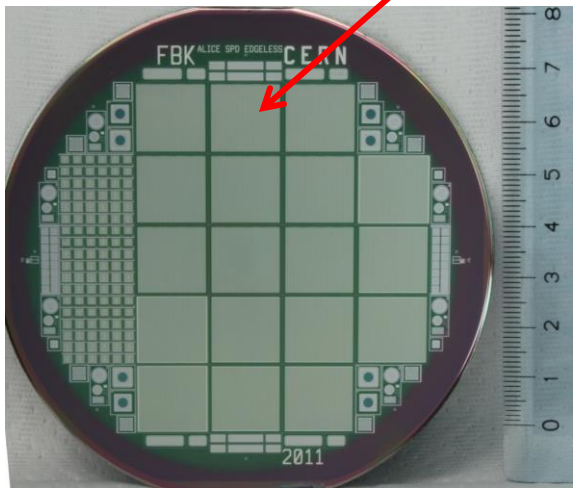


FBK past experience on back end process: edgless technology

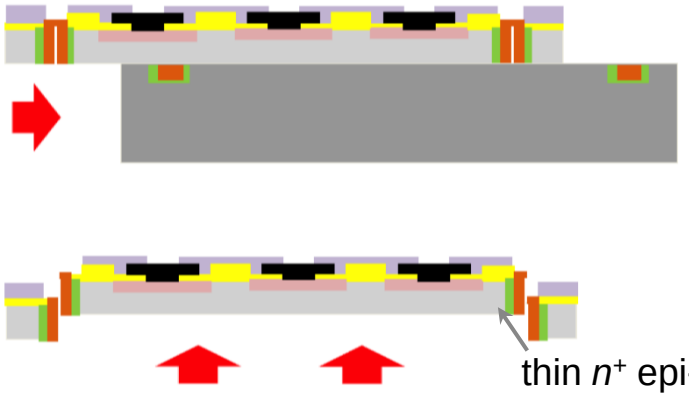


SOI (200um Fz)
ATLAS

Epi
PANDA
ALICE

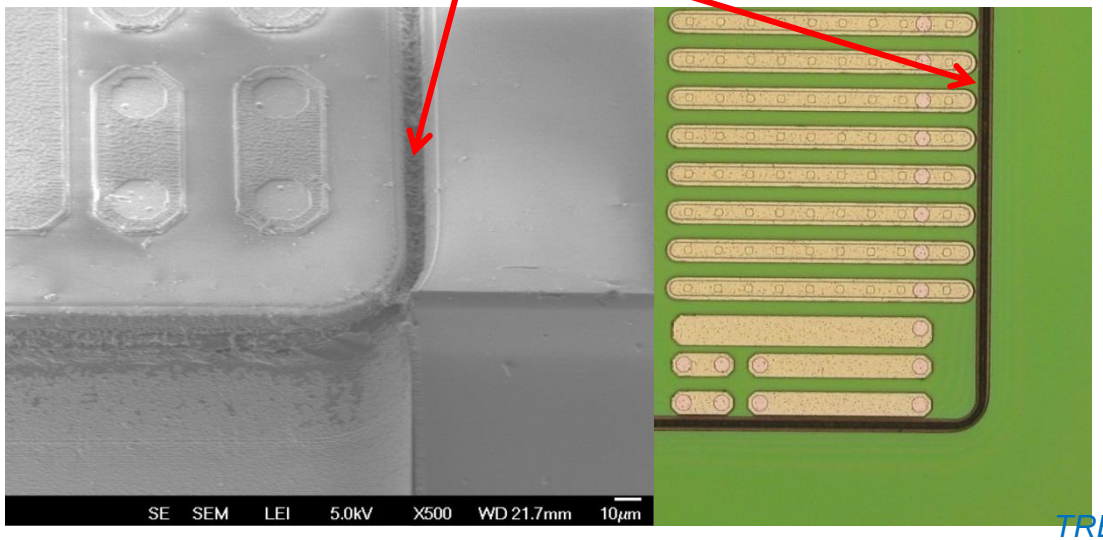


Substrate thinning (by IZM)



Device separation along the trenches

Trench filled with polisilicon



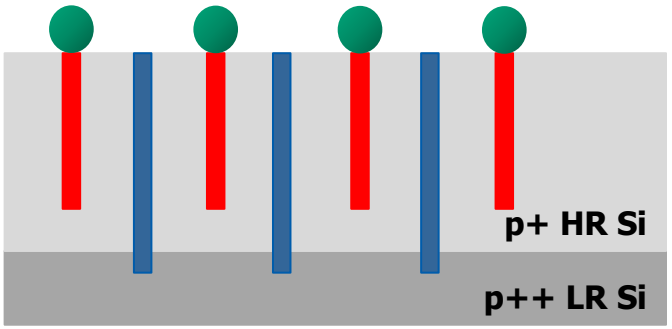
Thin Si3D: proposed fabrication approach

Thin silicon HR-p-type active layer (100-150 μm)

Ohmic columns depth > device wafers

Junction columns depth < device wafers

Compatible with edgless



Single side process with support wafer

Most critical issues

1. Identify the "best" row material
   - We need a "processable" thin silicon substrate (100-150 μm)

2. Controls of the hole depth
   - Optimization of DRIE process

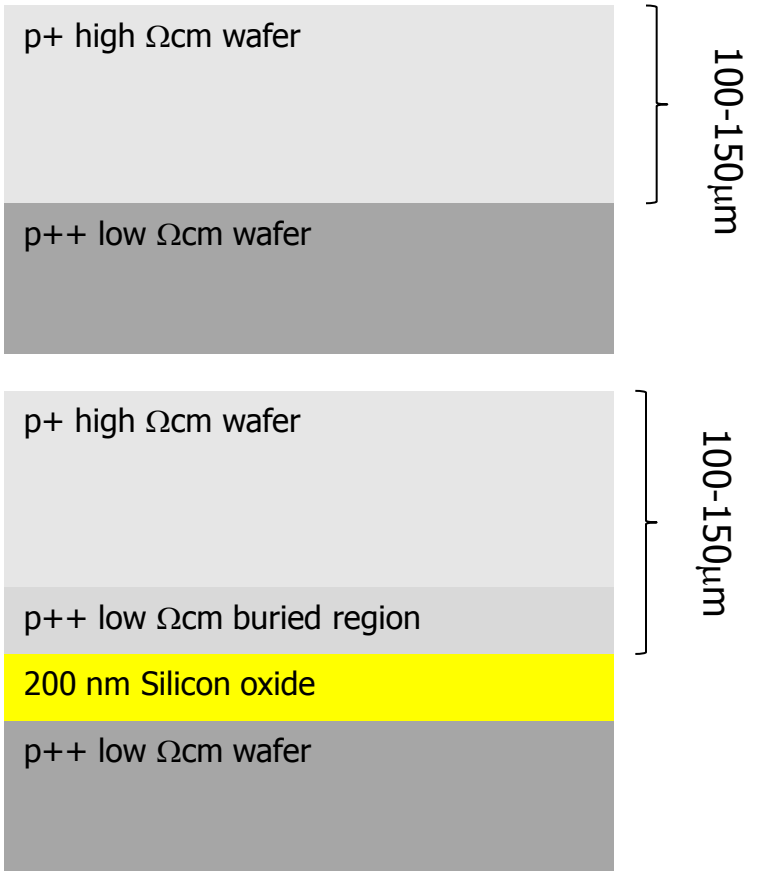
3. Doped Polysilicon Filling
   - Hole must be filled or partially filled

4. Two DRIE on the same wafer side

5. Deep SiO_2 etching

1. Identify the “best” row material

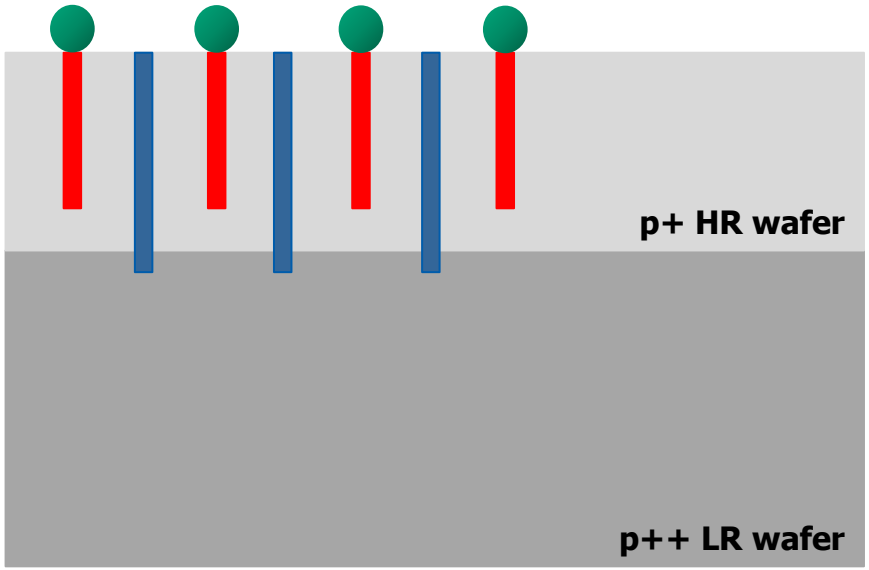
Thin silicon with support wafer



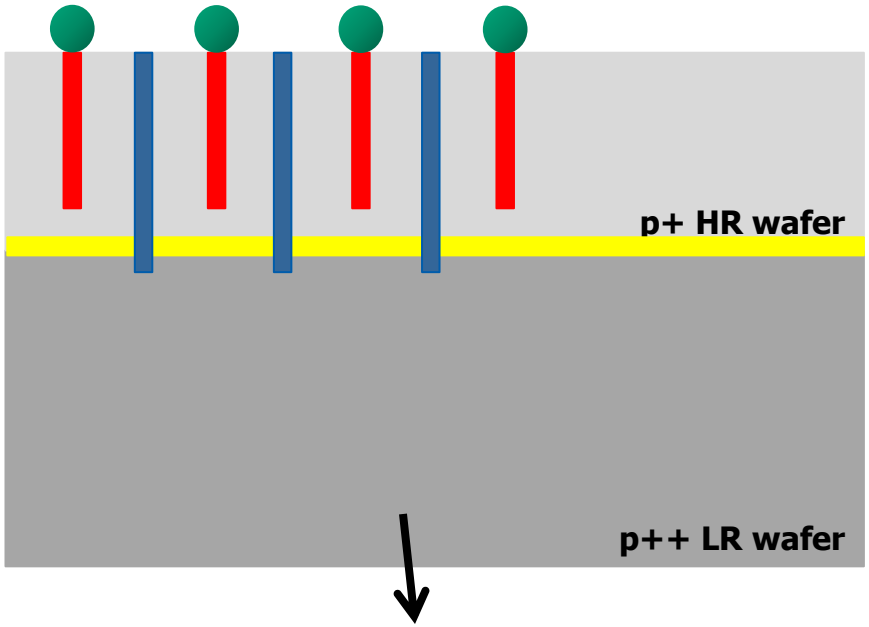
- Two possibilities:
  a) Epi or Si-Si
  b) SOI
- Under bump metallization
- Support wafer thinning (removal)
- back-side metal deposition

Thin Si3D: the two technological options

Epi or Si-Si wafer



SOI wafer



Ohmic columns must be passing through the bonding oxide

Planar test run on Si-Si to test available wafers

Wafers

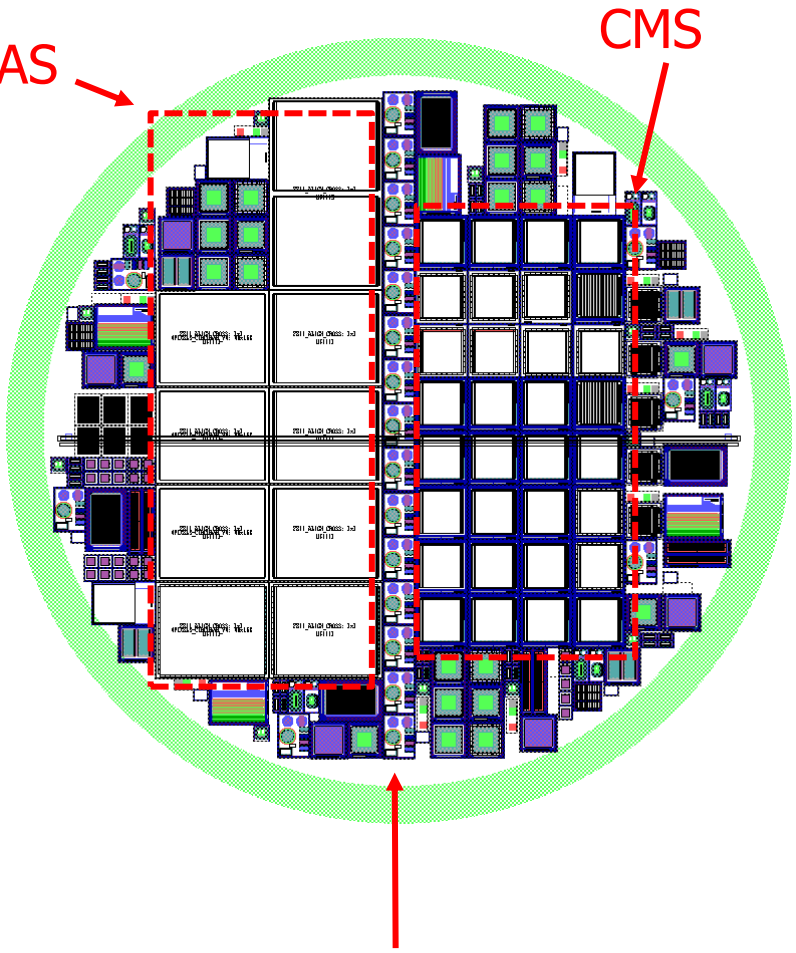
Si-Si Icemos silicon wafers, 100±2μm and 130±2μm active material with a ρ>3000 Ωcm

Process

- n-on-p planar process
- three p-spray doses

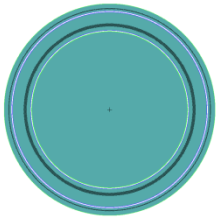
Layout

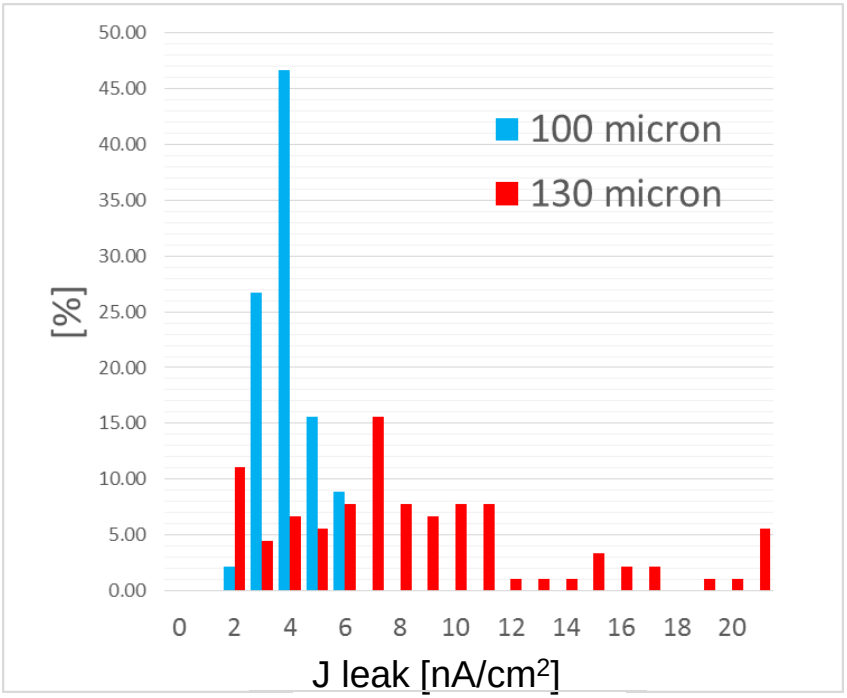
- Many test structures
- 10 ATLAS & 30 CMS pixel design



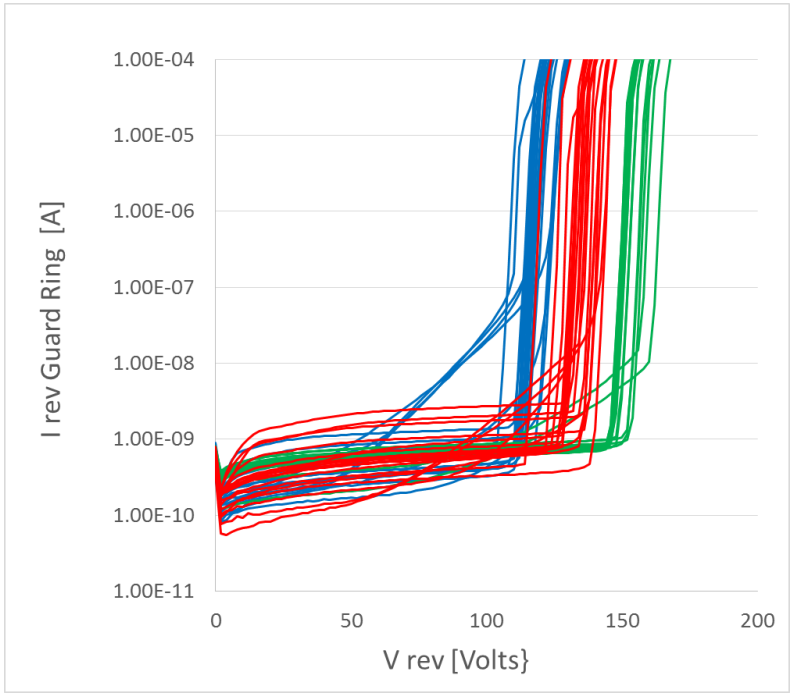
FBK test diode IV measurements

Circular 4mm2 diode with two GR





J_{leak} distributions on 135 diodes



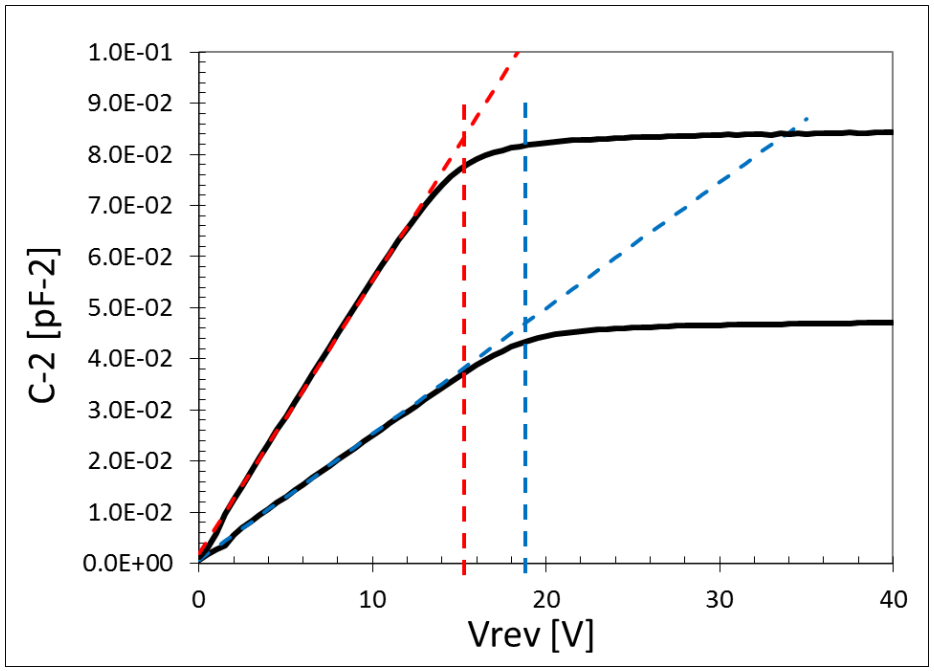
Guar Ring I_{rev} on 3 wafers
3 p-spray dose
Low Medium High

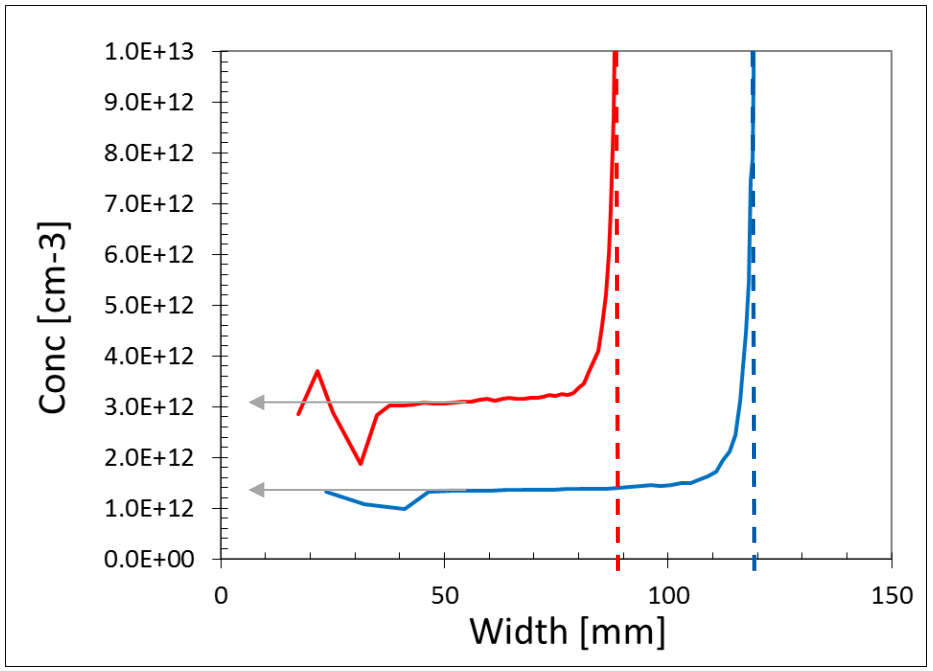
Test diode: CV measurements

$\frac{1}{C^2}$ → V_{dep} 16V and 20V

Concentration profile from CV

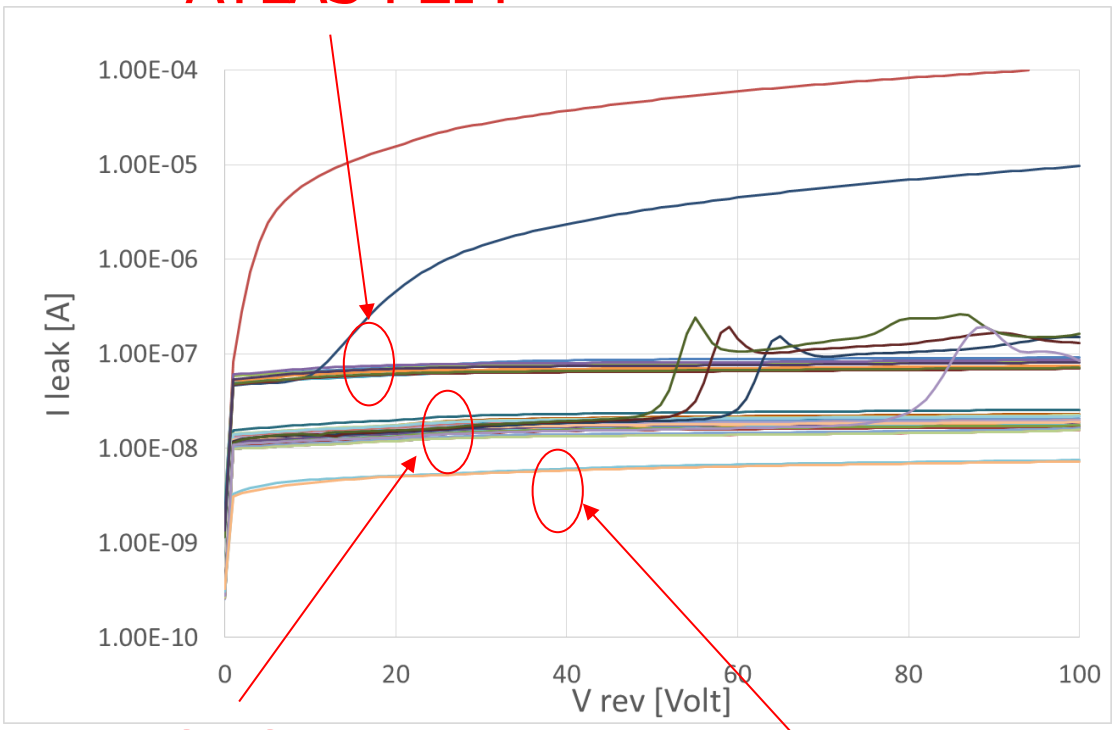
- Doping 1 – 3 E12
- Thickness about 10micron less than the nominal value





Pixel detectors: IV measurements on W81

ATLAS FEI4



CMS

CMS without Bias Grid

only a small part of the detectors is depleted

Comments:

- 40 devices (10Atlas + 30CMS)
- Some defective devices
- $V_{BK} > 100V$
- I_{leak} decrease if detectors area decrease

Pixel detectors: statistics

"good" detectors if

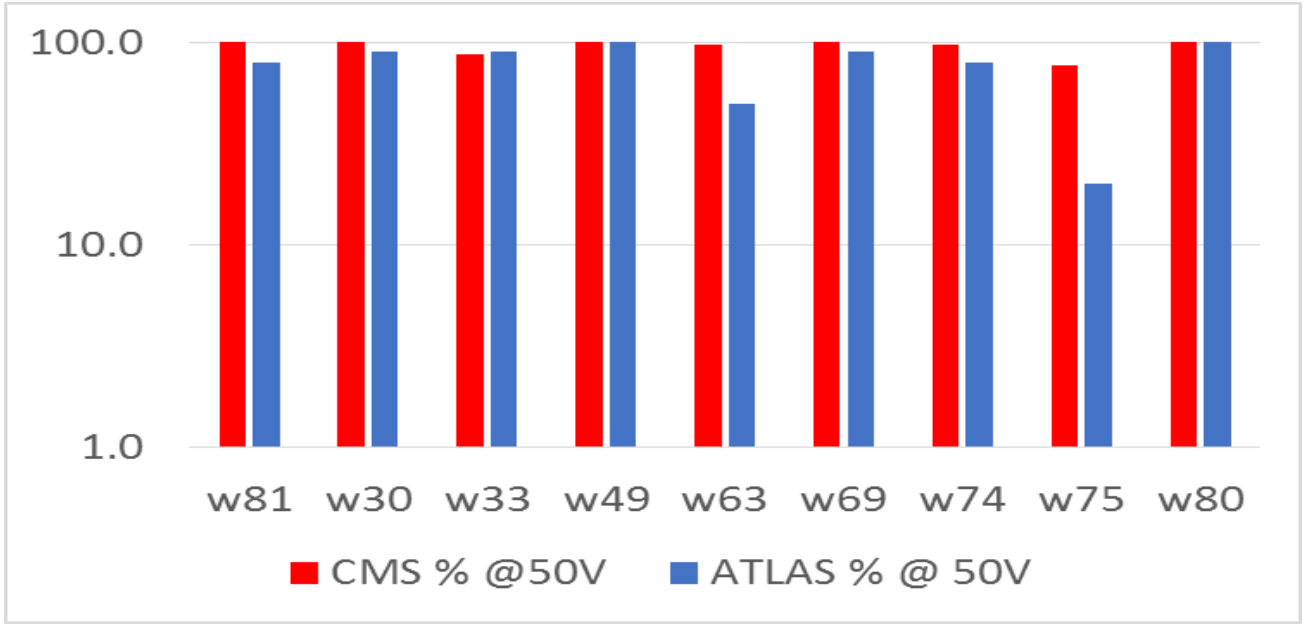
ATLAS I_{leak} < 1E-7 @ 50V

CMS I_{leak} < 5E-8 @ 50V

V_{depl} 20V

ATLAS 70/100 (70%)

CMS 257/270 (95%)



Most critical issues

1. Identify the "best" row material
   - We need a "processable" thin silicon substrate (100-150 μm)

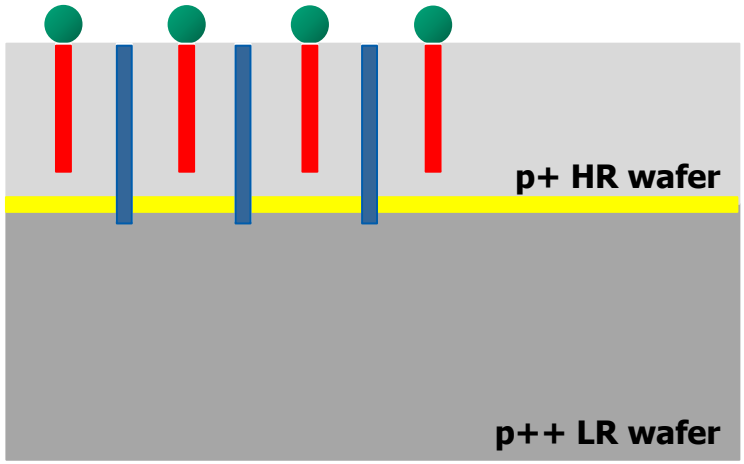
✓

2. Controls of the hole depth
   - Optimization of DRIE process

3. Doped Polysilicon Filling
   - Hole must be filled or partially filled

4. Two DRIE on the same wafer side

5. Deep SiO2 etching

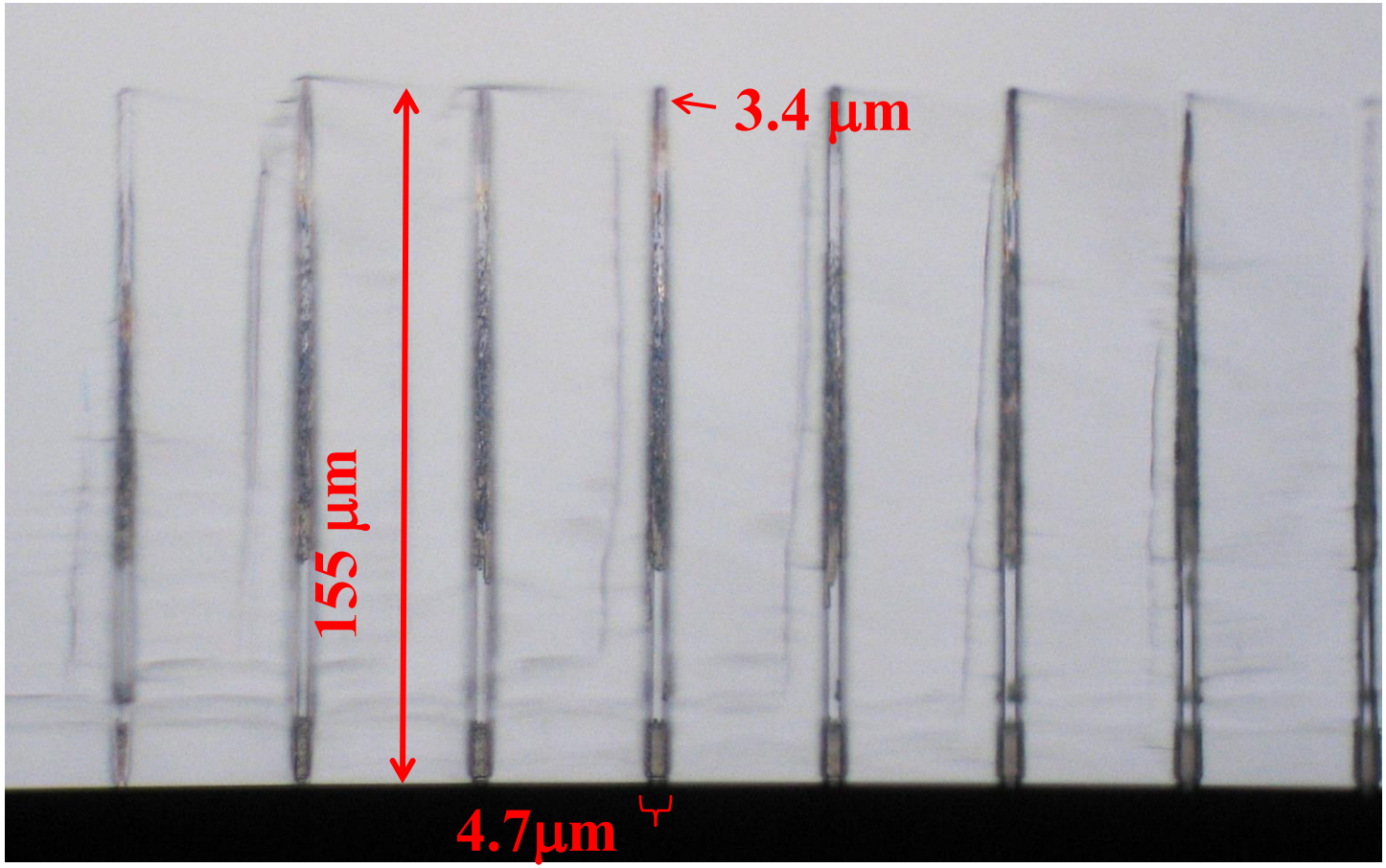


2. Controls of the hole depth (1)

- Optimization of DRIE process

TSV deeper than 130 μm

Holes with ∅=5 μm

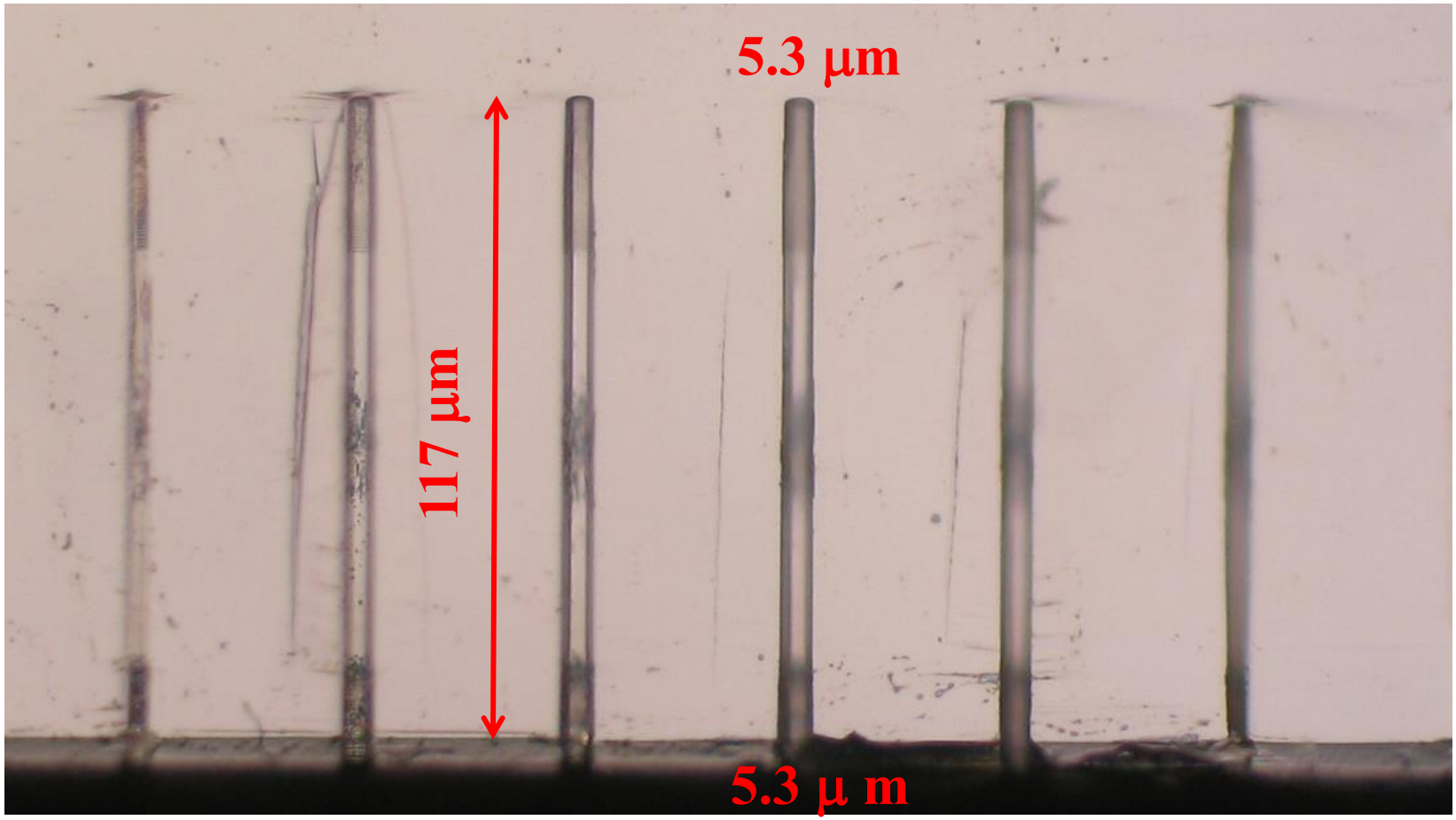


2. Controls of the hole depth (2)

- Optimization of DRIE process

Not TSV shallower than 130 μm

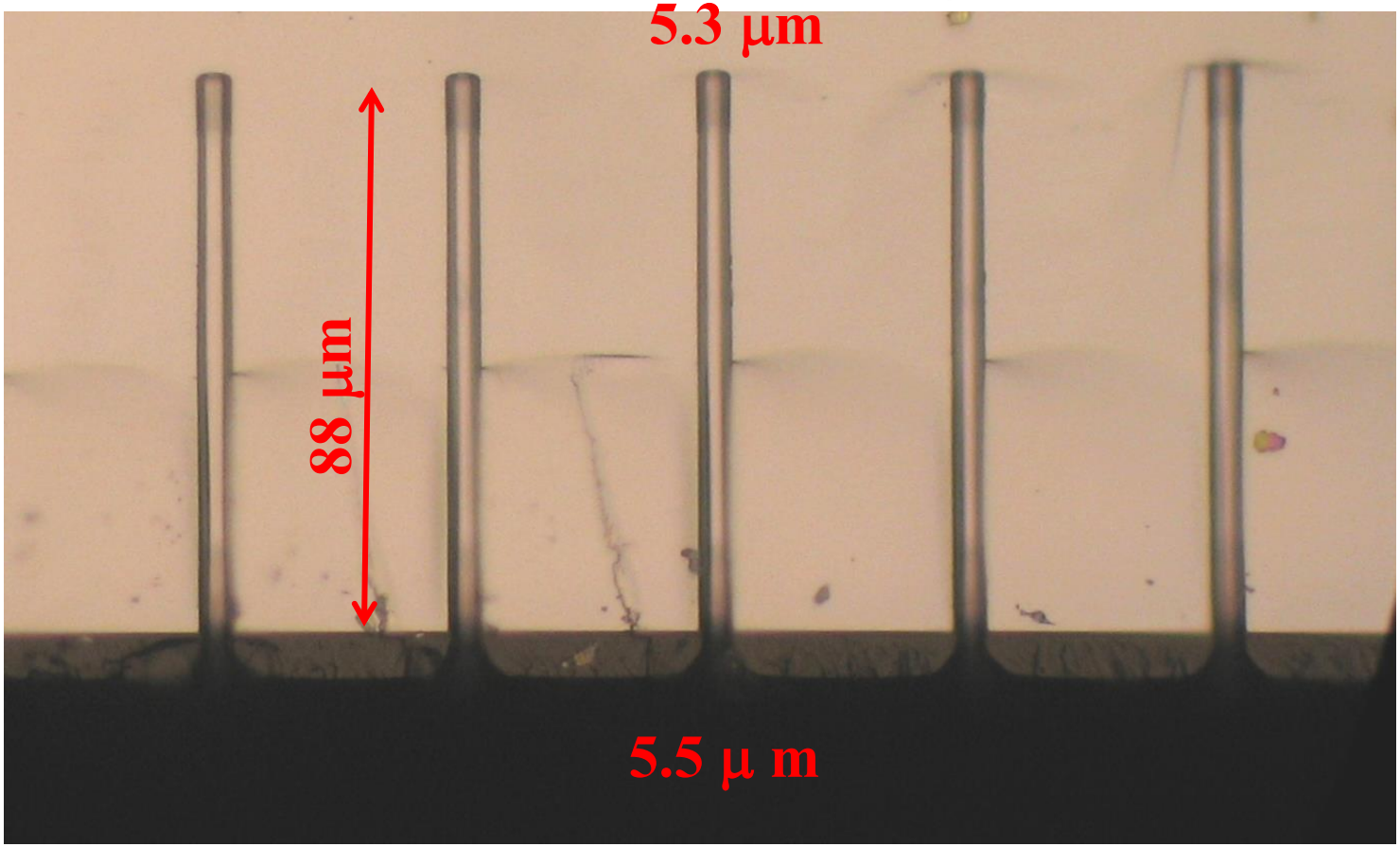
Holes with ∅=5 μm



2. Controls of the hole depth (3)

- Optimization of DRIE process

Holes with ∅=5 μm



Not TSV shallower than 100 μm

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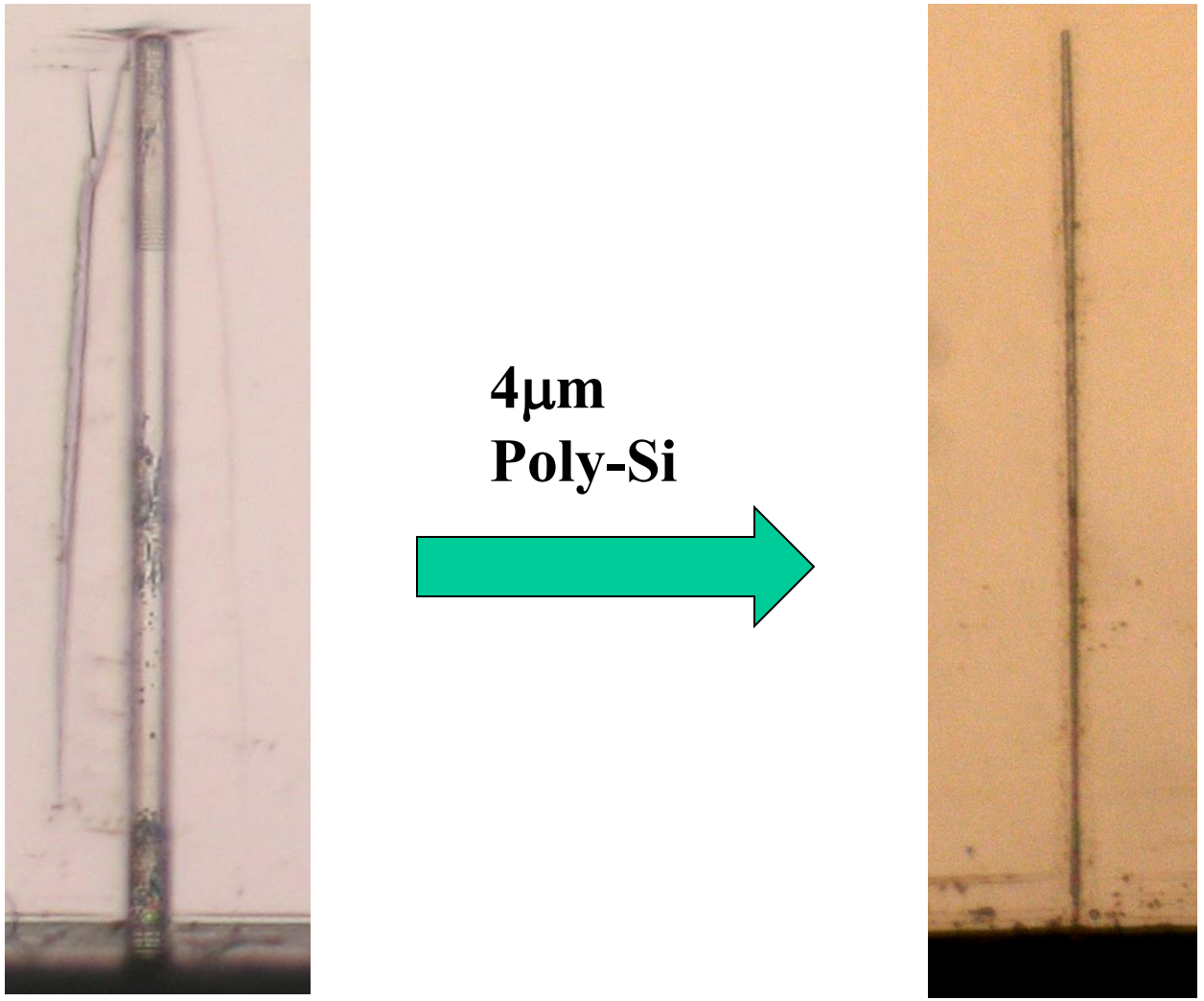
3. Doped Polysilicon Filling (1)

- Hole must be filled or partially filled

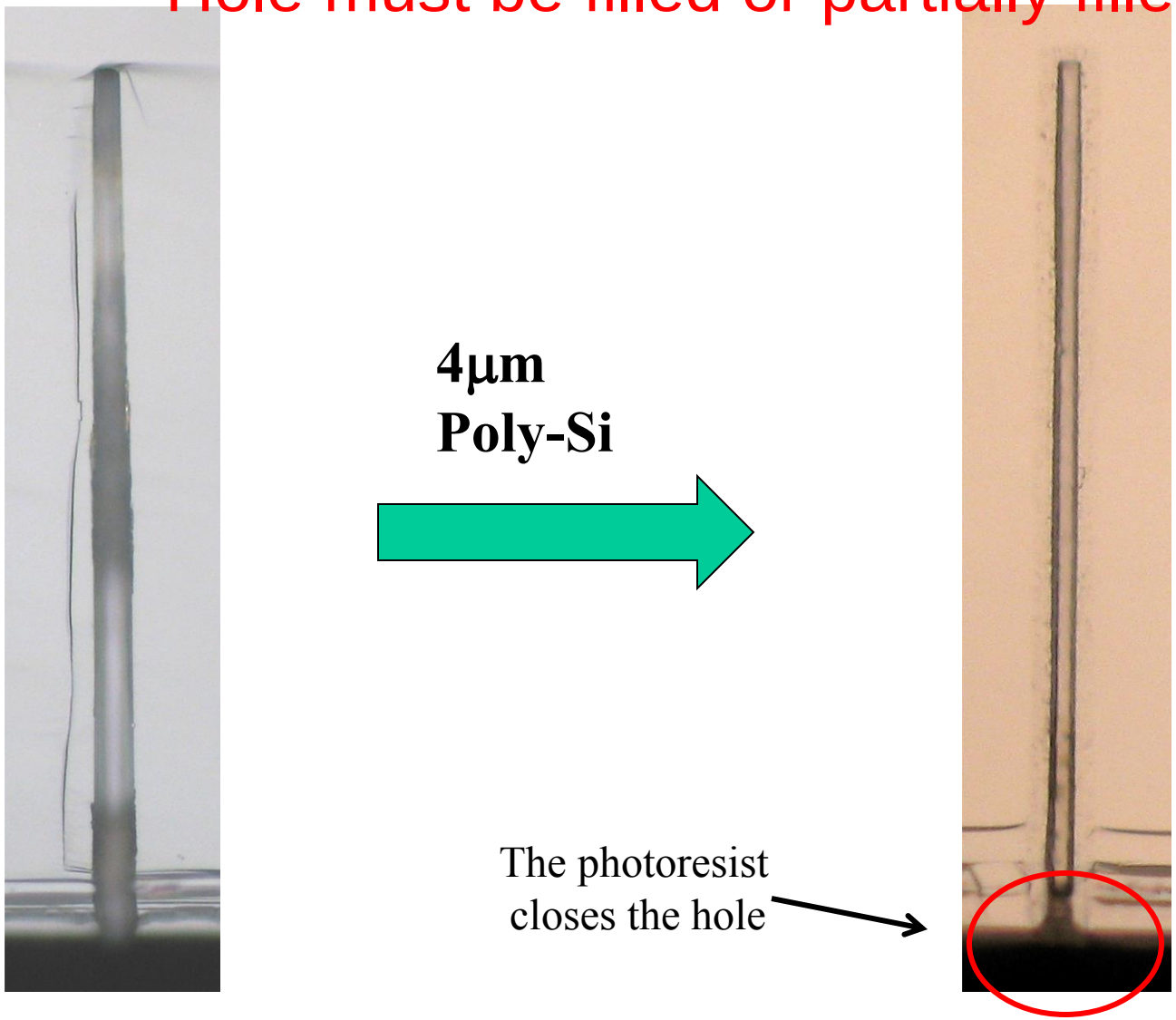
Poly-Si filling of a 5 µm hole



3. Doped Polysilicon Filling (2)

- Hole must be filled or partially filled

Poly-Si filling of a 12 µm hole



Most critical issues

1. Identify the "best" row material
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2. Controls of the hole depth
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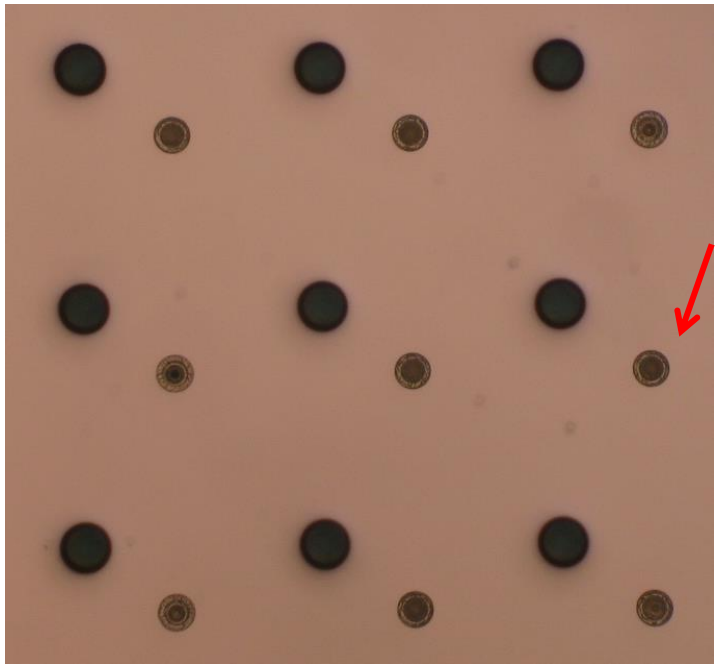
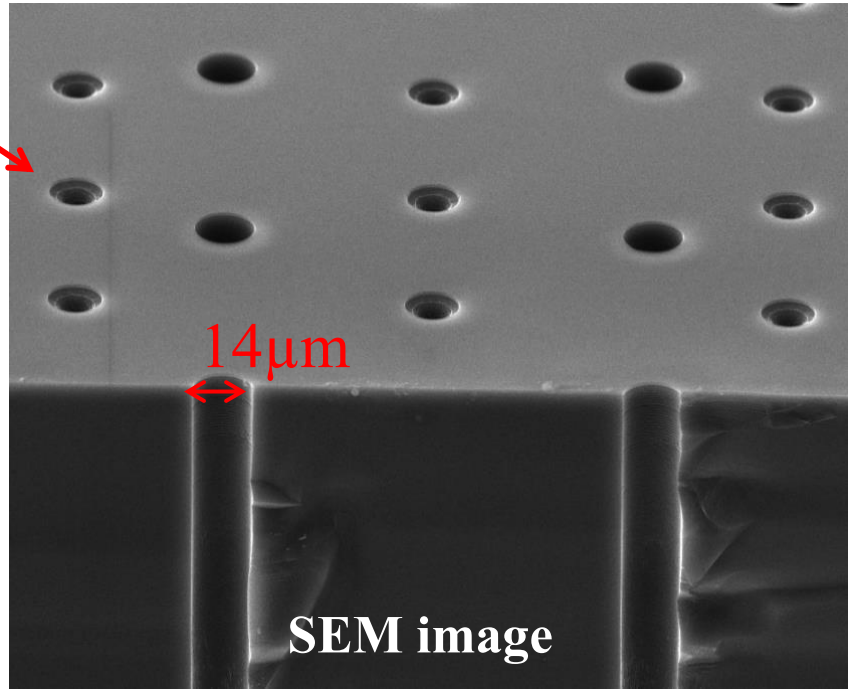
4. Two DRIE on the same wafer side
5. Deep SiO2 etching

4. Two DRIE on the same wafer side

Reducing the hole diameter with a polysilicon deposition



First holes
partially filled
with poly-Si



Picture from the surface
with photresist after second DRIE

Most critical issues

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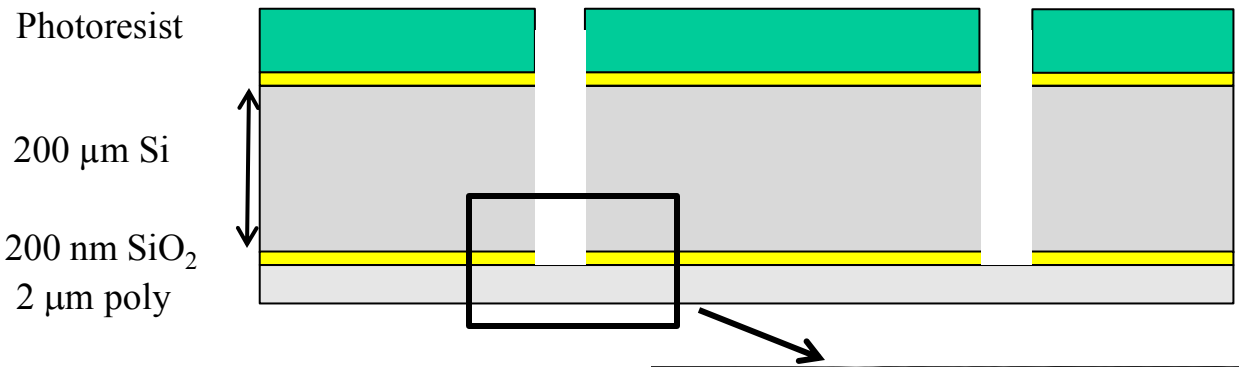

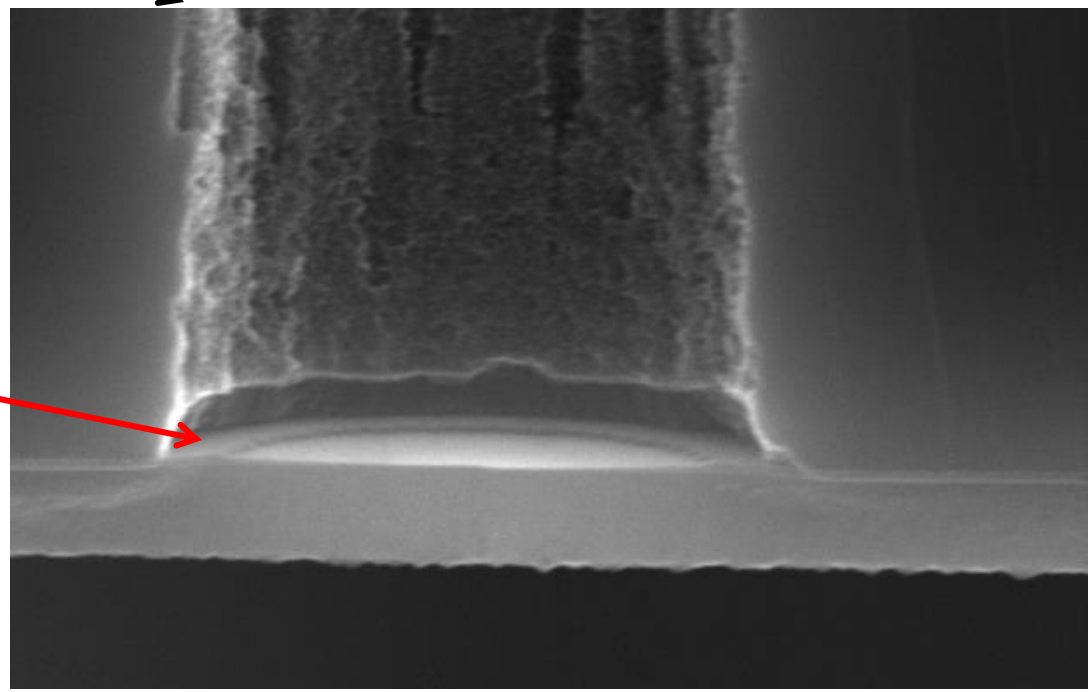

200 nm etched SiO_2

2 µm poly-Si

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Conclusions

- Designed a new technology for 3D single side detectors on thin material
- Settled most process critical issues
- Validation of acquired Si-Si material

Ready to start a new 3D batch!!!

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Thanks for your attention