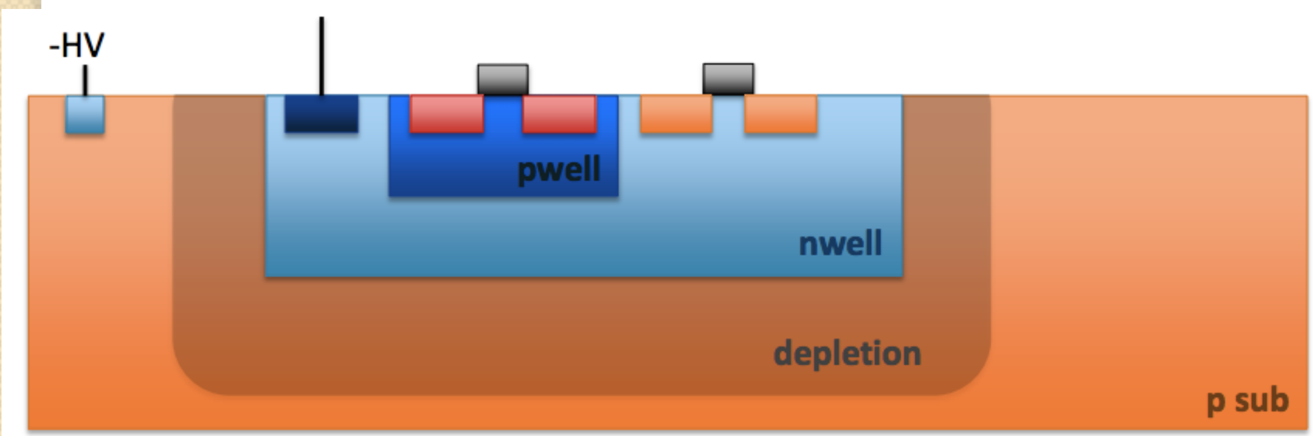
# Studies and status of CMOS-based sensors research and development for ATLAS strip detector upgrade

Vitaliy Fadeyev, Zach Galloway ,
Herve Grabas, Alexander Grillo , Zhijun Liang
Hartmut Sadrozinski, Abraham Seiden
*University of California, Santa Cruz*

# CMOS sensors developments

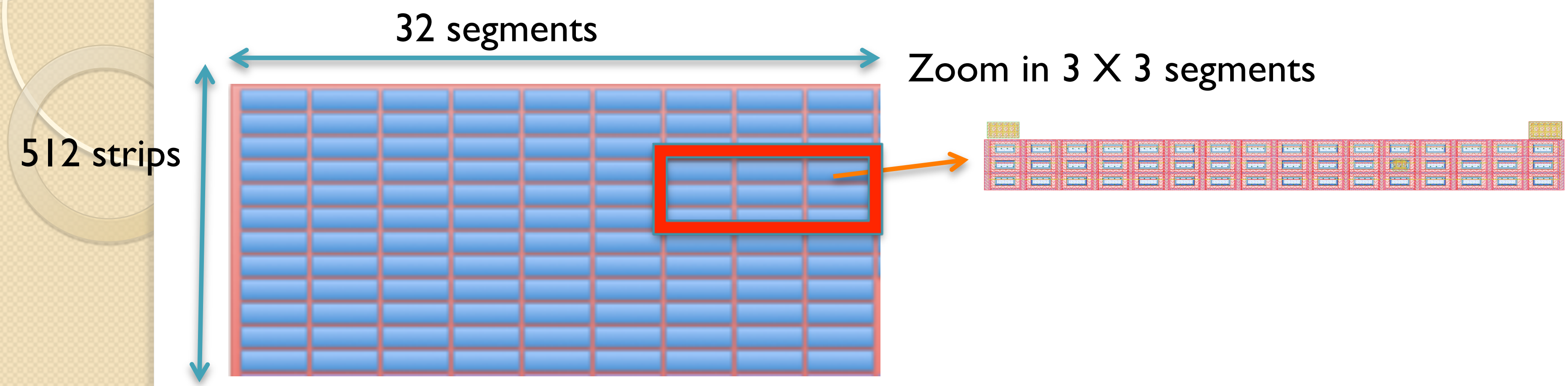
- Implemented in commercial CMOS (HV) technologies (350nm, 180nm)
  - Collection electrode is a large n-well/p-substrate diode
- Advantage:
  - High granularity: pitch can be reduced to below 50um
  - low material budget : Can be thinned down to 50um
  - Monolithic: Front-end electronics and sensor can be built in the same chip
  - Low cost
- Drawback:
  - Low MIP signal : 1000~2000 e



# CMOS sensors in ATLAS

- ATLAS agreed to explore the possible use of the technology for silicon strip detector upgrade
- Three-year plan:
  - Year 1: Characterization of basic sensor/electronics properties and architecture
  - Year 2: Fabricating and evaluating a large-scale device.
  - Year 3: Full prototypes of sensors and ABCN' readout chip
- Two foundries are targeted :
  - Tower-Jazz TJ180
  - Austrian Micro Systems AMS-H35.
- This talk will focus on the study of one of the test chip (CHESS chip)
  - fabricated in AMS-H35 HV-CMOS process.
  - designed by UCSC and SLAC
  - contains passive pixel arrays, stand-alone amplifiers, active pixel arrays, transistors.
- The testing results of CHESS chip in this talk includes
  - Characterize the diode properties of the pixel array
  - Characterize the stand-along built-in amplifier

# The concept of strip detector using CMOS technology




- one example design of the full size strip sensor based on CMOS technology.
  - Strip Sensor is made of 512 strips
  - Each strip is subdivided in 32 segments.
- Typical size of one segment of strip sensor is 40μm X 800μm

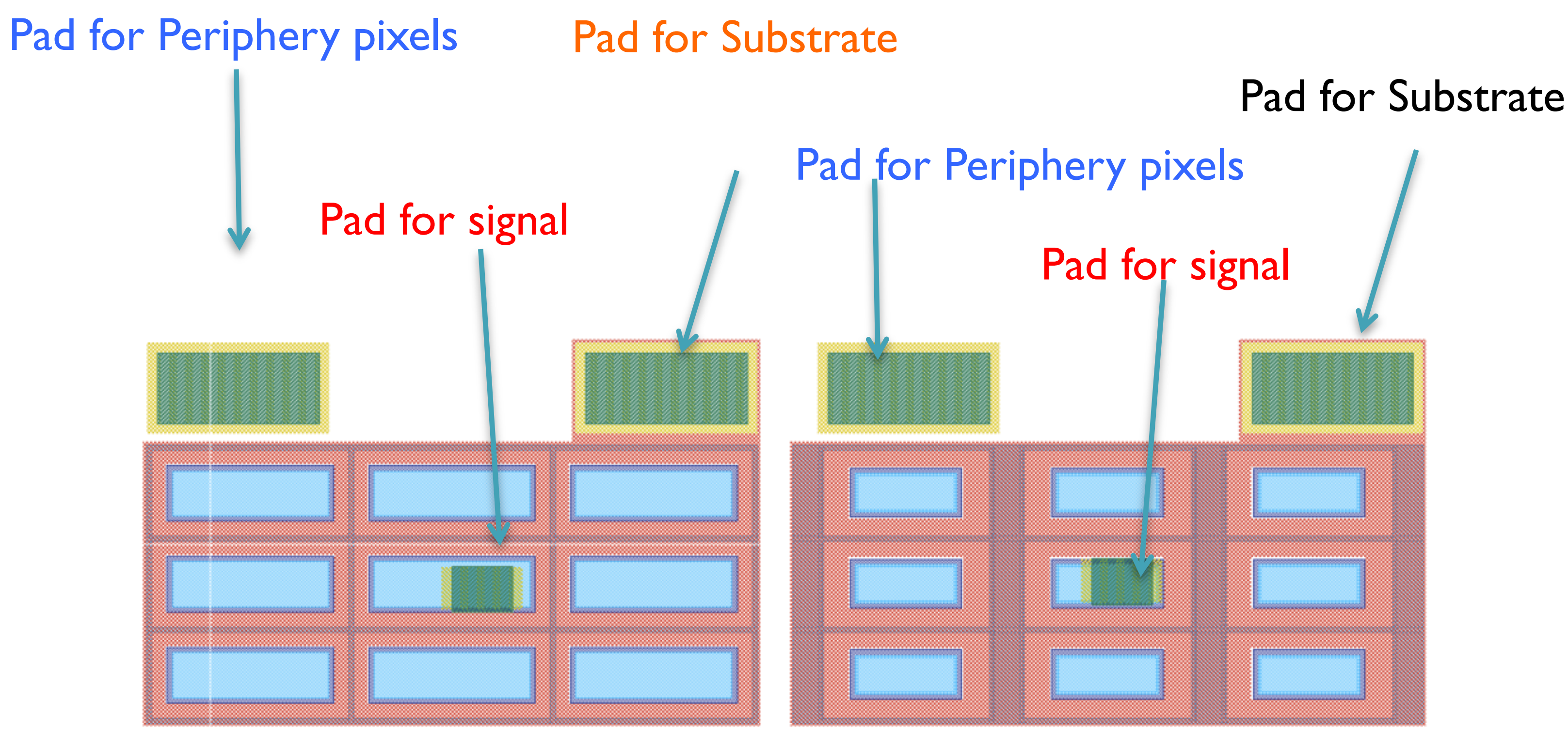
# HV-CMOS pixel array design

- Need to understand the performance of the segment (pixel) for strip detector application

- For strip application, larger segment (pixel) size is considered in the last test chip
  - 45μmX100μm , 45μmX200μm, 45μmX400μm 45μmX800μm
  - 30%-50% N-well fraction
    - Expect better performance in higher Nwell fraction
  - Electronics in the strip allow for strip segmentation
  - – AMS provides options for high resistivity substrate
    - Substrate resistivity can be up to a few thousand Ω*cm

# Layout of passive pixel arrays

- Groups of 3 x 3 pixels in a rectangular array
  - the eight outer pixels are electrically tied together
  - The inner pixel is connected to a separate probe pad
  - An additional probe pad is added for substrate biasing.

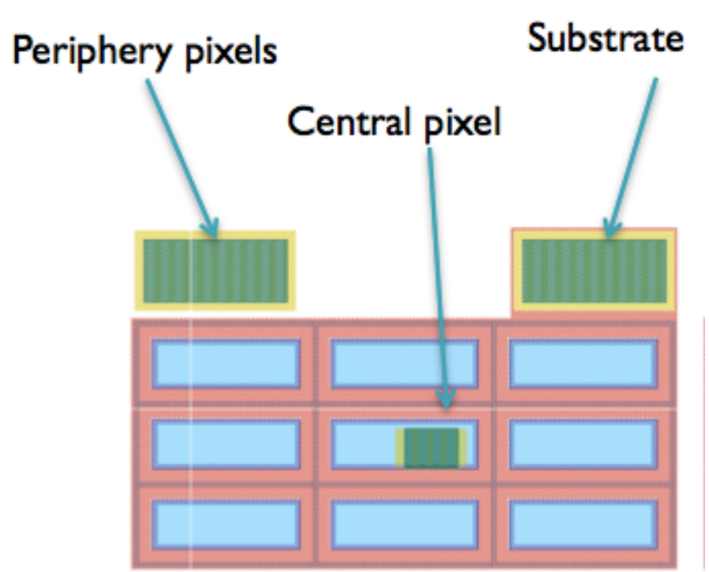



100µm x 45µm pixel 50% diode fraction

100µm x 45µm pixel 30% diode fraction

# I-V curve for CMOS pixel
# Testing setup and major Challenge

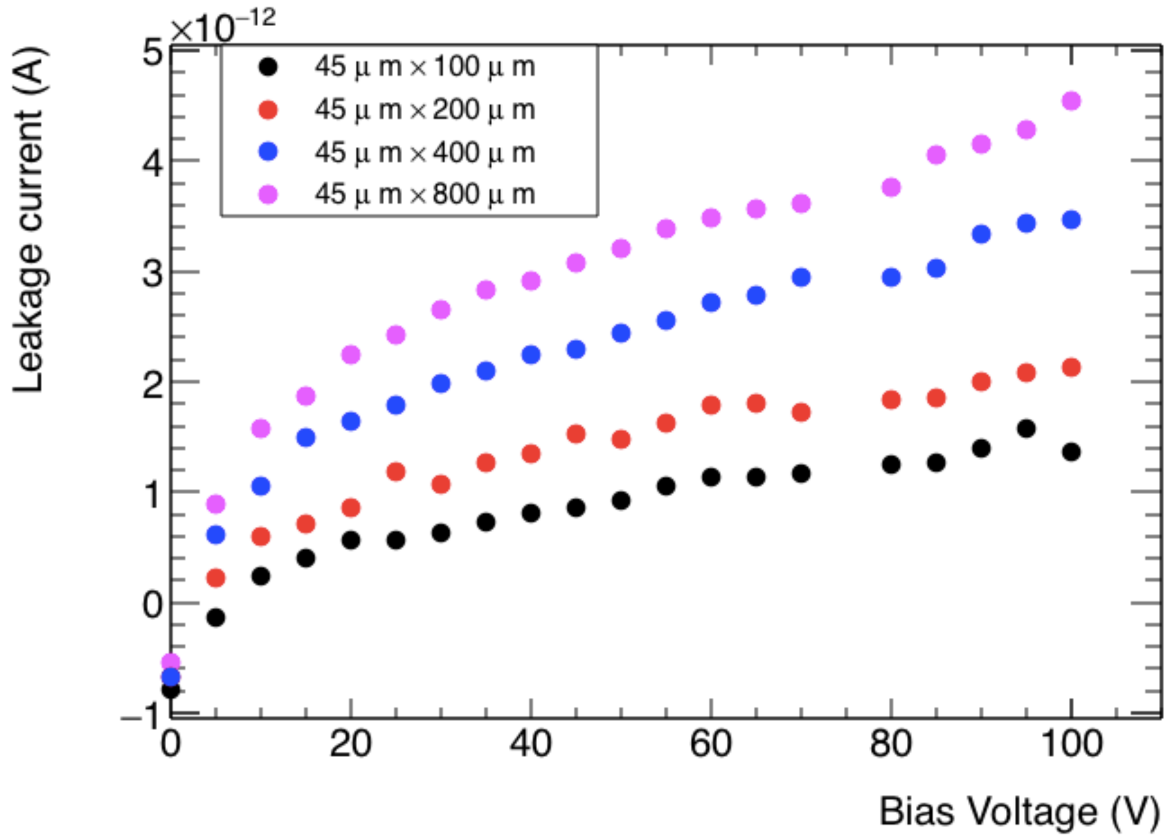
- Leakage current as function of bias voltage (I-V) is one of the basic test
  - Large Leakage current may induce noise in readout electronics
    - -> Lead to a low signal to background ratio
- Compared to conventional planar sensors for strip detector
  - Leakage current in single pixel is about much lower, by five orders of magnitude
  - Need setup for low noise measurement




Substrate: grounded
Perimeter pixels: +HV
Central pixel: +HV

# Central pixel IV

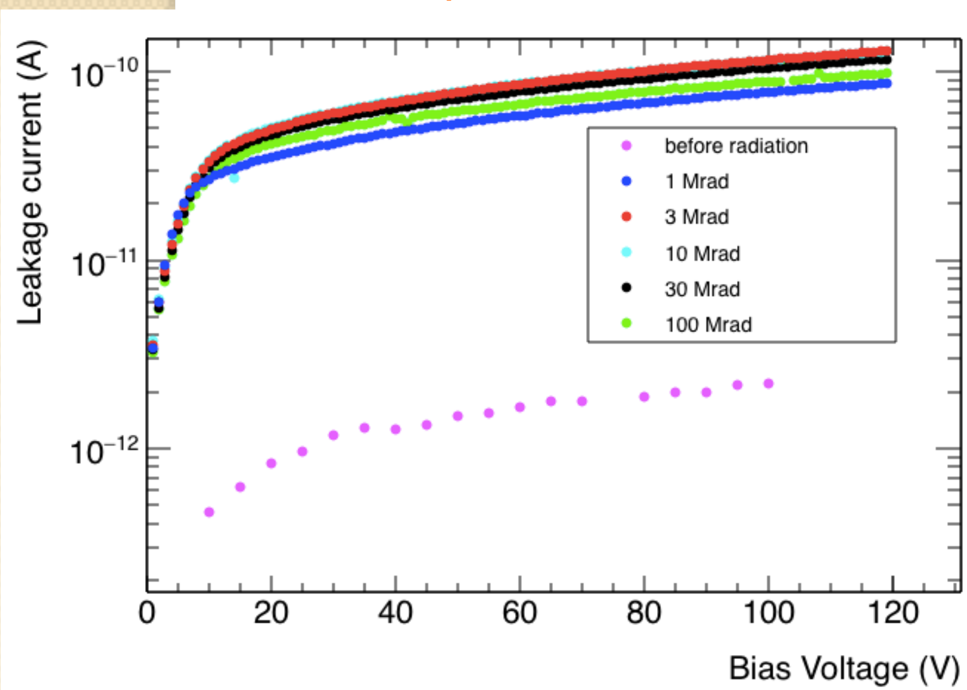
- Design of pixel in CHESS1 chip
  - Two design rule in AMS HV-CMOS technology : 60V and 120V
  - pixel array layout in CHESS1 chip follows the 120V design rule
- I-V measurement result
  - Can Biased up to 120V without breakdown
  - Low leakage current (pA level)
  - Leakage current proportional to pixel size.



# I-V curve after gamma Irradiation(1)

- Five CHESS1 chip with different dose
  - Irradiated by UNM group (Sally Seidel et al) at Sandia source
  - From 1Mrad to 100Mrad
  - Requirement in ATLAS strip detector phase two upgrade: 60Mrad
  - I-V measurement result after gamma irradiation
    - Orders of magnitude higher in leakage current than before
    - No significant difference between 1Mrad and 100 Mrad irradiated chip
    - it is still less 1nA after gamma radiation.

45X200um pixel , 50% N-well fraction



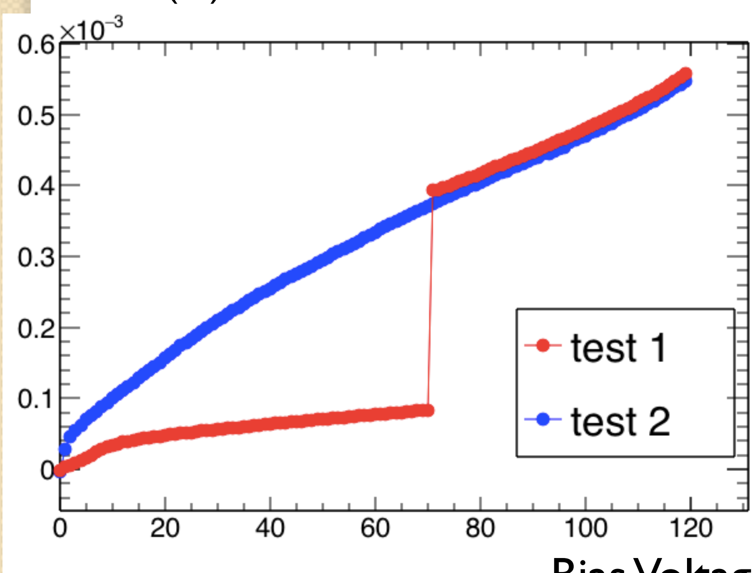

| ionizing dose | Leakage Current @VBias=100V |
|---|---|
| 100Mrad | 0.07 nA |
| 30 Mrad | 0.08 nA |
| 10Mard | 0.09 nA |
| 3Mard | 0.09 nA |
| 1Mrad | 0.06 nA |
| Before irradiated | 2 pA |

# I-V measurement in gamma irradiated CMOS chip (2)

- No break down in pixel array with 50% N-well fraction
- break-down like behavior in part of the pixels with 30% N-well fraction
- Perform two test in one of 30% N-well fraction pixel
  - Break down in the first scan at about 70V.
  - Leakage current increase by order of magnitude
  - The leakage current remain high after the first test.

Pixel size: 45X200μm
with 30% N-well fraction
30 Mrad gamma radiation

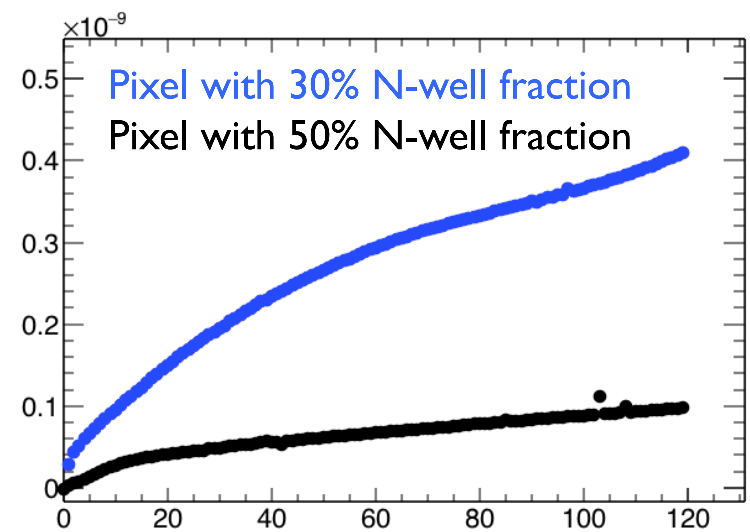
Leakage current (A)




Bias Voltage (V)

Pixel size: 45X200μm
With 30% N-well fraction
100 Mrad gamma radiation

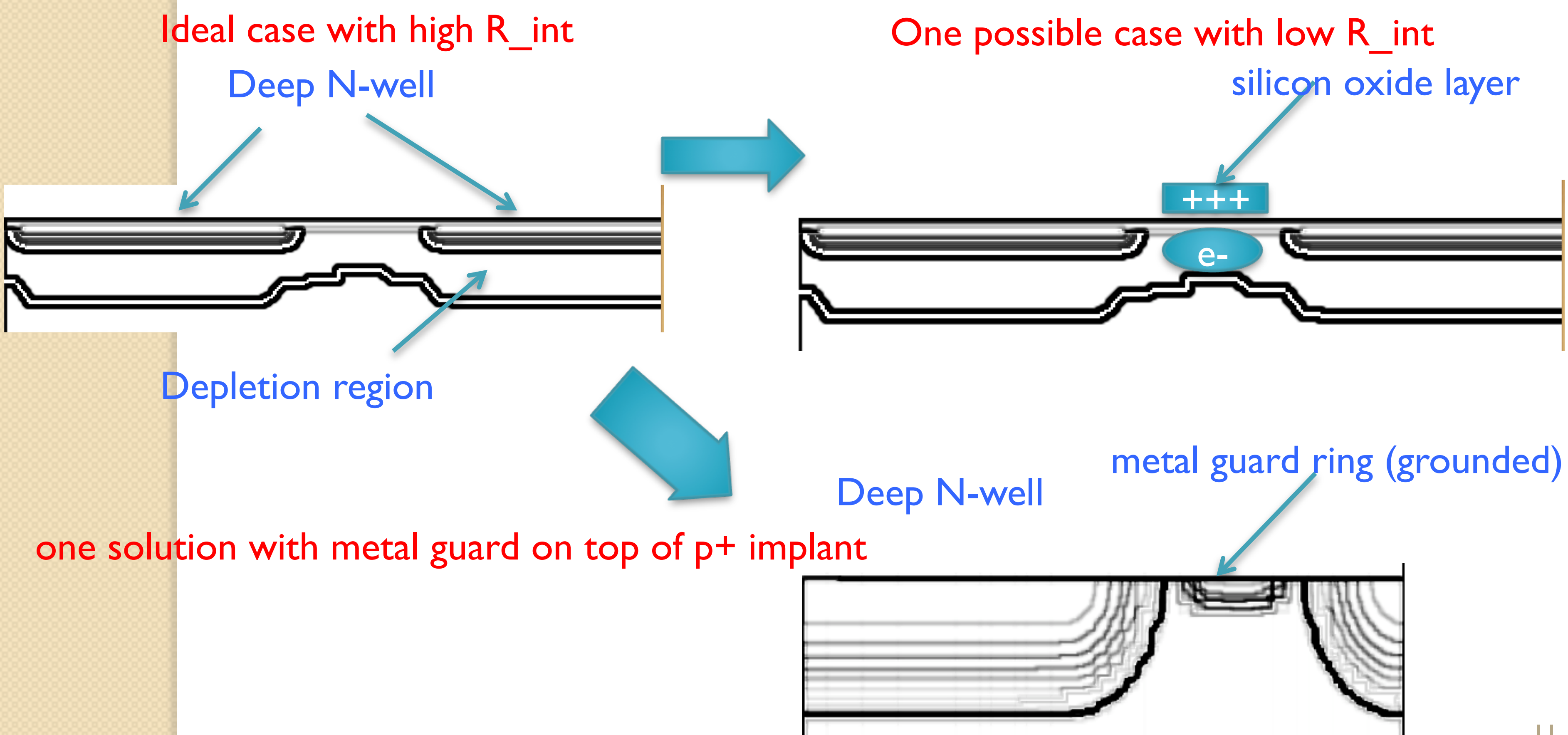
Leakage current (A)




Bias Voltage (V)

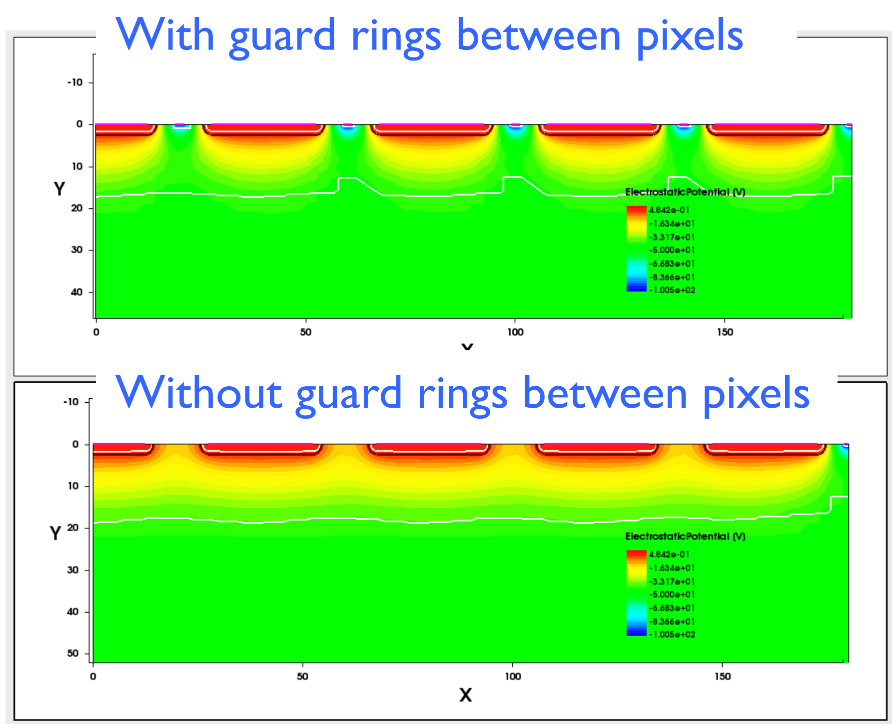
# Inter-pixel resistance measurement

- Inter-pixel resistance is the resistance between pixels
  - Low Inter-strip resistance
    - May lead to charge spread to nearby pixels -> low position resolution
- fixed oxide charges in the Si–SiO2 interface
  - may lead to a conductive layer of electrons at the surface
- One solution is use metal guard ring on top of p+ implant



# Inter-pixel resistance measurement simulation

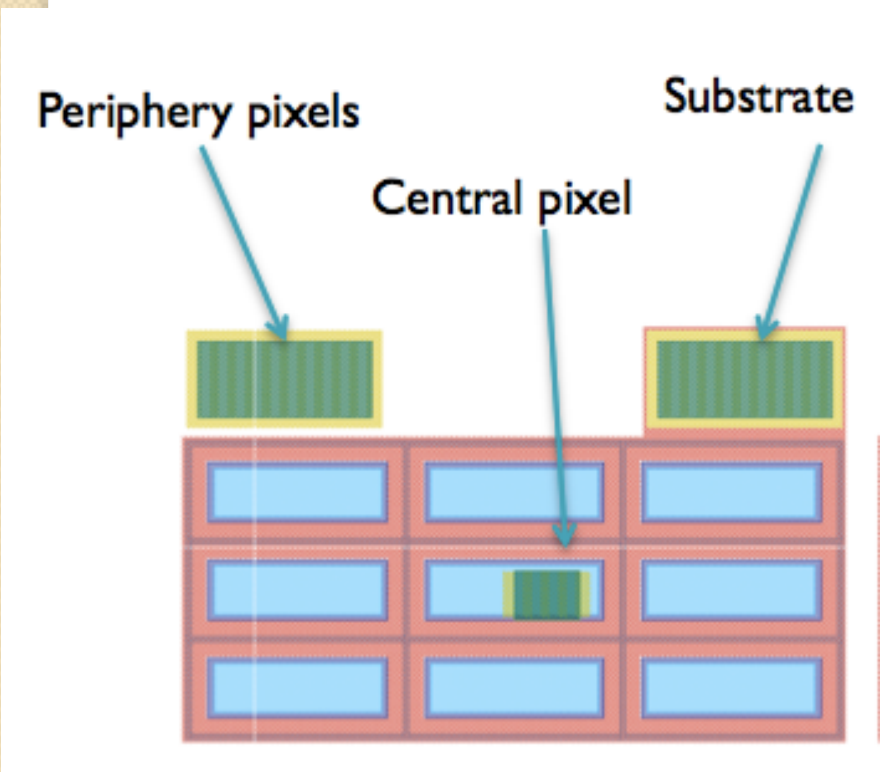
- Two type of pixel arrays are designed
  - Pixel array with guard rings
    - Guard ring grounded the region between pixels
    - get a better isolation and larger inter-pixel resistance
    - Draw back : may lead to inefficiency in regions between two pixels
  - Pixel array without guard rings
    - Need to understand the surface condition and its inter-strip resistance




Simulated by Julie Segal from SLAC

# Test setup for inter-pixel resistance

- Vary the bias voltage of the perimeter pixels by 1 V.
  - The variation in central pixel current reflect inter-pixel resistance

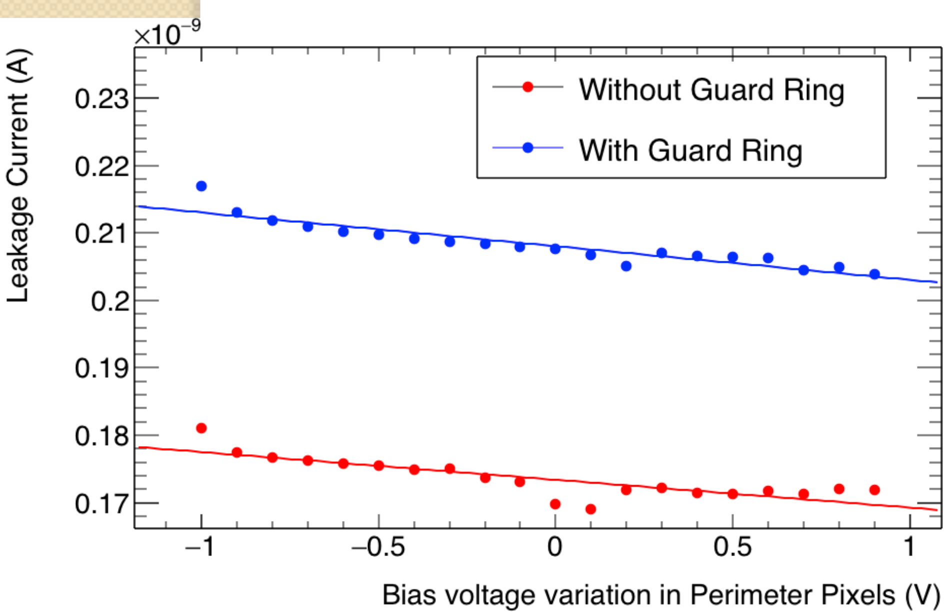


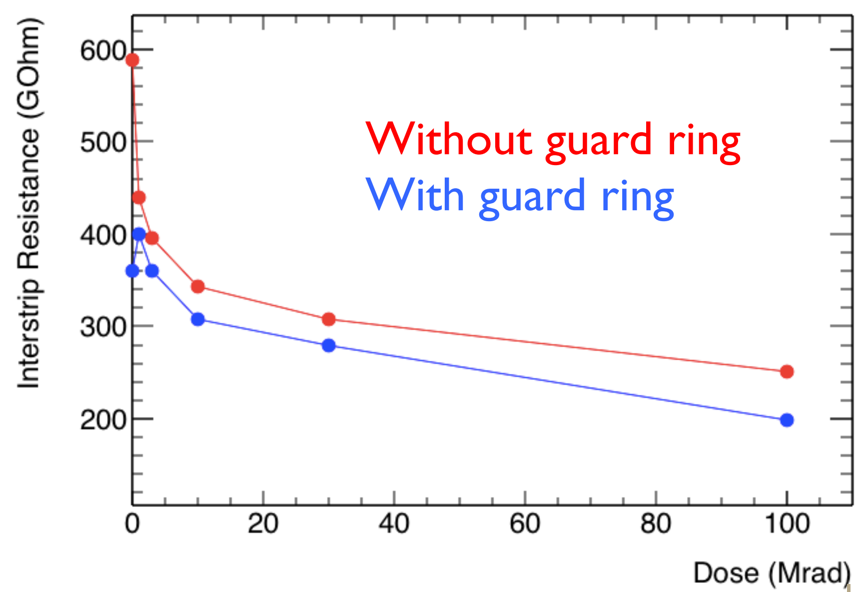

- Substrate: grounded
- Perimeter pixels: from 98V to 100V
- Central pixel: 99V

# Inter-pixel resistance (2)

- The inter-pixel resistance is obtained by measuring
  - "current in center pixel"
  - "voltage difference between the central and peripheral pixels"
- The pixel without guard ring may lead to low inter-pixel resistance
  - It turned out that Inter-pixel resistance is large in both case w/wo guard ring.

Pixel size: 45X200μm
with 30% N-well fraction

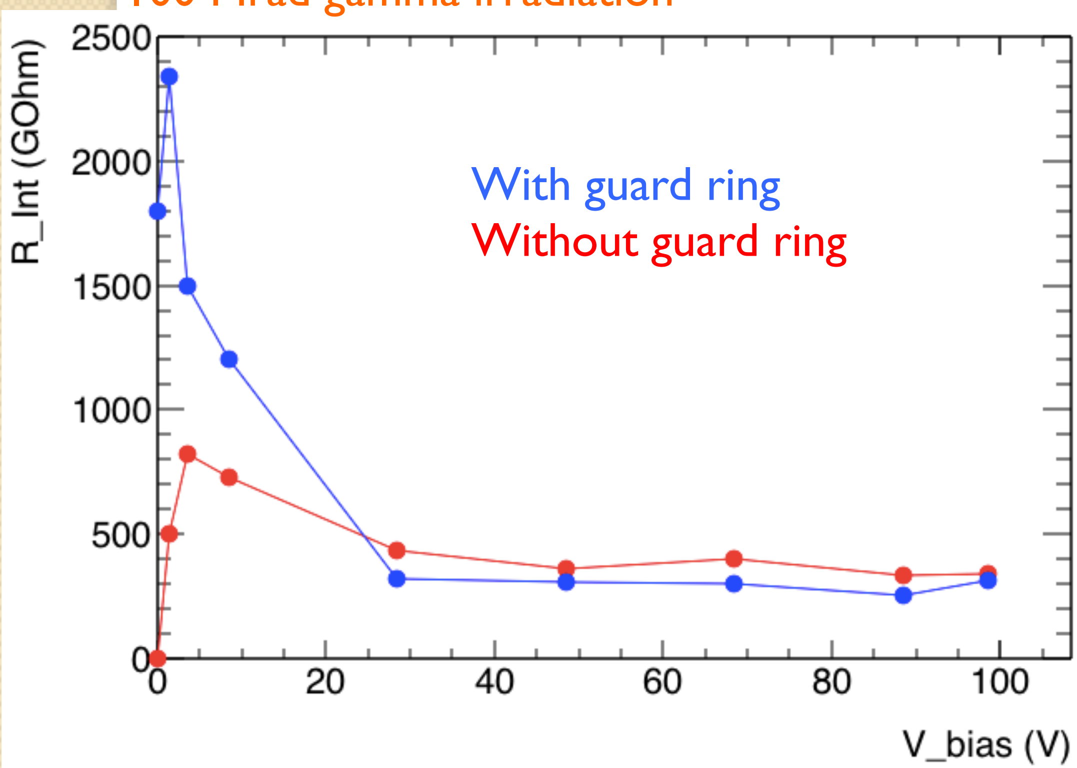


# inter-pixel resistance Vs Bias voltage

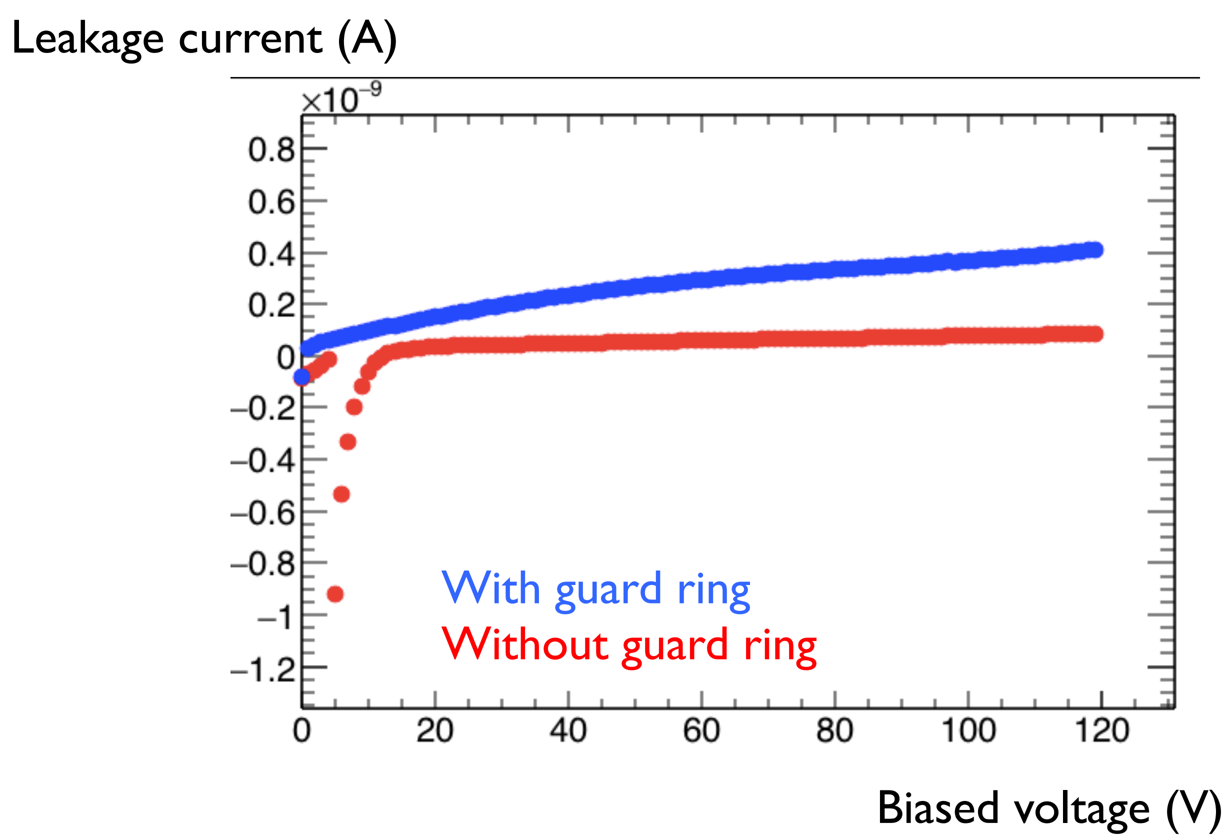
- Comparing inter-pixel resistance for pixel with and without guard ring
  - Inter-pixel resistance (R_INT) is similar at high bias voltage
  - At zero bias case, R_INT goes down to Mohm level for the pixel without guard ring.

Pixel size: 45X200μm
with 30% N-well fraction
100 Mrad gamma irradiation



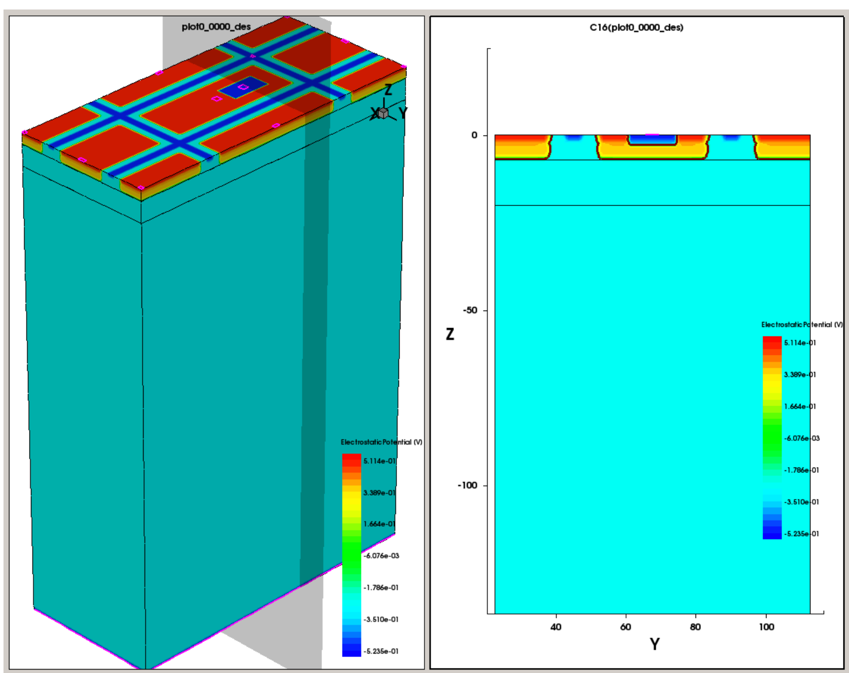
# I-V curve for the pixel w/wo guard ring

- Found negative leakage current for the pixel without guard ring.
- May be due to inversion layer after radiation predicted by simulation
  - However, inversion layer hypothesis is in contradiction with the high inter-pixel resistance.
  - high resistance for non-guard ring array is a puzzle we are trying to understand



# capacitance measurement

- Capacitance of the pixel is very important
  - Very important input to the design of readout frontend electronic
  - Related to the readout noise
- Simulations predicts that
  - Single N-well capacitance without in-pixel electronics : ~50fF
  - Single N-well capacitance with in-pixel electronics: ~100fF
- Need measurement to verify that.



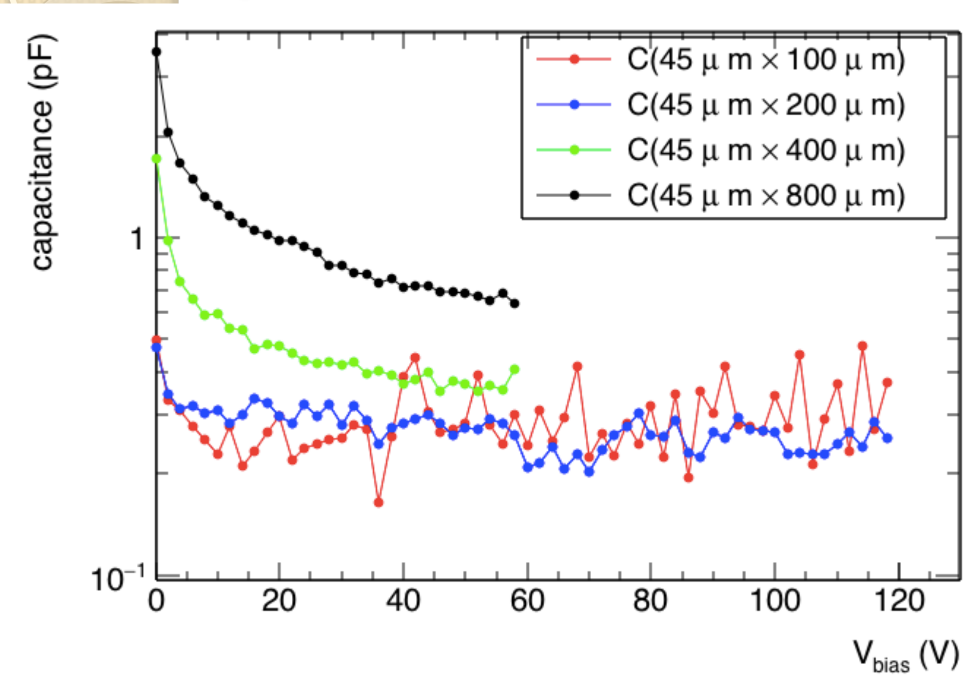

P-well size: 25um x 14um (from CHESS1)

Single n-well pixel capacitance without p-well: 46fF

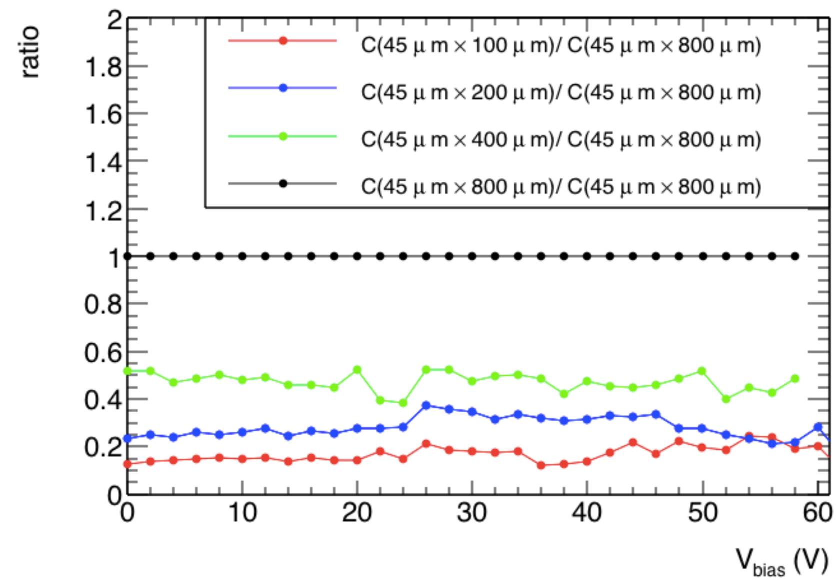
With p-well: 104fF

Simulated by Julie Segal from SLAC

# Capacitance measurement of central pixel with different size




The central pixel capacitance at low bias voltage is roughly proportional to pixel size.

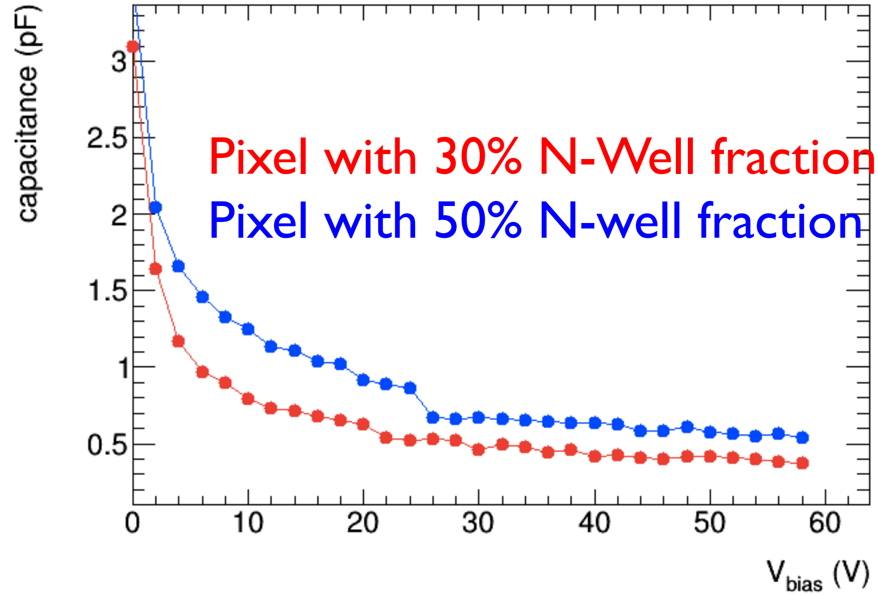



The simulation predictions are fairly consistent the measurements for the case of single N-well capacitance without in-pixel electronics

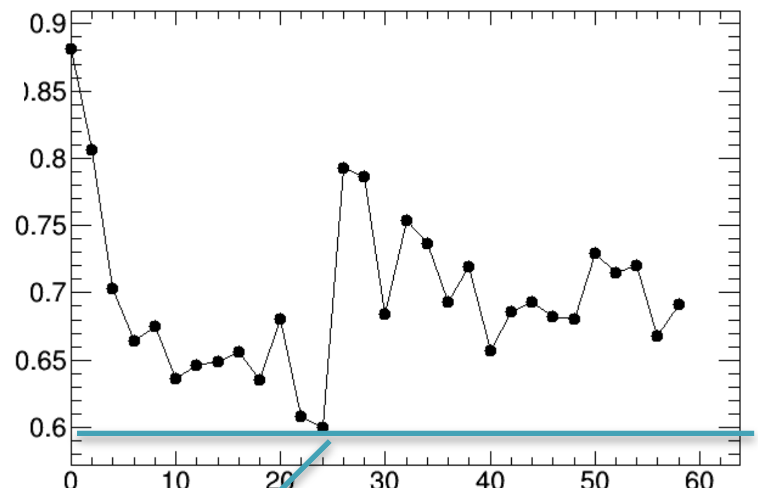
| Bias voltage | Measurement Result (fF) | Prediction from simulation (fF) |
|---|---|---|
| 60V | 87 | 63 |
| 120V | 52 | 55 |

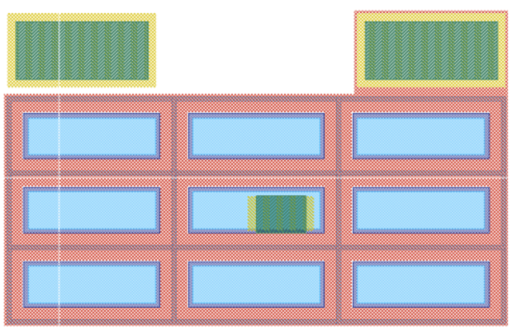
# Capacitance of pixel array with different diode area fraction

Observe lower capacitance for pixel with lower diode fraction

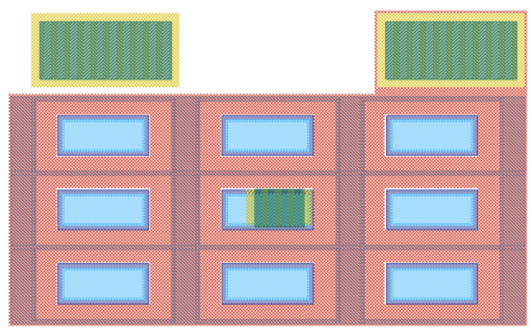



C(30% N well)/C(50% N-well)



100µm x 45µm pixel 50% diode fraction

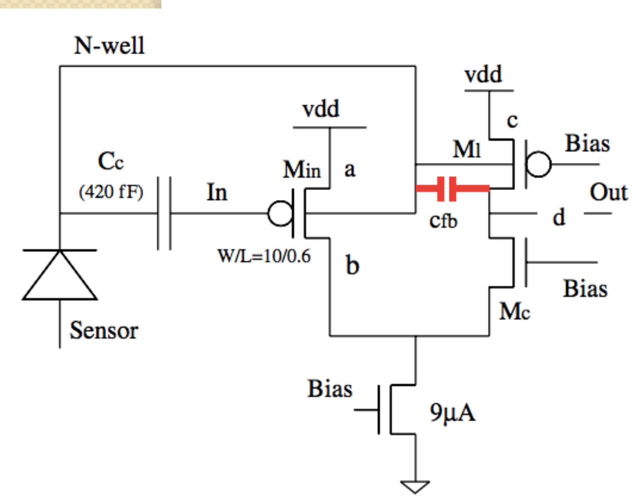


100µm x 45µm pixel 30% diode fraction

Expected ratio between the bulk capacitance of Pixel with 30% N-well fraction and pixel with 50% N-well

# Design of amplifier

- signal is relatively low due to thin depletion region.
- A monolithic design of a built-in low-noise amplifier is needed
  - The pixel array and amplifier are designed in the same chip
  - The amplifier design must be radiation hard
    - radiation tolerant layout techniques is used
  - The raise time should be fast as well for LHC application
    - 16ns raise time for active pixel signal after amplification



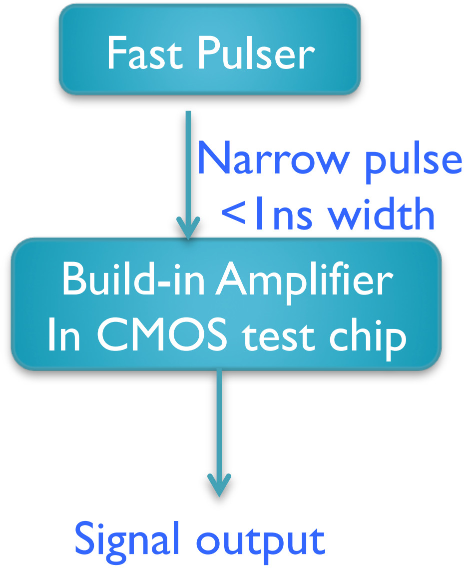

Schematic from Ivan Peric

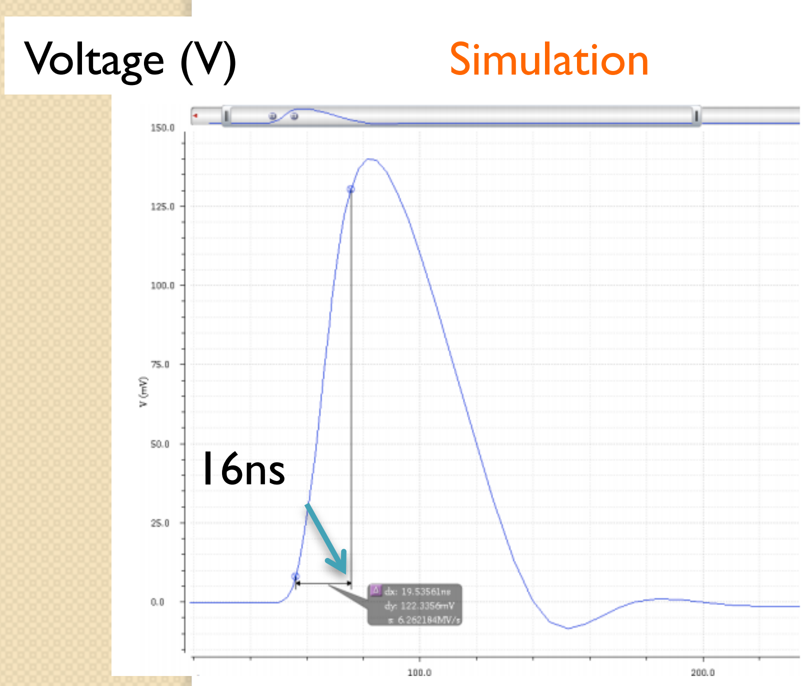
Nuclear Instruments and Methods in Physics Research A 582 (2007) 876–885

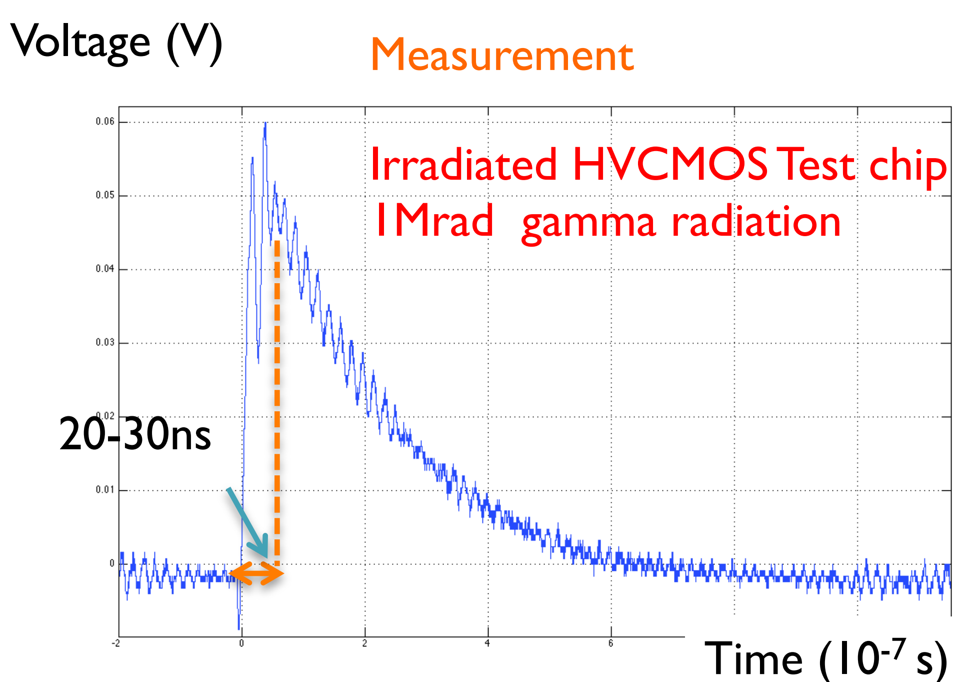
| Specifications | Simulated values |
|---|---|
| Rise time | 16 ns (10 - 90 %) |
| Noise | 200 $e^-$ |
| Gain | 500 mV/fC |
| Power consumption | 210µW/ amplifier |
| Pulse duration | 50ns |

# Amplifier testing

- Preliminary study of stand-alone amplifier in CMOS chip
- Response time to narrow signal pulse input is about 20~30ns.
  - Close to simulation prediction (16ns)
  - Fully functional after 1Mrad gamma radiation
- More study to do done for input noise and the gain.
  - Still getting pickup noise , and  mis-adaptation at the input.
  - Need better shielding and input setup in next step



# Summary of CMOS sensor testing

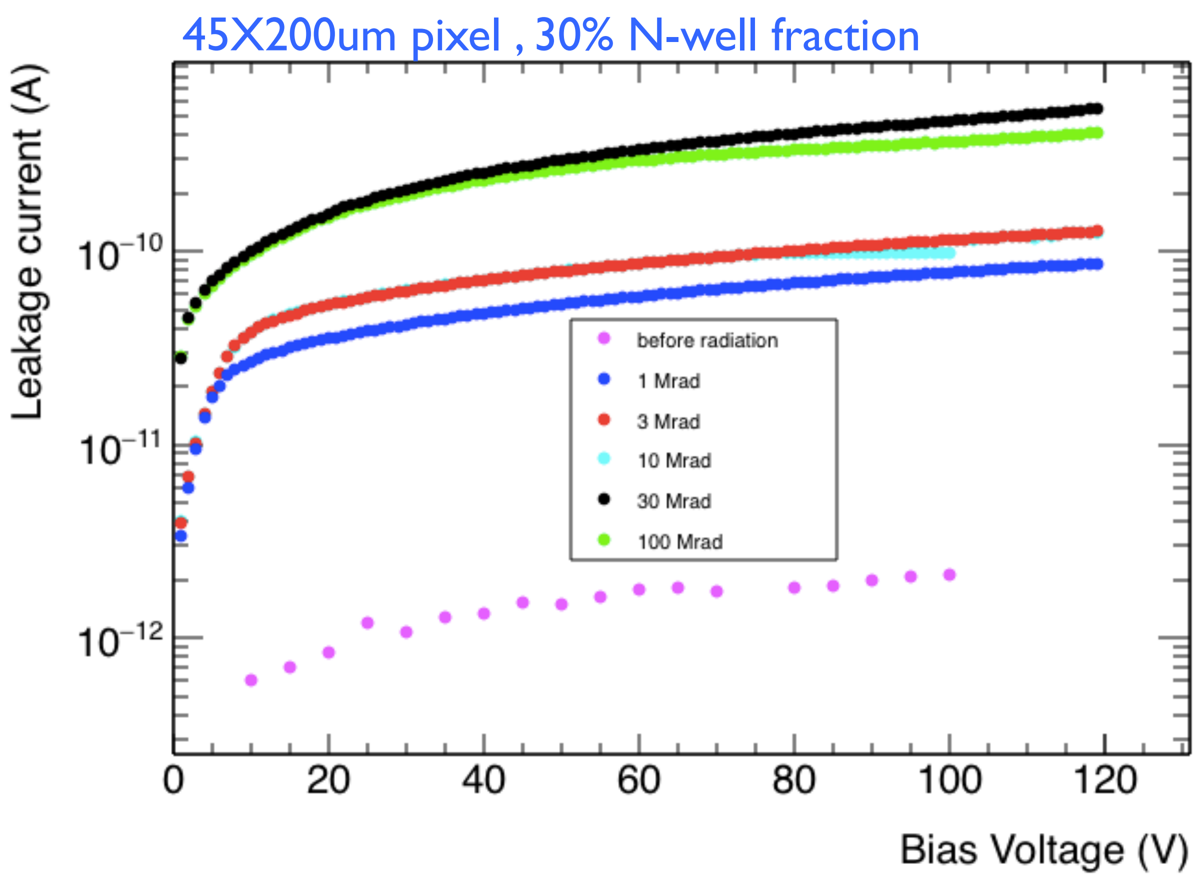
- Preliminary I-V and capacitance results for pixel array in test chip
  - I-V measurement
    - Before radiation
      - Can Biased up to 120V without breakdown
      - Low leakage current (pA level)
    - After gamma radiation
      - No breakdown for Pixels with 50% N-well fraction
      - Soft breakdown for part of the pixels with 30%
  - C-V measurement
    - Capacitance at low bias voltage is roughly proportional to pixel size.
    - Observe lower capacitance for pixel with lower diode fraction
  - Inter-pixel resistance
    - Very good isolation between pixel even after 100MRad Gamma radiation
    - inter-pixel resistance is high even in pixel array without guard ring.
      - This is not understood yet, further study is needed.
  - Build-in Amplifier testing in CMOS test chip
    - Response time is about 20~30ns
    - Agree with simulation

# Next step for CMOS sensor development

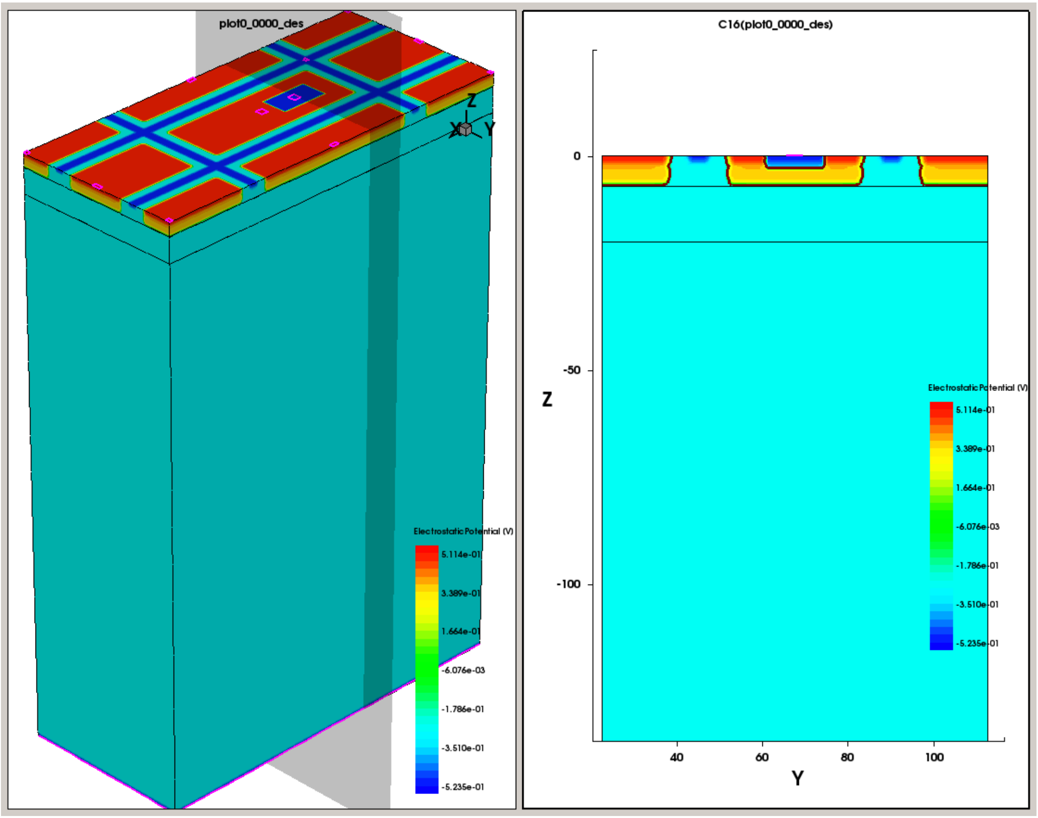
- Next test chip in March 2015 is planned.
  - It will be  a large array.
    - 128 strips made of 32 pixels.
    - plan to prototype the readout architecture.
  - Strips with active amplifier and discriminators
  - Strip hit for groups of 128 strips with LVDS readout.
  - Engineering run with AMS HV-CMOS technology with multiple substrate resistivity

# Backup

# I-V curve after gamma radiation 30% N-well fraction



# Capacitance with embedded p-well




P-well size: 25um x 14um (from CHESS1)

Single n-well pixel capacitance without p-well: 46fF

With p-well: 104fF

P-well to n-well: 57fF

- All the usual disclaimers apply, *but more* (don't know process details, especially diffusion profiles, etc)
  - *For n-well to substrate capacitance simulation, we know substrate doping*
- Did not include p-diff or Gate ox capacitance for PMOS transistors in n-well