HVCMOS Sensors for LHC Upgrade

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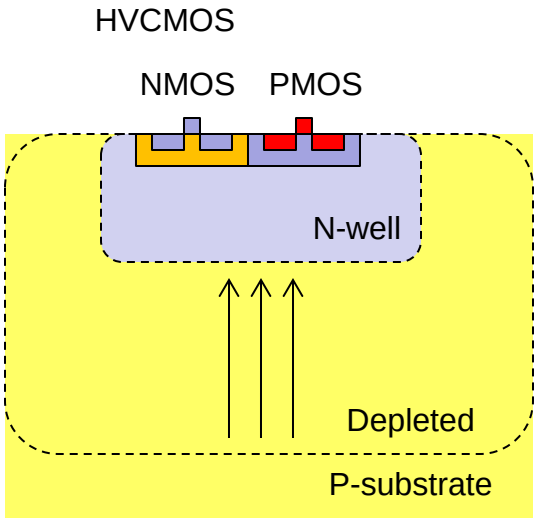
for HVCMOS collaborations

Introduction

- HVCMOS detectors are depleted active segmented detectors implemented in a CMOS process
- The sensor element is an n-well diode in a p-type substrate
- The electronics is placed inside the n-well sensor electrode.
- High voltage is used to deplete a part of the substrate.
- The main charge collection mechanism is drift of the charge signal from the depleted region

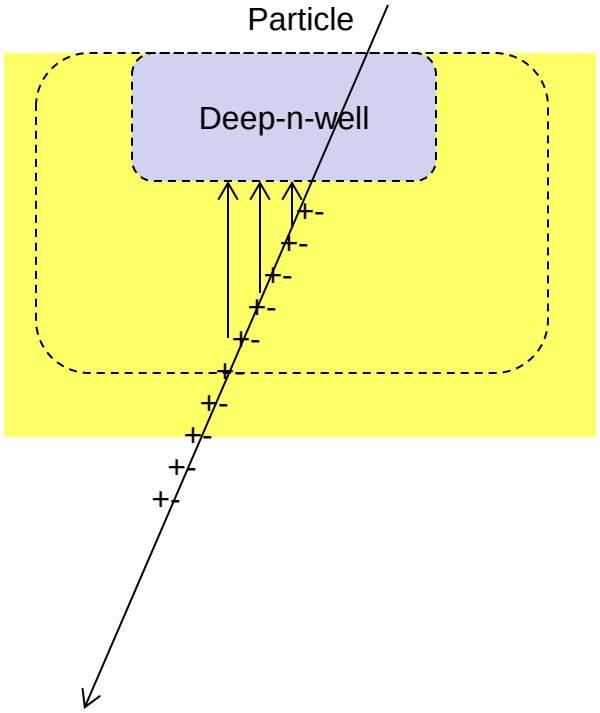


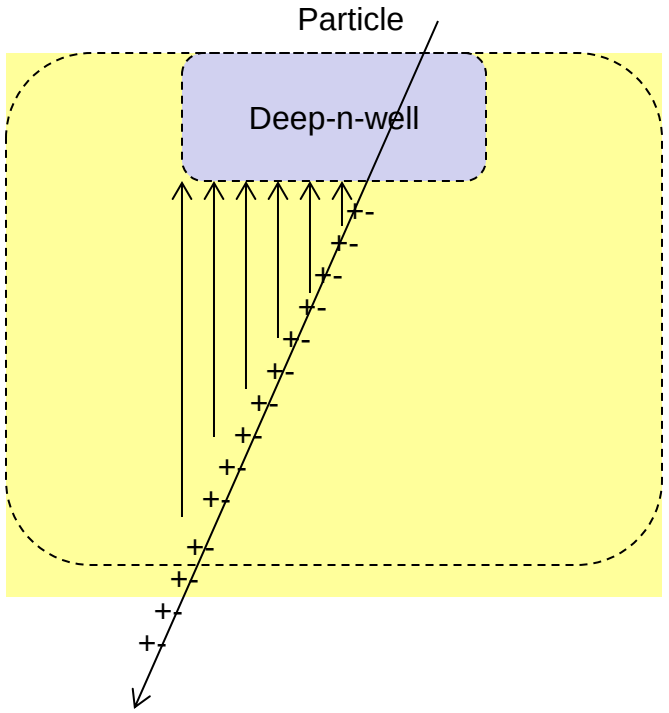
Applications

- We are developing HVCMOS sensors for the following experiments: ATLAS pixels, strips (ATLAS, CMS), CLIC, Mu3e

Substrate resistivity

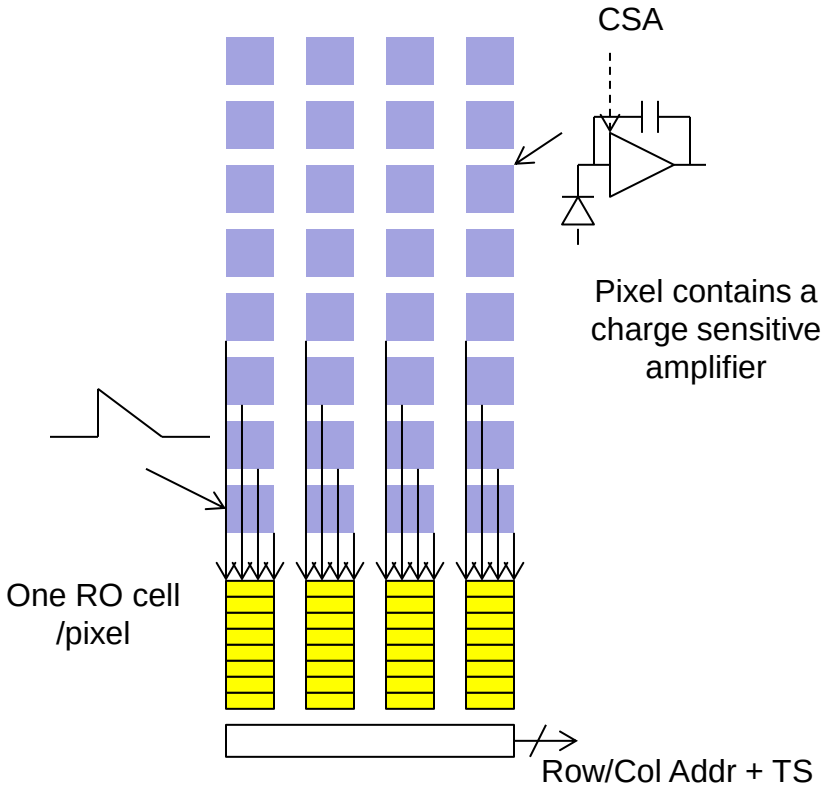
- HVCMOS can be implemented in standard CMOS technologies
- These technologies have substrate resistances of 10 to 20 Ωcm.
- The HVCMOS structure can be improved by taking a substrate of higher resistance (for instance 100 – 1000 Ωcm) instead of the standard one. (Non-standard CMOS process)
- The transistors will be not affected since they are placed in n-wells and not is in the substrate itself





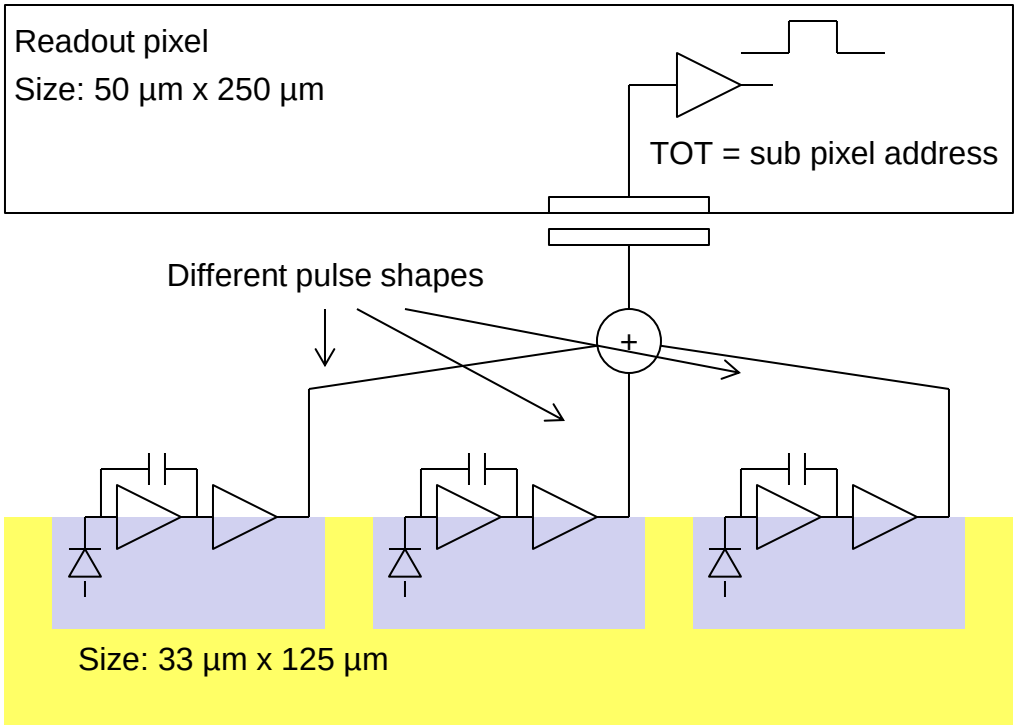
Sensor architectures - monolithic

- Depending on proposed application we have several sensor architectures.
- For Mu3e and strips we have the monolithic sensors. Active pixels contain usually only the analog circuits like the charge sensitive amplifier. The pixels are connected to the readout cells placed at the chip periphery. Every pixel has its readout cell. These RO cells do zero-suppression and generate hit-addresses. RO-cells contain hit buffers (Mu3e) of hit multiplexer (strips)
- Instead of analog pixels we are investigating the use the pixels with comparators that generate pixel addresses and transmit the addresses to the periphery.



Sensor architectures - hybrid

- For ATLAS pixels and CLIC we propose the smart sensor concept
- We use the existing readout chips (FEI4 in the case of ATLAS and CLIC-pix in the case of CLIC) for the readout of HVCMOS sensors.
- Advantages in comparison with the standard hybrid sensors:
- The signal transmission between sensor- and readout chip can be done capacitively, without bumps
- Capacitively coupled pixel detectors - CCPD
- Another advantage can be increased spatial resolution. Many smaller pixels can be coupled to one channel of the readout chip



350nm and 180nm technologies

- We have started HVCMOS developments in AMS H35 (350nm) technology
- Since 2011 we investigate also AMS H18 (180nm) because this technology allows smaller pixels and potentially better radiation tolerance of transistors
- For certain applications - like large area strip sensors - H35 technology has some advantages: Cheaper production and better standard substrate. (20 Ωcm instead of 10 Ωcm)
- In 2015 we are planning at least two engineering runs: H35, for large pixels and strips and H18 for small pixels.
- Within these runs we will implement sensors on various substrates.

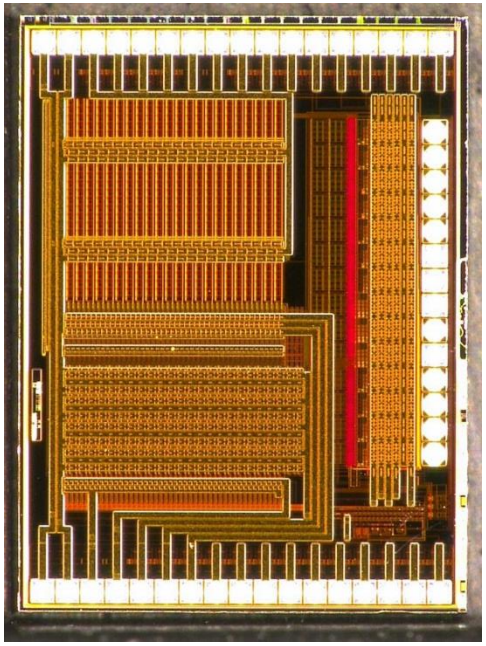
Collaborations

- The development of HVCMOS sensors is done within following collaborations
- Mu3e collaboration (Heidelberg, PSI, KIT, University and ETH Zuerich)
- ATLAS pixel HVCMOS collaboration (subset of the larger ATLAS CMOS collaboration)
- ATLAS Strip CMOS collaboration and KIT
- CLIC detector R&D group

HVCMOS pixels for strip layers in 350nm technology - experimental results

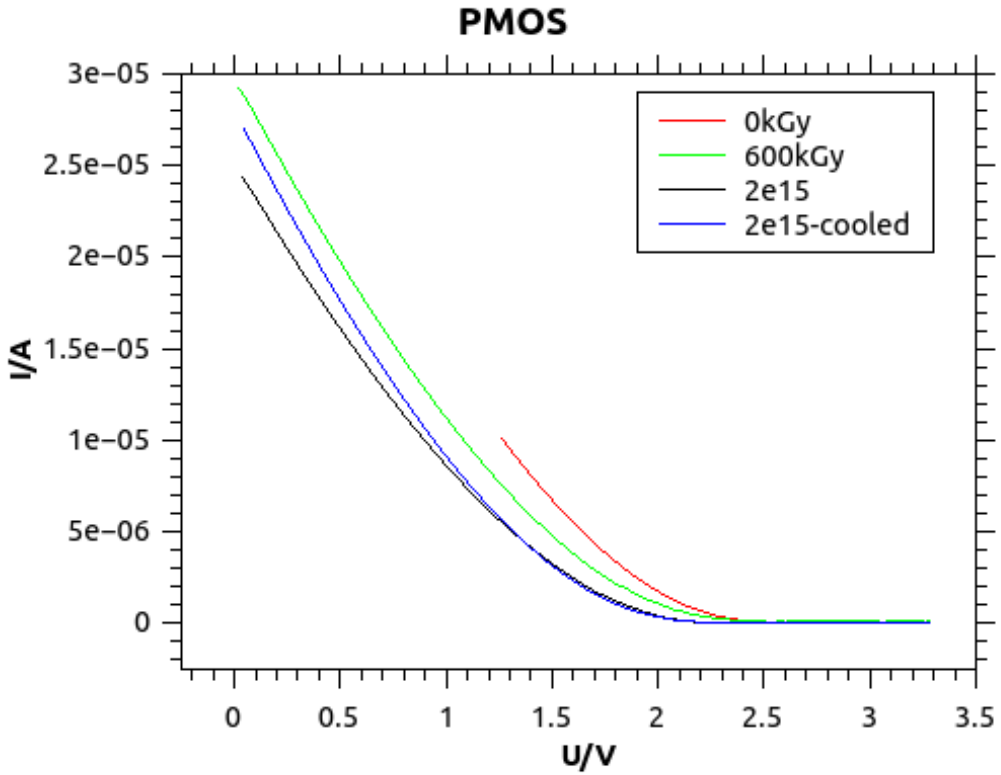
Test chip for strip layers HVStrip

- Measurements on CMOS strip test chip implemented in AMS 350nm technology - HVStripV1
- Pixel detector with long pixels. Pixel signals are transferred to the periphery where zero suppression and hit-address generation is done.
- We have not done efficiency measurement yet. We expect similar results as in the case of H18 detectors (see later)
- Here shown: Tests of radiation tolerance of the H35 technology at KIT, Karlsruhe



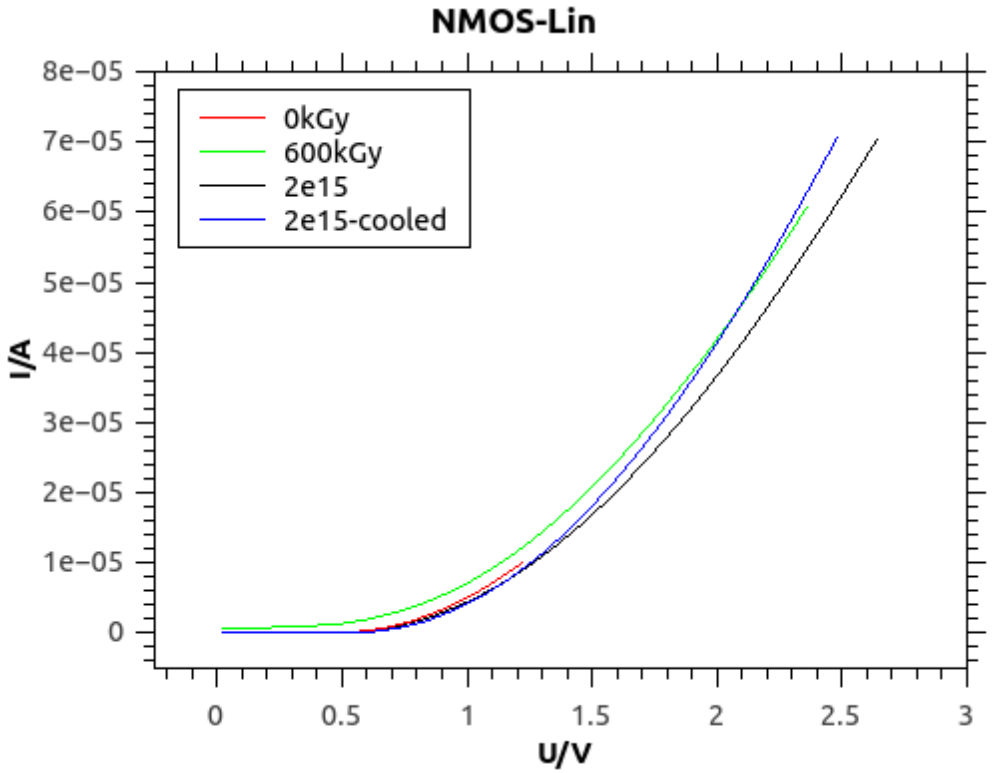
Single transistor measurements

- Single transistor measurements
- Ids vs Vgs characteristics of a PMOS transistor, before irradiation, after a dose of 60Mrad (X-ray irradiation) and after irradiation with protons (at KIT) to 2 10^{15} n_{eq} (probably 600 MRad)
- The PMOS transistors are radiation tolerant (no leakage current)



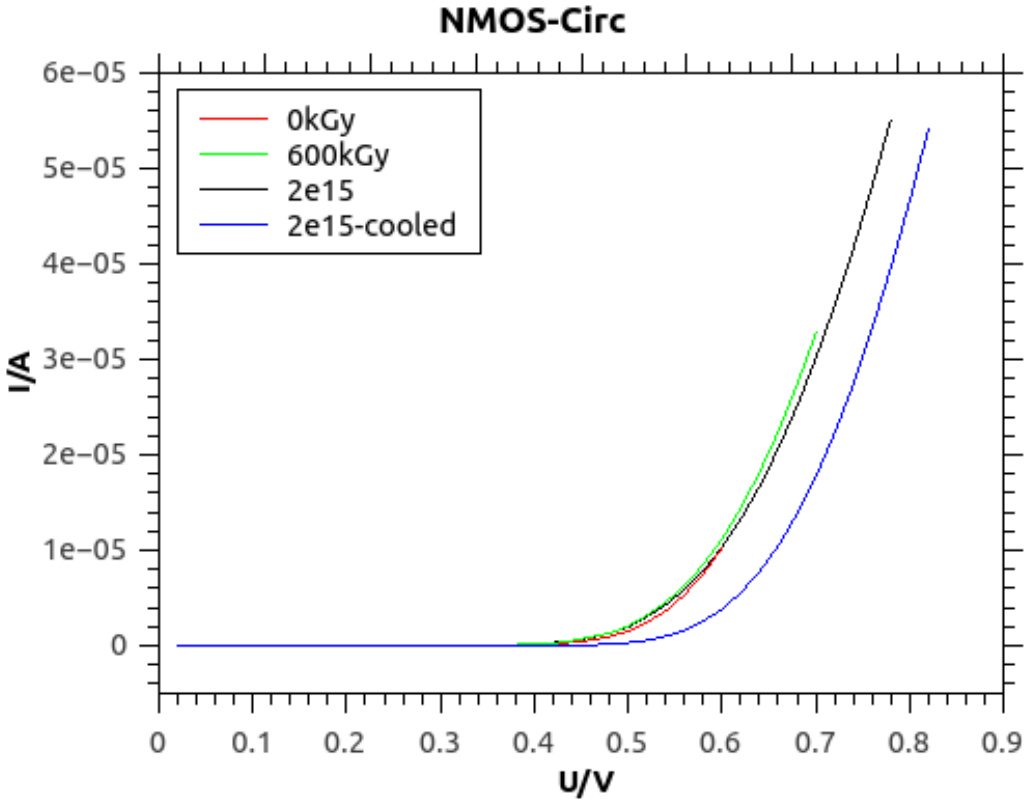
Single transistor measurements

- Ids vs Vgs characteristics of a standard linear NMOS.
- The NMOS has a leakage current of about 100nA after 60Mrad. This leakage current is not large and in most cases will not cause a problem (analog circuits).
- The measurement has been done after annealing – leakage current was larger in the dose range 1-10MRad (without annealing)



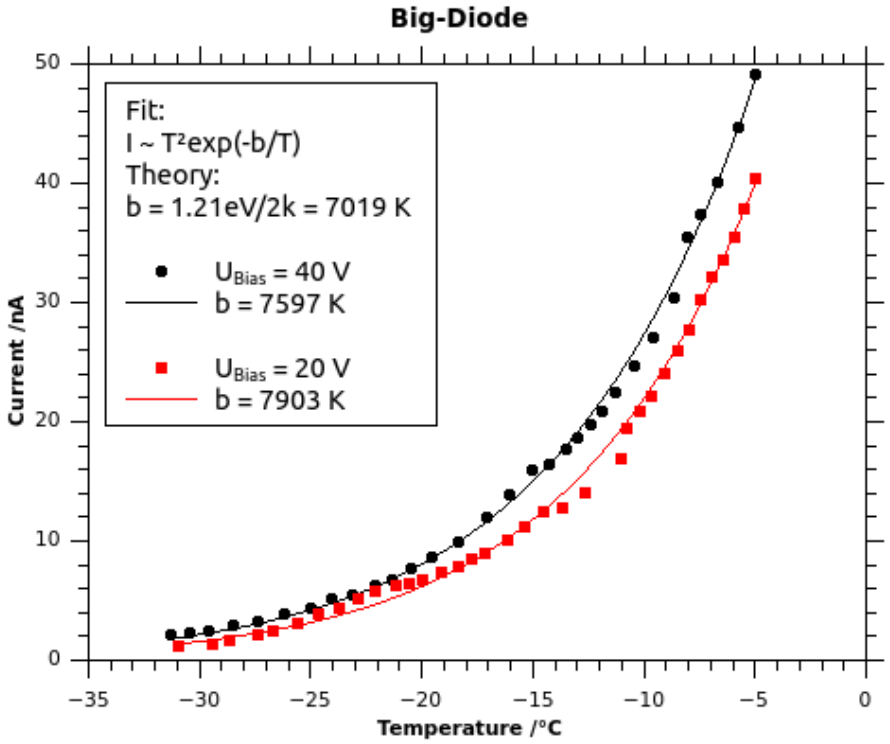
Single transistor measurements

- Ids vs Vgs characteristics of a enclosed NMOS.
- This device is radiation tolerant – no leakage current



Nonionizing irradiation effects in sensor

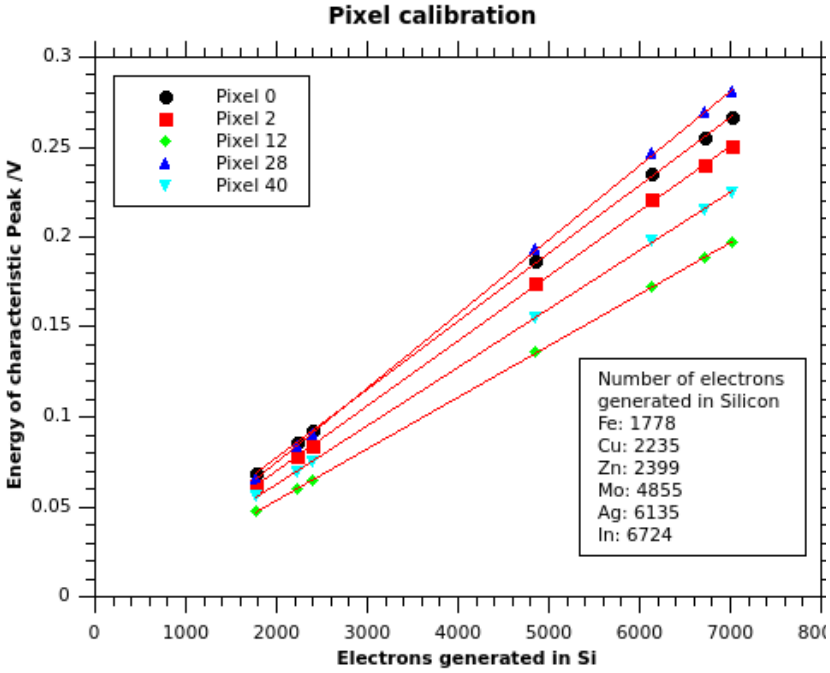
- We have also investigated the influence of irradiation to sensor diode.
- Results after irradiation with protons 2 10^{15} n^{eq}.
- Increased noise at room temperature.
- Test diode of the same size as the pixel diode for leakage current measurements.
- Leakage current increased after irradiation.
- Leakage current causes noise – this effect is well known and can be seen in simulation.
- Leakage current can be decreased by cooling to about 1nA at -30C – exponential dependence
- (Temperature of the chip not precisely known)



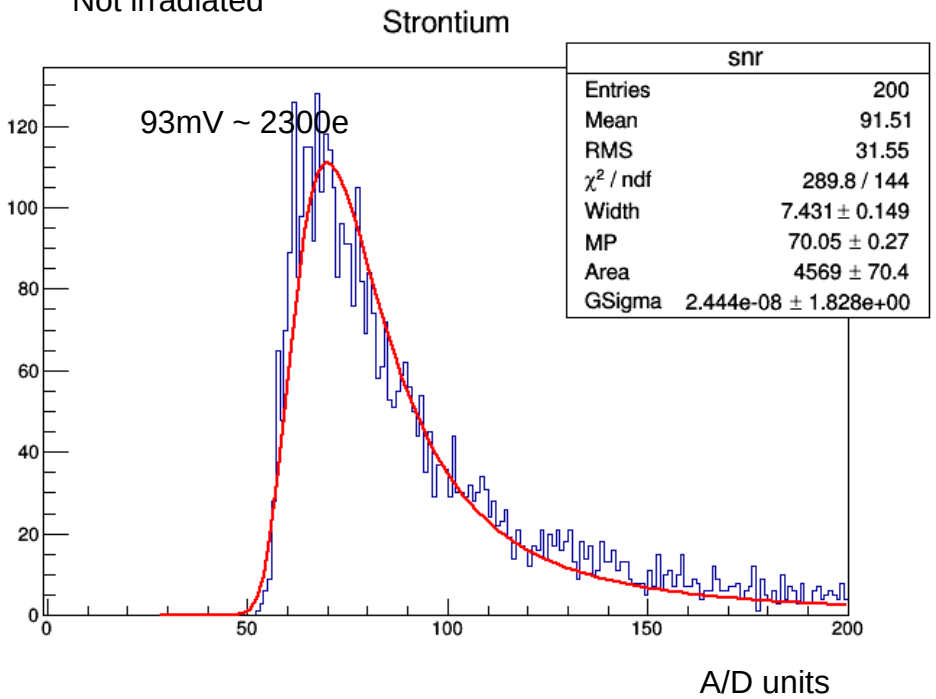
Nonionizing irradiation effects in sensor

- Before irradiation the beta signal (Sr90) was about 2300e. The result was obtained by comparing the amplitudes in the case of strontium illumination with the amplitudes we obtain when the illuminate the sensor with x-rays from different targets.

Calibration with x-rays



Strontium-90 illumination – spectrum
Not irradiated

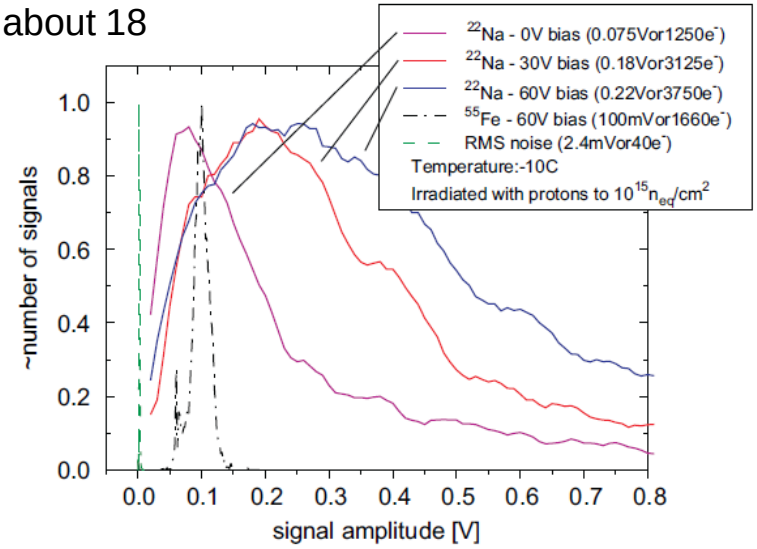


A/D units

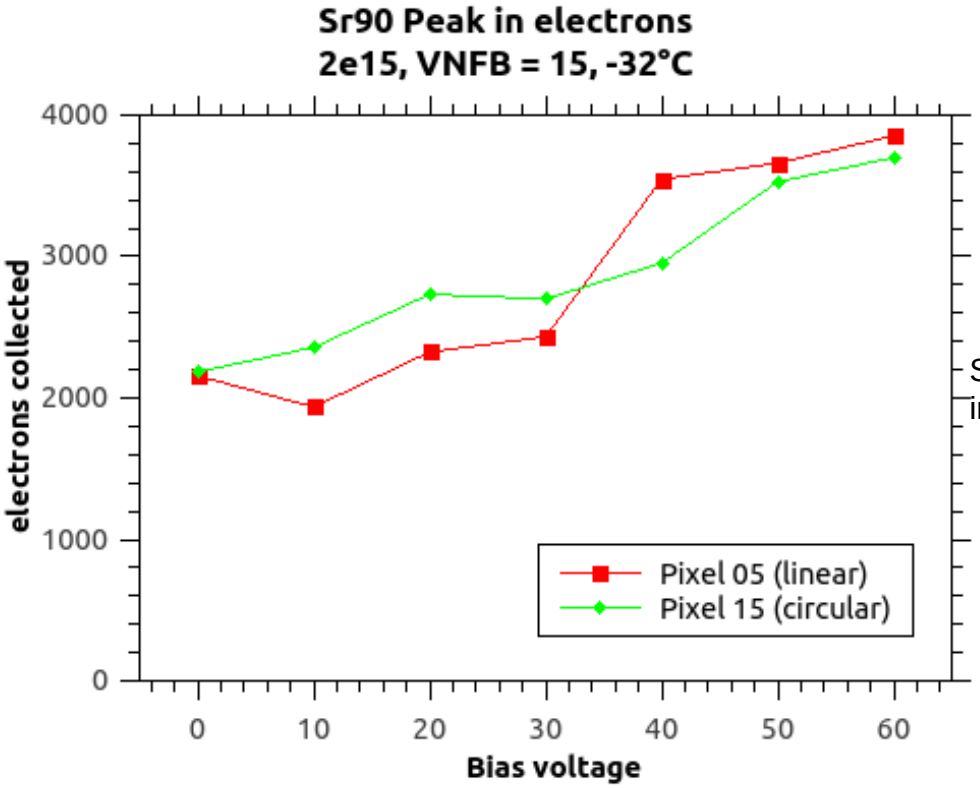
Nonionizing irradiation effects in sensor

- **After irradiation with protons 2 10^{15} n^{eq} the strontium signal is higher – it is up to 3800e.**
  This result was confirmed with a new calibration.
- Similar result has been measured in 2010
- Signal to noise ratio measured with injection circuit is about 18

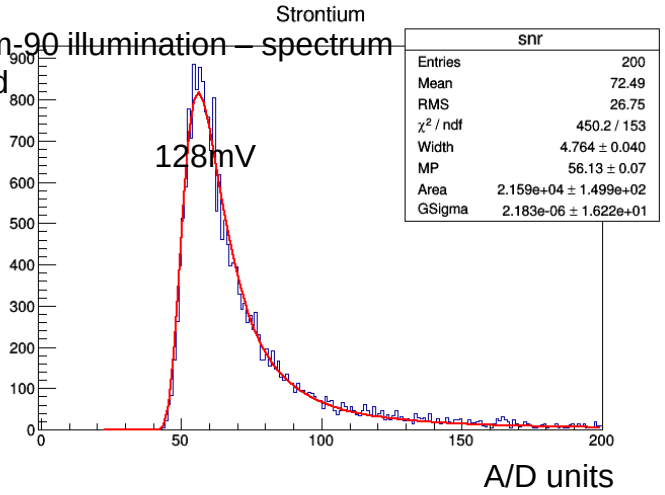
Old measurement on “capsens” detector



Strontium-90 illumination – spectrum irradiated



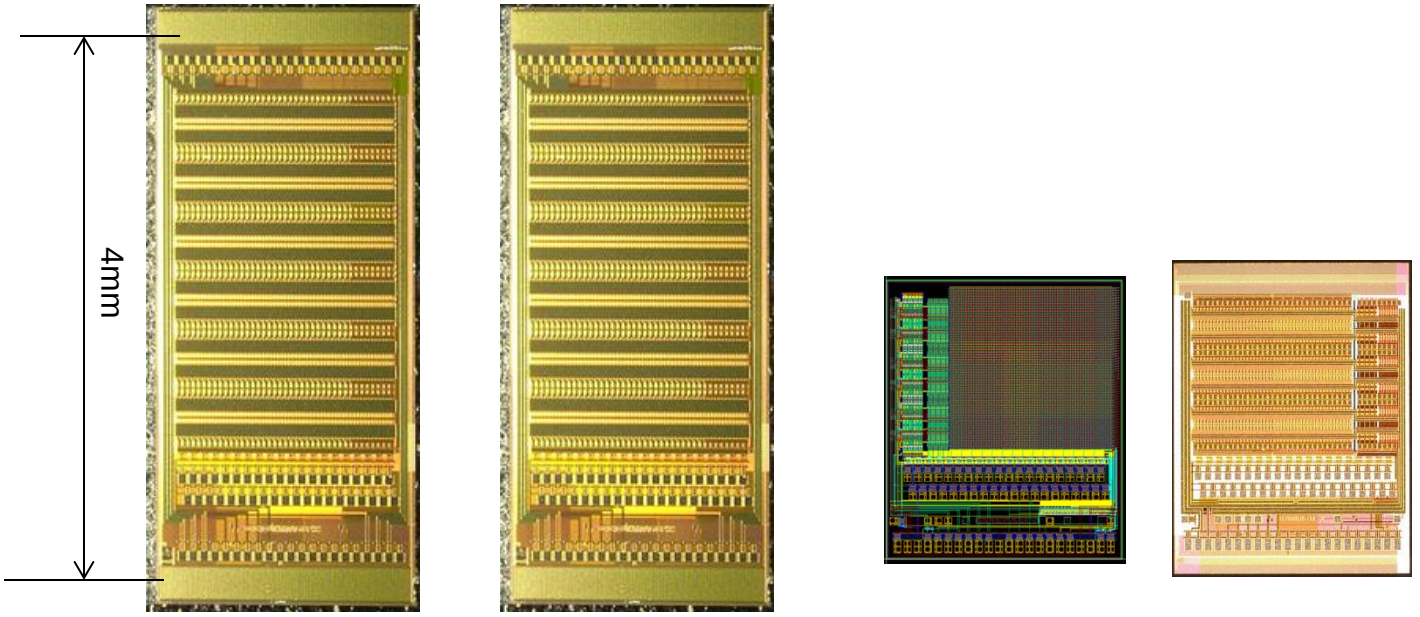
Strontium-90 illumination – spectrum irradiated



HVCMOS pixels for ATLAS in 180nm technology - experimental results

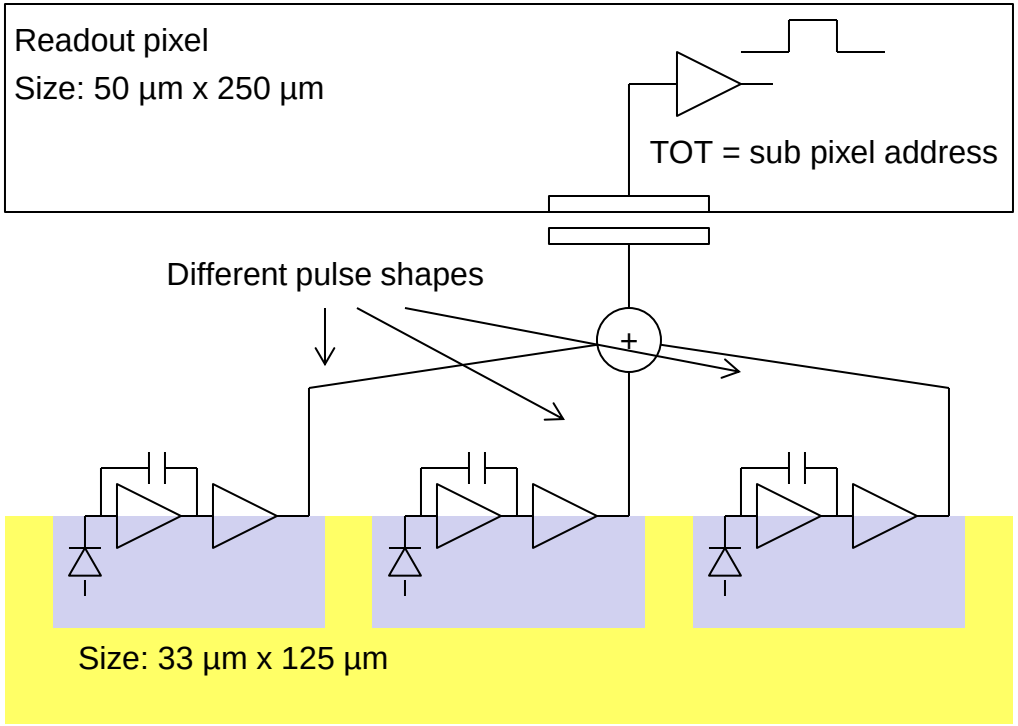
CCPD test-chips

- We present here HVCMOS detector-prototype for ATLAS pixels that has been implemented in H18 AMS technology
- Smart sensor readout by FEI4 – bumpless signal transmission CCPD
- The latest test chip is rather small – it contains several small pixel matrices with pixels of different types.



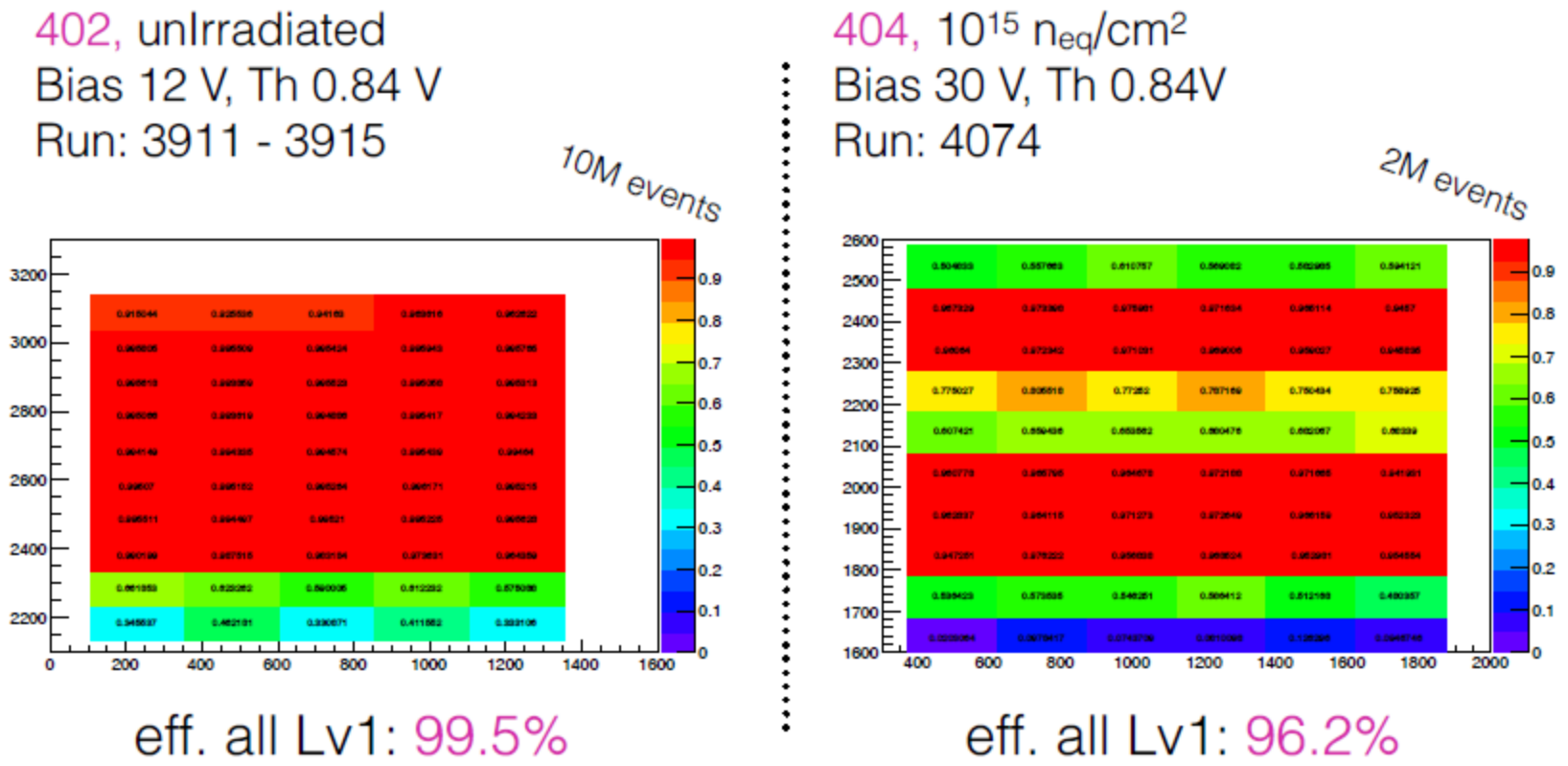
CCPDv1 CCPDv2 CCPDv3 CCPDv4

- The main pixel type employs the pixels with discriminators. Three pixels are grouped and coupled to one FEI4 channel. Digital comparator outputs are transmitted capacitively to the readout chip.
- We have also a smaller pixel matrix with analog pixels that do not have comparators.



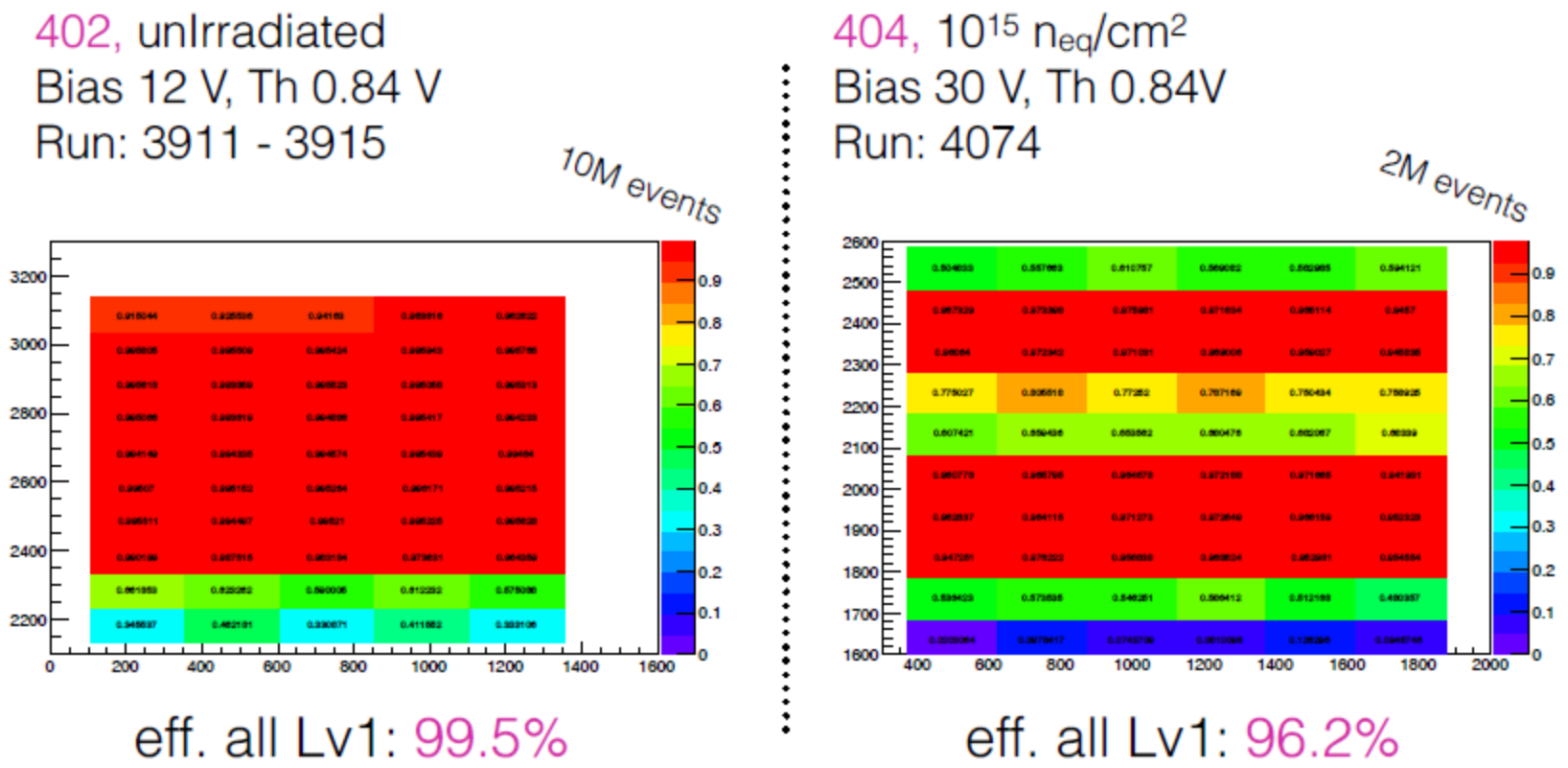
Test beam results

- University of Geneva group has done a test beam measurement in November 2014
- **99.5% detection efficiency** with the latest prototype (left). (Pixels with comparators.)
- The measurement has been done under suboptimal conditions – the bias voltage was only 12V.



Test beam results

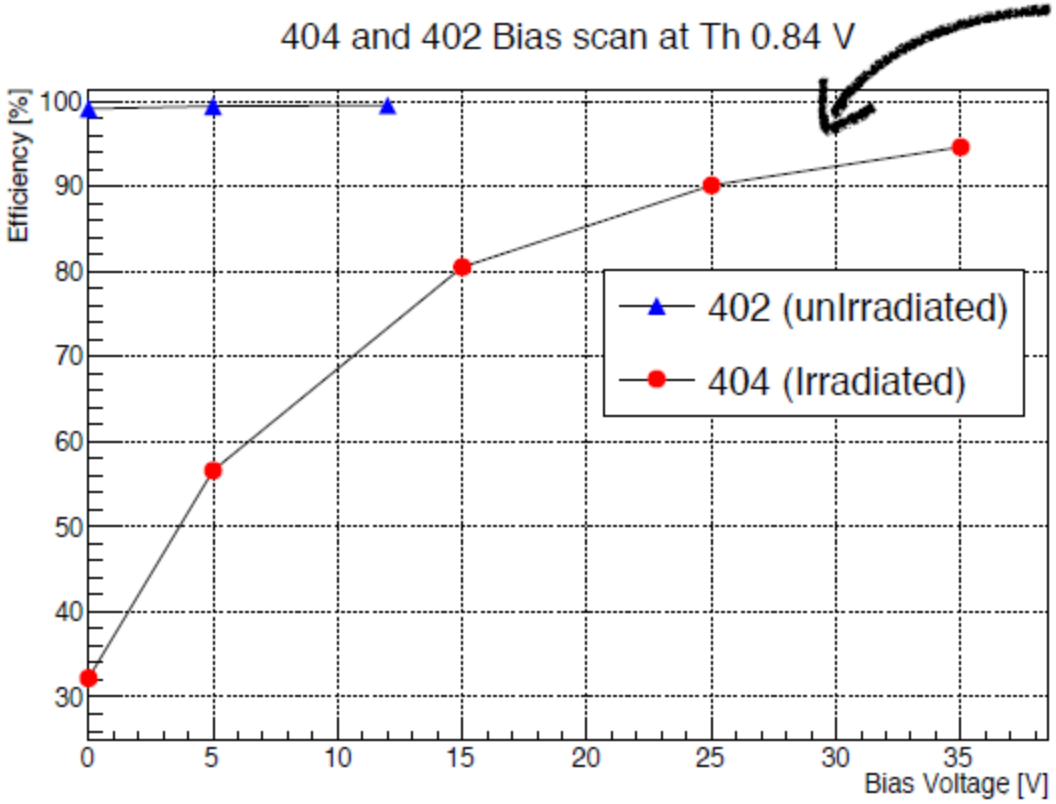
- Several chips irradiated with neutrons at Jozef Stefan institute in Ljubljana.
- Detection efficiency with an irradiated chip (fluence 10^{15} n_{eq}) 96% (right)
- Bias voltage was reduced – 35V



Efficiency of irradiated detector

- The efficiency increases when we increase the high voltage bias.
- Due to a damage it was not possible to increase the bias more than 35V

eff. for all Lv1:

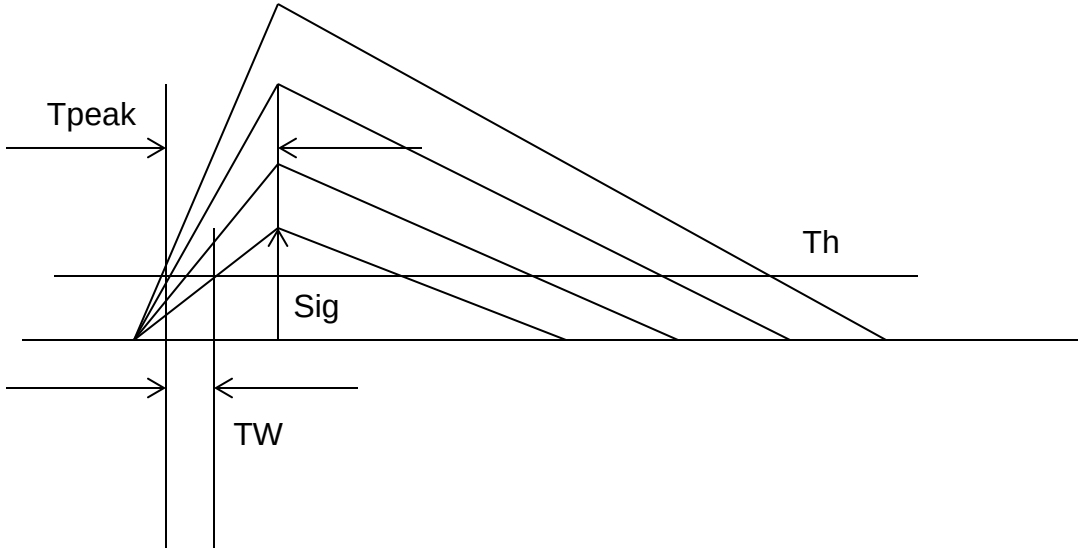


Need to reach the plateau

- There are several possibilities to improve the signal to noise ratio
- One is to examine which structure limits the bias voltage to ~80V. This is probably the guard ring around the N-wells. This guard ring is too close to the n-well and is in present designs shorted with the bias. We will leave it floating on the next test chip. We hope in this way to increase the maximum bias voltage, which should improve signal.
- Another possibility is to use high resistive substrates – we are planning an engineering run in H18 technology with this detector design.
- The capacitive signal transmission works well!!

Time resolution

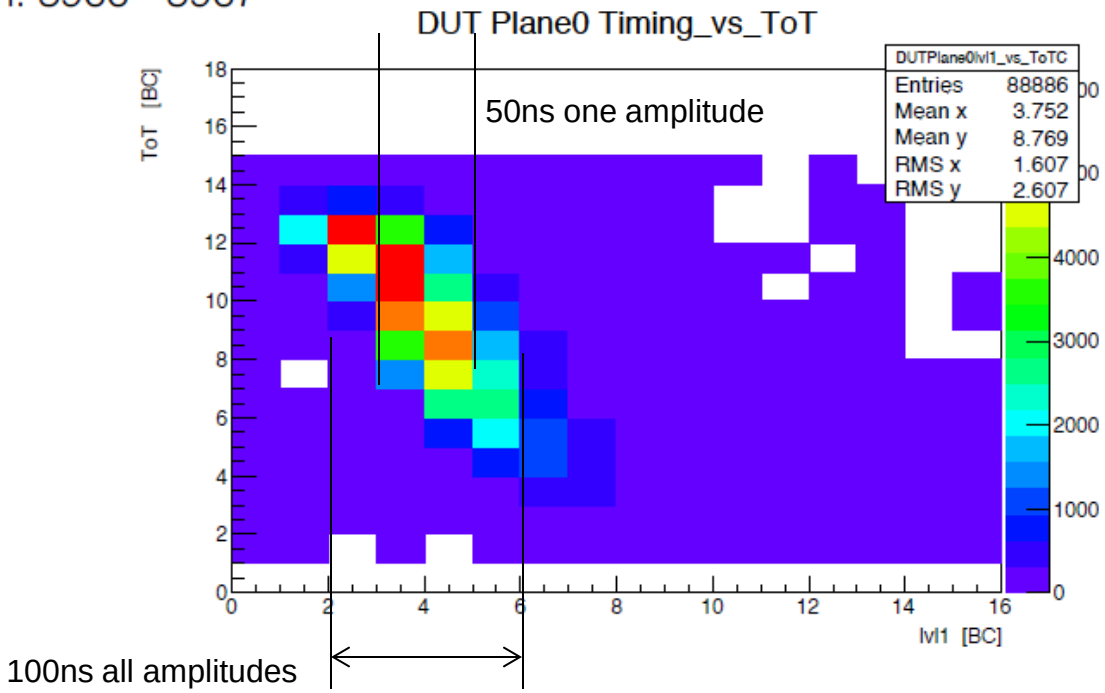
- Still not satisfactory:
- Time resolution was about 100ns – we need 25ns
- This time uncertainty is mostly caused by the time walk effect
- The problem is that the preamplifier is designed to have a peaking time > 100ns.
- The peaking time can be adjusted – in the test beam measurement the slow setting was used.
- Using of long peaking time allows us to operate the detector in low-power mode – long peaking time reduces noise for an equal bias current (power). However if the signal spread is large (landau distribution, we will have a time walk – time skew.

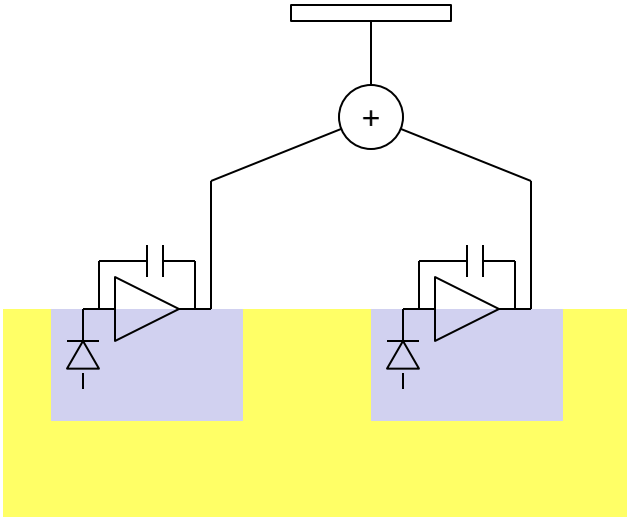


- There are a few way to improve time resolution
- One is to make the amplifier faster. This is possible, however it increases the noise. If we make amplifier faster we will probably need to increase the signal – which can be done by using high resistive substrate.
- More elegant way to improve the timing - compensation
- Bases of the fact that the time walk is proportional to the signal amplitude

- Several pixels with analog output – the signal they produce in FEI4 is proportional to the input charge signal.
- If we plot the arrival time vs the TOT (charge amplitude) we see a clear dependence. This means for certain amplitude the time walk is smaller that when we consider all the amplitudes. It is of the order of 50ns. This means that if we use the amplitude information we can correct for time walk.

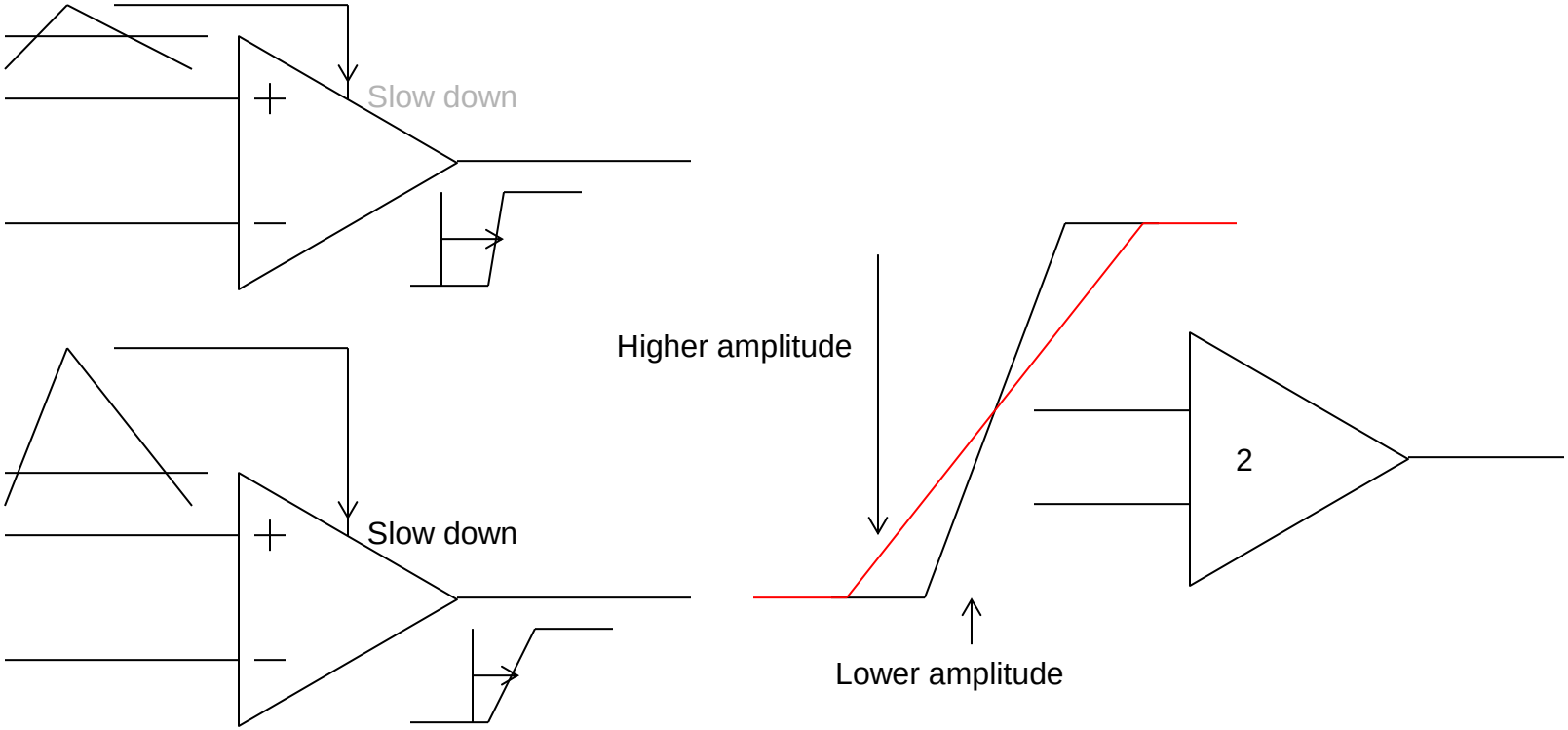
402, unIrradiated
Bias 12 V, Th 0.84 V
Run: 3966 - 3967





Time walk compensation

- We have implemented on the test chip a time walk compensating comparator. Its rise time is longer for signal with high amplitudes. This means a signal with higher amplitude has a faster threshold crossing, but the comparator output is slower.
- A signal with lower amplitude has a later threshold crossing but the comparator output is faster. As consequence of this the comparator outputs for all amplitudes can cross in one point. By adding another comparator we can make the response time independent of amplitude.



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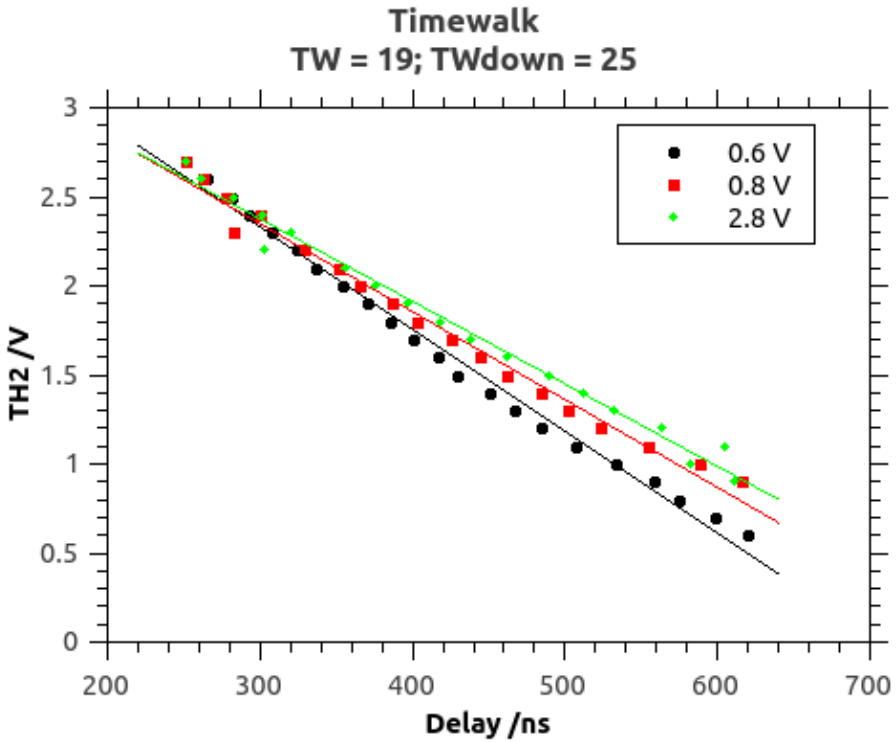

- Finally I will mention the development for CLIC. We have here 25 x 25um pixels on HVCMOS. The sensor is capacitivelly coupled to the CLIC pix ASIC. Test beam has been done – the detection efficiency is better than 99%.
- The pixels on the CLIC HVCMOS contain only amplifiers – the output is analog.
- Similar results are achieved with Mu3e sensors as well.

Summary

- We are developing sensors for LHC strips, pixels CLIC and Mu3e
- We have the following structures:
- CCPD for ATLAS pixels - the HVCMOS sensor is readout by FEI4 chip
- Monolithic sensors for ATLAS (or CMS) strips and Mu3e – the readout parts are on the periphery of the sensor chip
- CCPD with small pixels for CLIC
- **We measure 99% efficiency for ATLAS pixels, CLIC, Mu3e**. The strip detectors will be tested soon
- After irradiation 10^{15} n_{eq} we measure efficiency of >95% (preliminary, suboptimal settings)
- We are planning engineering runs in AMS H35 and H18 technologies that will bring us the possibility to test different substrate resistances and improve SNR
- For the strip project we are using H35 technology
- For the pixel project we are using both technologies: for inner pixels H18 and for outer pixels H35
- Irradiation results on H35 test detector have been shown
- Enclosed NMOS and PMOS transistors are radiation tolerant – no leakage current after irradiation with x-rays (60MRad) and with protons (2×10^{15} n_{eq})
- We measure **increased beta-particle signal (Sr-90) after irradiation with protons** (2×10^{15} n_{eq})
- The signal is 3800e

- Thank you