Analog circuit design in 65 nm CMOS for the readout of silicon pixel detectors

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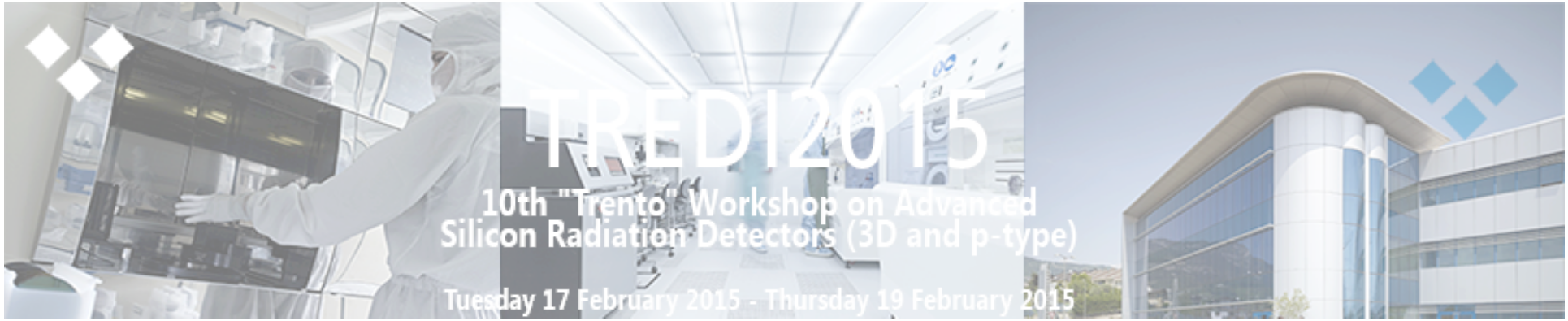


Analog front-end and mixed-signal 65 nm CMOS integrated circuits for pixel sensors

- 65 nm CMOS has attracted a wide interest in view of the design of very compact front-end systems with advanced integrated functionalities, such as required by semiconductor pixel sensors with low pitch for applications in high energy physics (silicon vertex trackers) and photon science experiments (high resolution imagers)

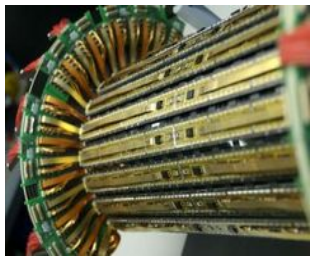
- Digital figures of merit (speed, density, power dissipation) are driving the evolution of CMOS technologies. What about analog performance?

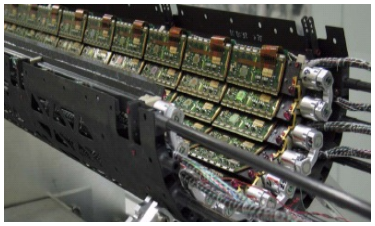
- For **analog applications** in which **speed and density** are important, scaling can be in principle beneficial, but what about critical performance parameters such as **noise, gain, radiation hardness…?**

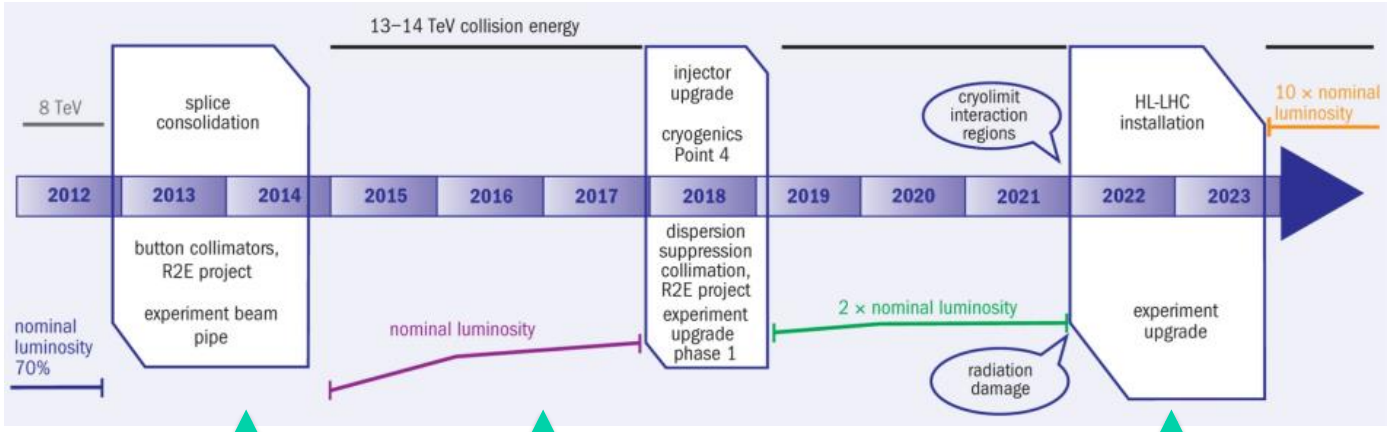
- This talk will focus on the design of the **analog section of the readout chips for the innermost layers of the pixel detectors for the phase-II upgrade** of ATLAS and CMS at LHC

LHC pixel upgrades

- Current LHC pixel detectors have clearly demonstrated the feasibility and power of pixel detectors for tracking in high rate environments
- Phase1 upgrades: Additional pixel layer, ~4 x hit rates
  - ATLAS: Addition of Inner B Layer (IBL) with new 130nm pixel ASIC (FEI4)
  - CMS: New pixel detector with modified 250nm pixel ASIC (PSI46DIG)
- **Phase2 upgrades**: ~16 x hit rates, ~4 x better resolution, 10 x trigger rates, 16 x radiation tolerance, Increased forward coverage, less material, , ,
  - Installation: ~ 2022
  - Relies fully on significantly improved performance from next generation pixel chips.







ATLAS Pixel IBL

CMS Pixel phase1

CMS & ATLAS phase 2 pixel upgrades

100MHz/cm^2

400MHz/cm^2

1-2GHz/cm^2

Advanced pixel detectors and readout microelectronics

Particle tracking at LHC- Phase II

- Very high hit rates (1-2 GHz/cm^2), need of an intelligent pixel-level data processing
- Very high radiation levels (1 Grad Total Ionizing Dose, 10^{16} neutrons/cm^2)
- Small pixel cells to increase resolution and reduce occupancy (~50x50μm^2 or 25x100 μm^2)

➔ **Large chips: > 2cm x 2cm, ½ - 1 Billion transistors**

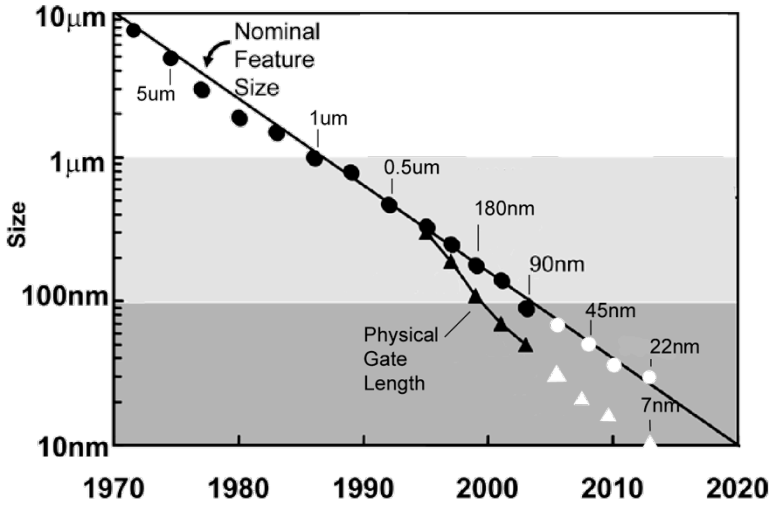
Another field where 65 nm CMOS can provide a solution to demanding requirements: X-ray imaging at free electron laser facilities

- Reduction of pixel size (100x100 μm^2 or even less), presently limited by the need of complex electronic functions in the pixel cell
- Larger memory capacity to store more images (at XFEL, ideally, 2700 frames at 4.5 MHz every 100 ms)
- Advanced pixel-level processing (1 – 10000 photons dynamic range, 10-bit ADC, 5 MHz operation)

Low Power 65 nm CMOS

- Mature technology:
  - Available since ~2007
- High density and low power
  - High density vital for smaller pixels and increased data buffering during bunch trains
  - Low power tech critical to maintain acceptable power for higher pixel density and much higher data rates
- Long term availability
  - Strong technology node used extensively for industrial/automotive
- Significantly increased density, speed, and complexity compared to previous generations!

- **Access: CERN frame-contract with TSMC and IMEC**
  Design tool set, Shared MPW runs, Libraries, Design exchange within HEP community

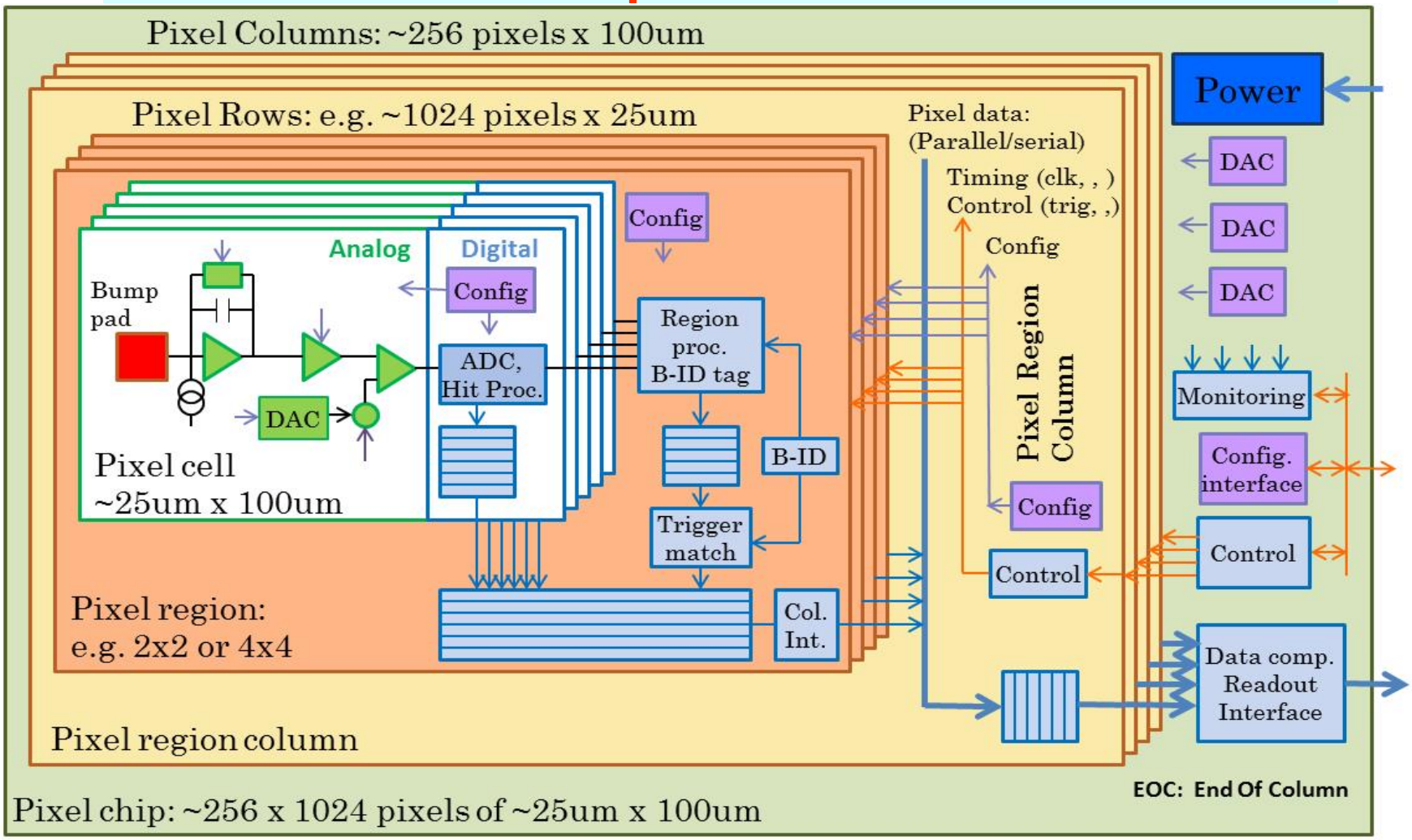


The **Low Power (LP)** flavor (V_{DD} = 1.2 V) is less aggressive than other variants of the process (thicker gate oxide, smaller gate current, higher voltage), and more attractive for mixed-signal chips where analog performance is an essential feature.

The RD53 collaboration

- Similar/identical requirements for ATLAS AND CMS pixel readout chips, same technology choice **(CMOS 65 nm)** and limited availability of rad hard IC design experts in HEP makes this ideal for a close CMS – ATLAS R&D collaboration
  - Even if we do not make a common pixel chip
- Forming an R&D collaboration has attracted additional groups and collaborators
  - Synergy with CLIC pixel (and others): Technology, Rad tol, Tools, etc.
- RD53 collaboration recommended by LHCC June 2013
  - Institutes: 19
    - ATLAS: CERN, Bonn, CPPM, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Prague, RAL, UC Santa Cruz.
    - CMS: Bari, Bergamo-Pavia, CERN, Fermilab, Padova, Perugia, Pisa, PSI, RAL, Torino.
  - Collaborators: ~100, ~50% chip designers
  - Collaboration organized by Institute Board (IB) with technical work done in specialized Working Groups (WG)
  - Initial work program covers ~3 years to make foundation for final pixel chips
  - Co-spokespersons: ATLAS: M. Garcia-Sciveres, LBNL. CMS: J. Christiansen, CERN
- RD53 web: www.cern.ch/RD53/

RD53 chip architecture



- 95% digital (as for FEI4)
- Charge digitization (TOT or ADC)
- ~256k pixel channels per chip
- Pixel regions with buffering
- Data compression in End Of Column
- Chip size: >20 x 20 mm^2

Analog design in nanoscale CMOS for advanced pixel detectors

- The **Analog Working Group of RD53** is studying the best design choices for the front-end stages, that interface the silicon sensor with the large and mostly digital readout chip
- Severe constraints for noise, power, speed, silicon area, immunity to digital interferences have to be taken into account in the classical analog blocks (preamplifier, discriminator,…)
- Scaling of transistor size to the nanometer region also stimulates analog design ideas that depart from the usual schemes of pixel front-end circuits, going beyond a simple translation of old schematics into a more advanced technology. Among them:
  - ❑ Switched-capacitor techniques
    (avoid local tuning in the pixel cell and additional hardware)
  - ❑ Fully differential architectures
    (increase immunity to interferences)
  - ❑ Current-mode schemes
  - ❑ …..

Critical technology features for pixel analog front-end design in 65 nm CMOS

- There are various technology features that analog designers have to take into account for a high performance pixel front-end in a nanoscale CMOS process:
  - Intrinsic gain
  - Thermal noise

  } Charge carriers in the device channel (short channel effects, strained silicon)

  - Gate leakage current
  - 1/f noise

  } Interaction of charge carriers with the gate oxide; tools for evaluating the quality of the gate dielectric

  - Radiation hardness

  } Radiation-induced positive charge in the gate oxide and in lateral isolation oxides

  - Device matching

  } Random components of local process parameters dependent on device size

Interfacing the 65 nm readout chip with a pixel sensor

- The features of the pixel sensors have an obvious impact on the design of the readout chip.
- Choices will be driven by physics needs, radiation tolerance, cost,…
- The pitch of pixel readout cells will also be dependent on the available interconnection technology, which brings along many other features and constraints (minimum pitch and height of bumps, minimum sensor thickness,…)
- Among essential specifications for the design of the analog front-end:
  - **pixel capacitance** → noise in the preamplifier
  - **leakage current** → compensation circuit in the preamp feedback
  - **collected charge** → hit discriminator threshold → noise, mismatch,…

Sensor parameters and the analog front-end: the pixel capacitance

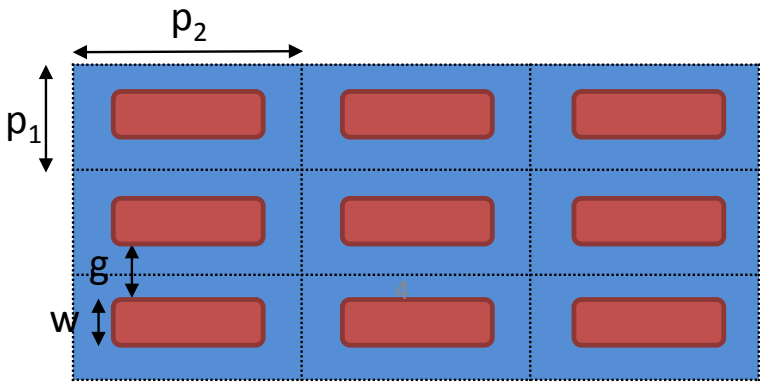
- Sensor design choices for the pixel geometry impact on the pixel capacitance. For planar sensors (analogous for 3D):

  pixel pitch

  pixel perimeter

  gap between implants

  .....



- This is a crucial parameter for analog designers optimizing noise, power, speed of the preamplifier.

- The current assumption is that the typical pixel capacitance C_D is 100 fF (including parasitics, i.e. strays between bumps), maximum 150 fF.

Specifications for threshold setting, noise, power, speed in the ATLAS/CMS RD53 pixel analog front-end

Need of **detecting charge released by MIPs in heavily damaged sensors (4000 e-) at extreme irradiation levels without efficiency degradation**

- Threshold setting for higher tolerable noise occupancy: $Q_{th,min}$ = 1000 e-
- ENC < 150 e rms at C_D = 100 fF (mostly determined by series noise, ENC is proportional to C_D)
- Threshold dispersion after local tuning: σ_{Qth} < 40 e rms

  (includes contributions by discriminator threshold mismatch and pixel-to-pixel preamplifier gain variations)

These specifications are based on the so called 4σ rule (empirical): $Q_{th,\,min} > 4 \cdot ENC + 4 \cdot \sigma_{Qth}$. They have to be achieved by analog circuits integrated in **a small silicon area** and operating at **very low power**:

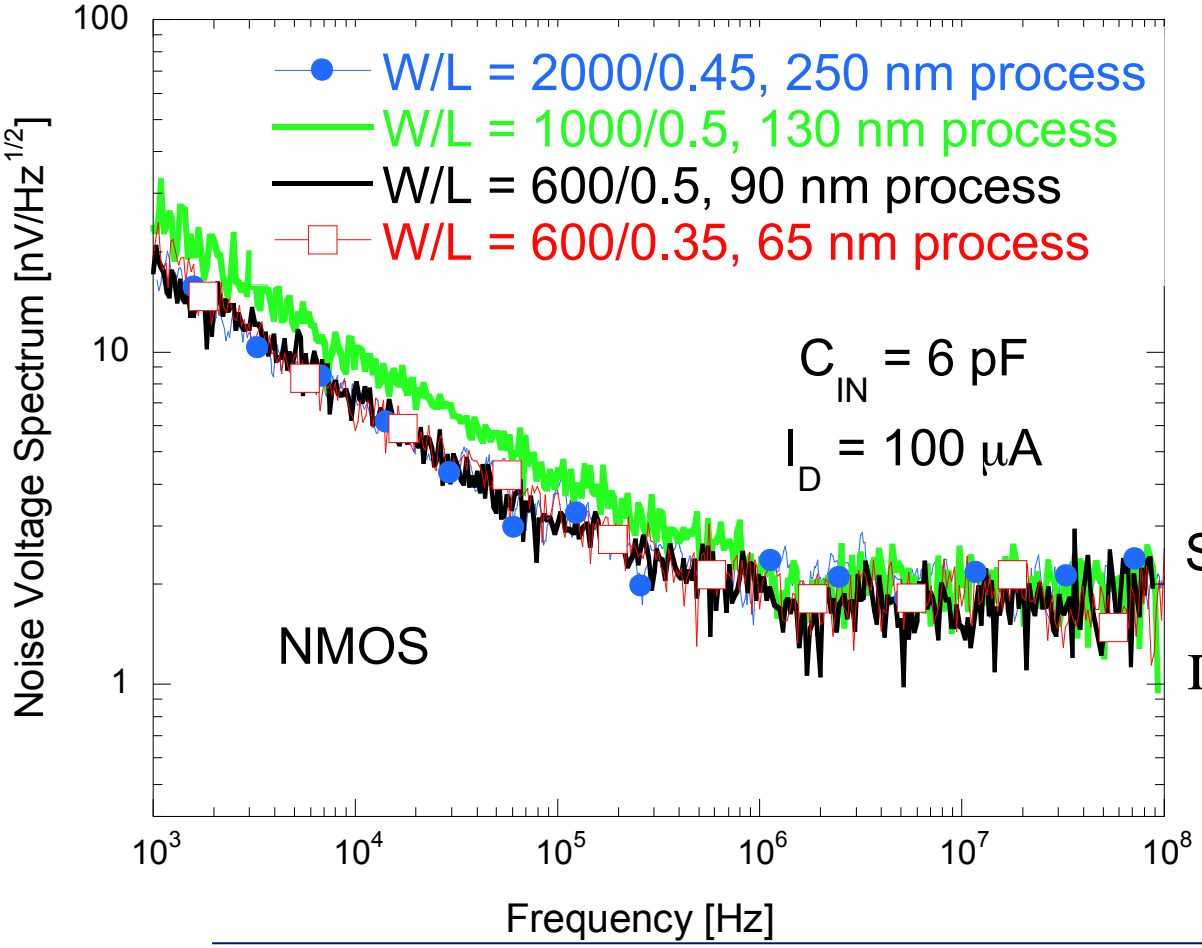
- Maximum power dissipation: 6 μW/pixel

(50 μm x 50 μm, or 25 μm x 100 μm)

- Maximum Hit time resolution = 25 ns, A/D conversion time < 400 ns

Noise in NMOS: CMOS generations from 250 nm to 65 nm

- 1/f noise has approximately the same magnitude (for a same WLC_{OX}) across different CMOS generations. White noise has also very similar properties (weak/moderate inversion).



1/f noise

$$S_{1/f}^2(f) = \frac{K_f}{C_{OX}WLf^{\alpha_f}}$$

- k_f 1/f noise parameter
- α_f 1/f noise slope-related coefficient

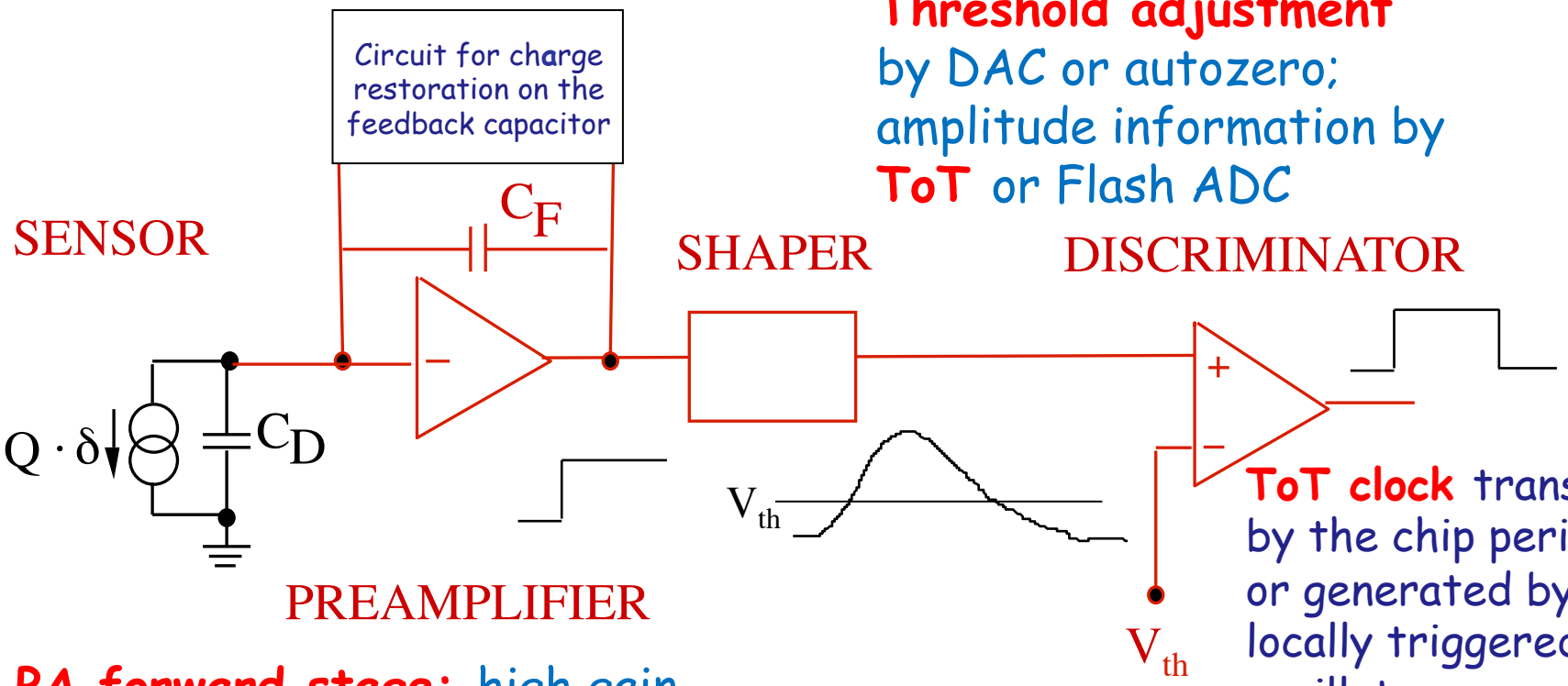
Channel thermal noise

$$S_W^2 = \frac{4k_BT\Gamma}{g_m}, \qquad \Gamma = \alpha_W n\gamma$$

- k_B Boltzmann's constant
- T absolute temperature
- α_w excess noise coefficient
- γ channel thermal noise coefficient

In weak inversion: $g_m = \frac{I_D}{nV_T}$

General schematics of a pixel analog front-end in 65 nm CMOS



Threshold adjustment by DAC or autozero; amplitude information by **ToT** or Flash ADC

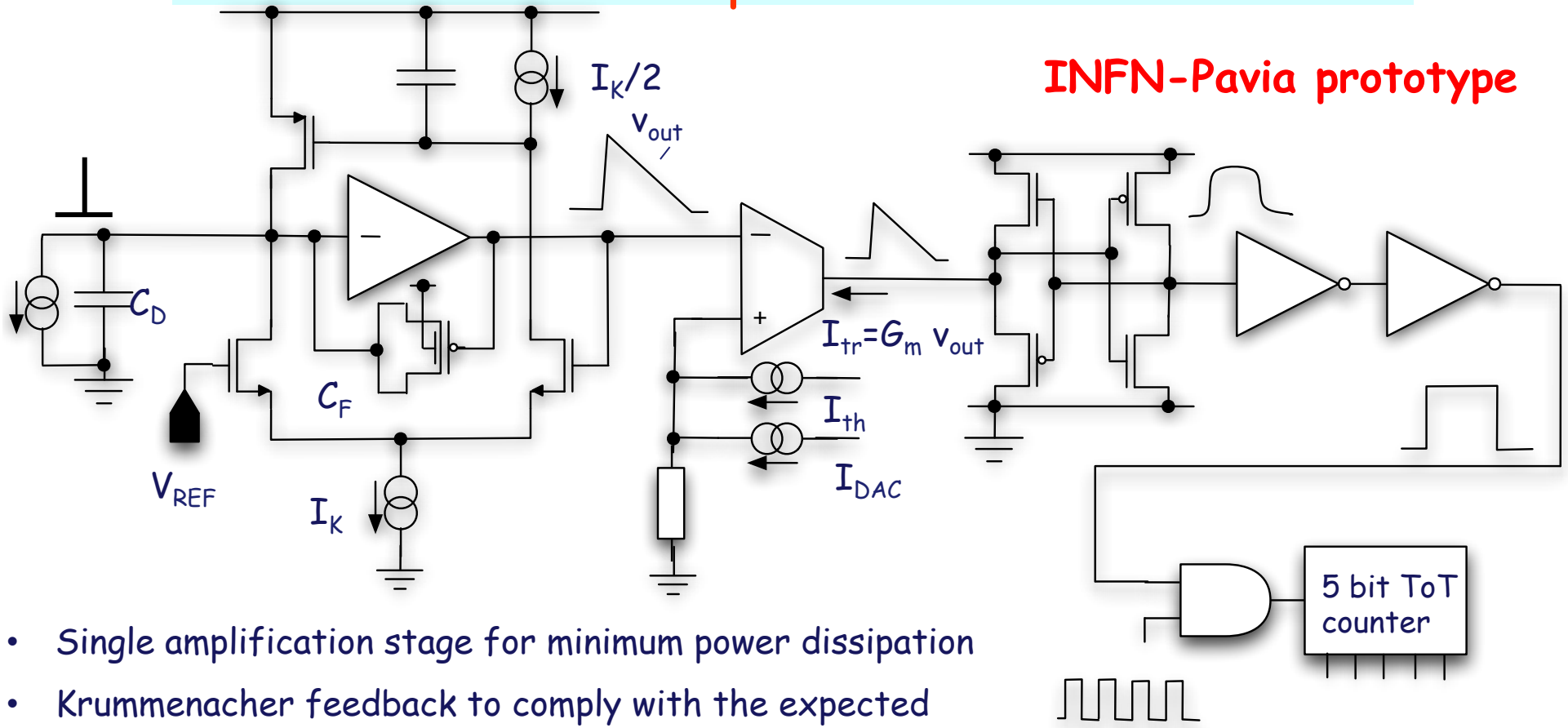
ToT clock transmitted by the chip periphery, or generated by a locally triggered oscillator

PA forward stage: high gain, low noise

Charge restoration: handle sensor leakage current after extreme irradiation levels (max. 20 nA at 2×10^{16} n/cm^2)

Trend is to **skip the shaping stage** in the RD 53 HL-LHC pixel cell, mostly because of power constraints (noise filtering in the preamplifier, or correlated double sampling)

How the analog channel may look like in a HL-LHC pixel readout



- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- High speed, low power current comparator
- Relatively slow ToT clock – 80 MHz
- 5 bit counter – 400 ns maximum time over threshold

- 30000 electron maximum input charge, ~450 mV preamplifier output dynamic range
- Selectable gain and recovery current

Designing amplifiers in 65 nm CMOS: the intrinsic gain

- It represents **the maximum gain that can be achieved with a single transistor amplifying stage**. It gives an indication concerning the design complexity that is necessary to implement a high gain amplifier.

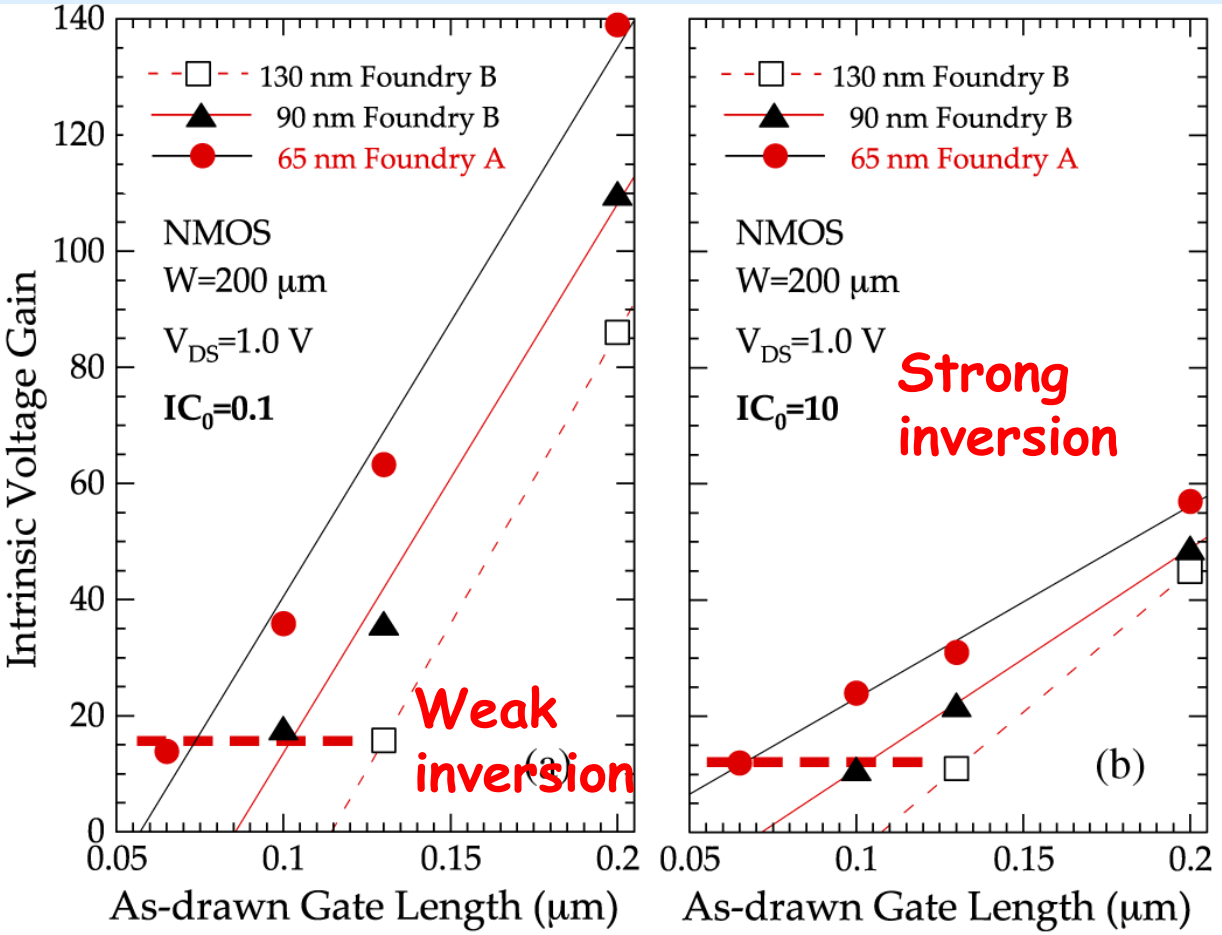
- Keeping the intrinsic gain constant with scaling below the 100 nm threshold (when you depart from classical scaling rules in advanced technologies) is considered as a major challenge which affects the design of analog circuits in nanoscale CMOS

- But Low Power CMOS processes do not follow aggressive scaling trends closely…

➔ **The value of the intrinsic gain is maintained across different CMOS technology nodes from 130 nm to Low Power 65 nm if inversion conditions are the same.**

Intrinsic gain in the LP 65 nm CMOS

When the gate length L is reduced, the transistor stays in the same inversion conditions if the drain current I_D is correspondingly increased (at constant W).



M. Manghisoni, et al. "Assessment of a Low-Power 65 nm CMOS process for analog front-end design", IEEE Trans. Nucl. Sci., vol. 61, no. 1, February 2014, pp. 553-560.

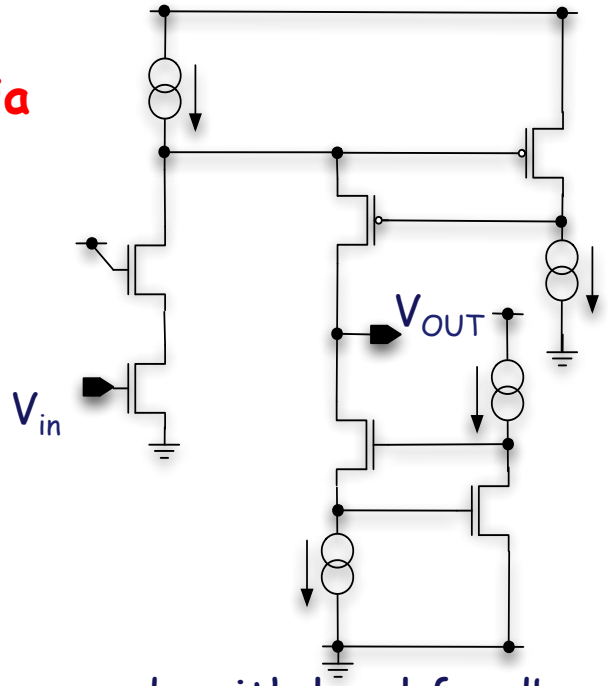
For the minimum gate length of the process, the same value of the intrinsic gain is achieved at the expense of an increased I_D. If this is not allowed because of power dissipation constraints, a value of L larger than the minimum one has to be used.

This is an example of the fact that **in analog circuits it is often impossible to take full benefit from CMOS scaling in terms of a reduced silicon area.** This is true also for other analog parameters (1/f noise, threshold dispersion,…)

Gain stages

- The good intrinsic gain properties of the LP 65 nm process make it possible to design amplifier stages with relatively simple schematics and an adequate forward gain in a low-power pixel front-end.

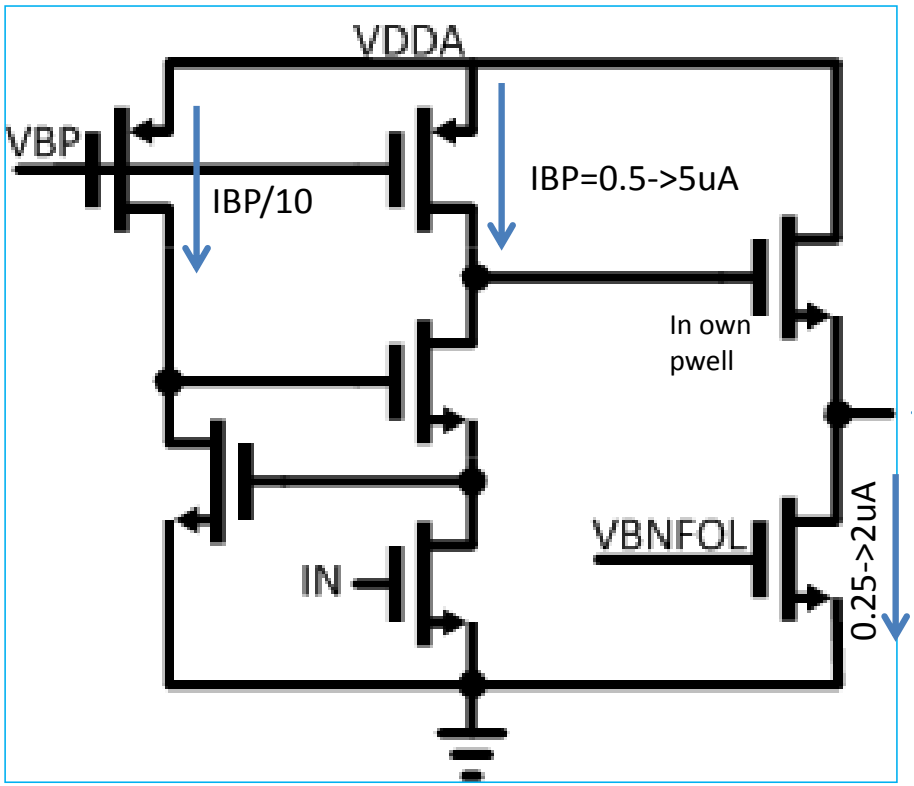
INFN-Pavia prototype



- Folded cascode with local feedback and active load
- Input device: W/L=9 μm/0.1 μm
  Power dissipation: ~3.6 uW

Low frequency gain ~100 dB, gain-bandwidth product 140 MHz

LBNL design

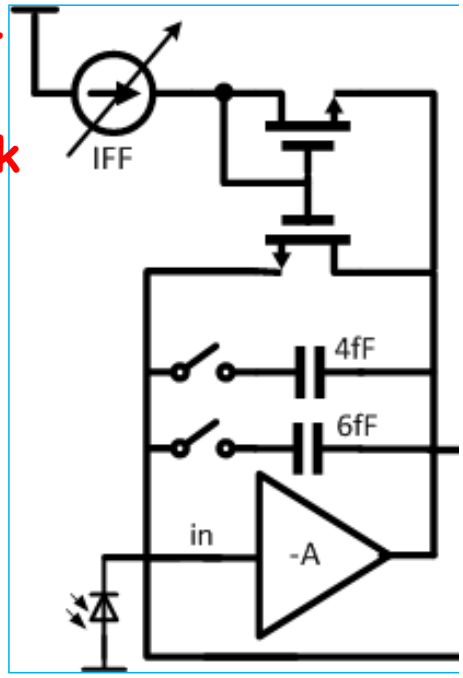


Gain stage with active cascode

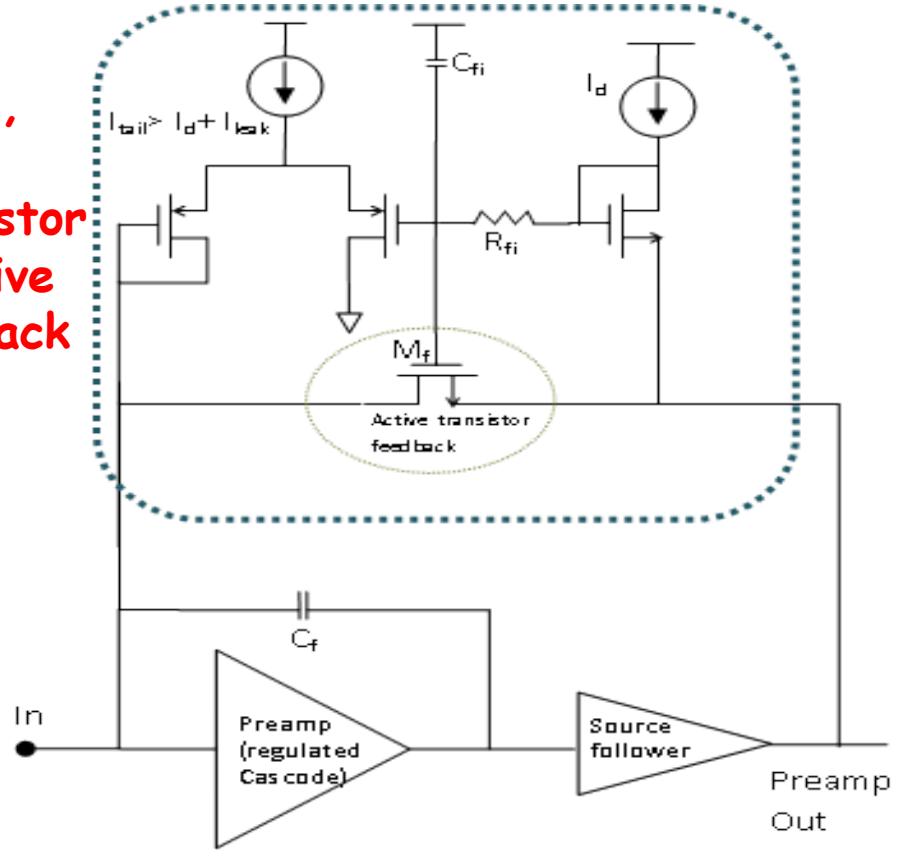
Preamplifier feedback and compensation of sensor leakage current

- Several schemes for the feedback network are being proposed and studied (Krummenacher feedback, current mirror constant current feedback, active transistor resistive feedback)
- Presently, the spec is 20 nA max leakage at $2 \cdot 10^{16}$ n/cm^2

LBNL design, constant current feedback



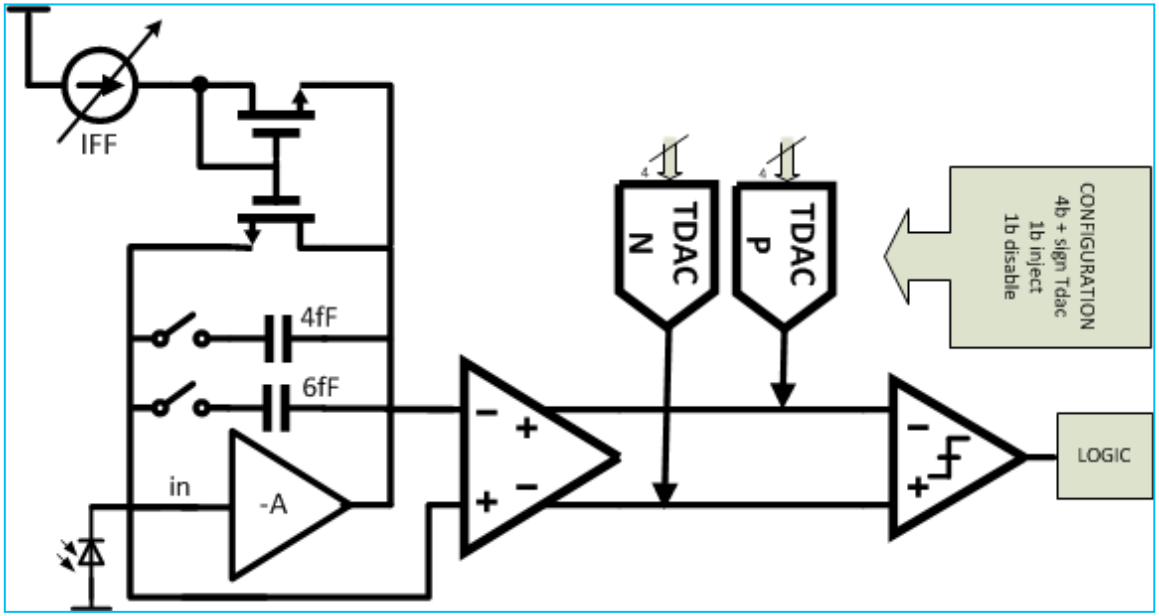
FNAL design, active transistor resistive feedback



Analog channel in the pixel readout cell: asynchronous or synchronous?

- The classical continuous-time analog processing channel is a well-established solution for pixel sensors in high-energy physics
- To reduce power (and area), this channel includes just two stages (charge-sensitive preamplifier + asynchronous comparator), and A/D conversion may be based on a time-over threshold measurement.

LBNL design, 2-stage continuous-time comparator (PA input used as reference in 1° stage)

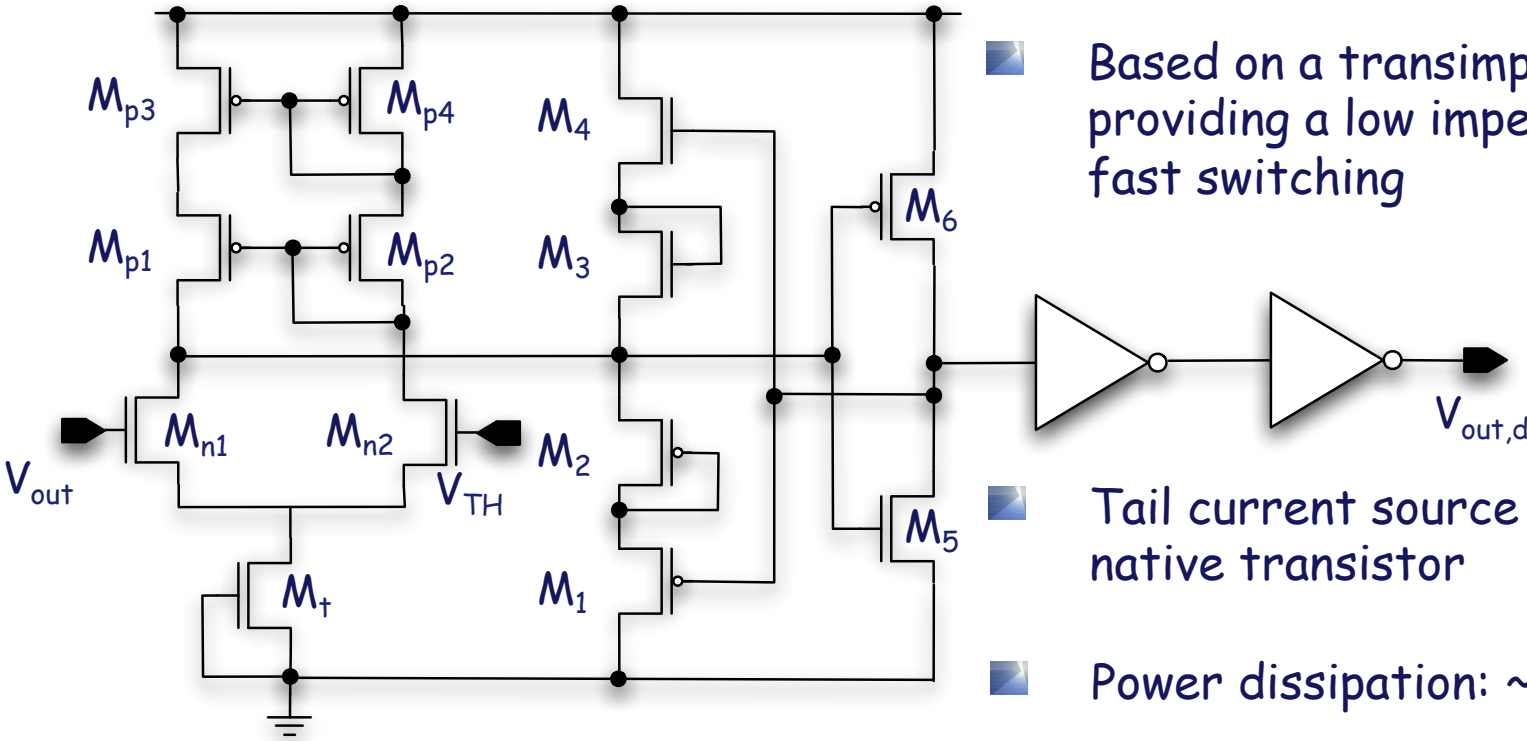


- In an advanced CMOS process, a synchronous architecture may be a good alternative, with self-calibration and discrete-time signal processing features (correlated double sampling, autozeroing) clocked by the bunch-crossing cadence

- **Diverse options are being explored, with interesting alternatives to classical analog pixel cell schemes**

Discriminators: asynchronous

Based on a transimpedance amplifier providing a low impedance path for fast switching

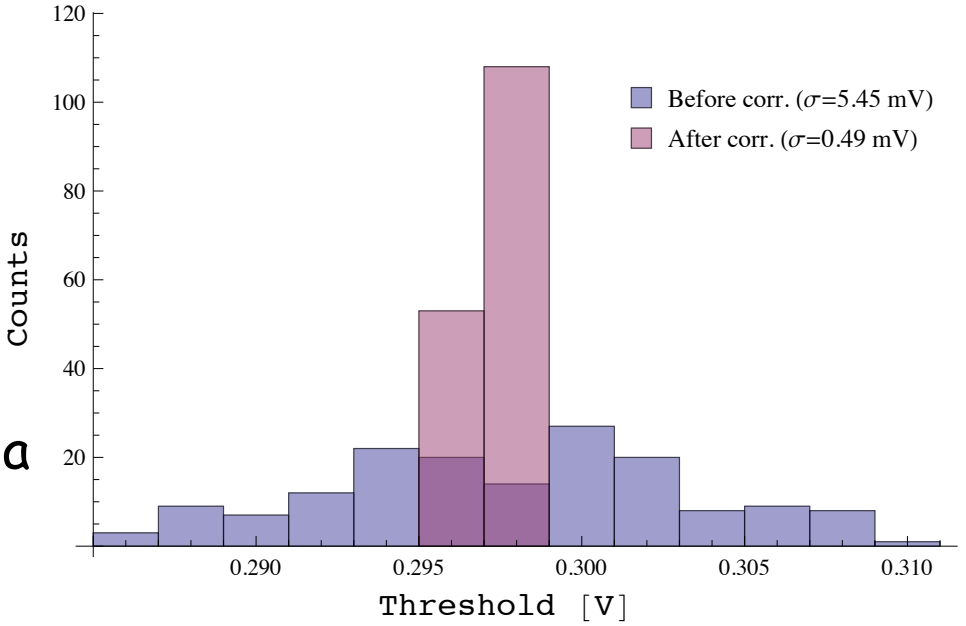


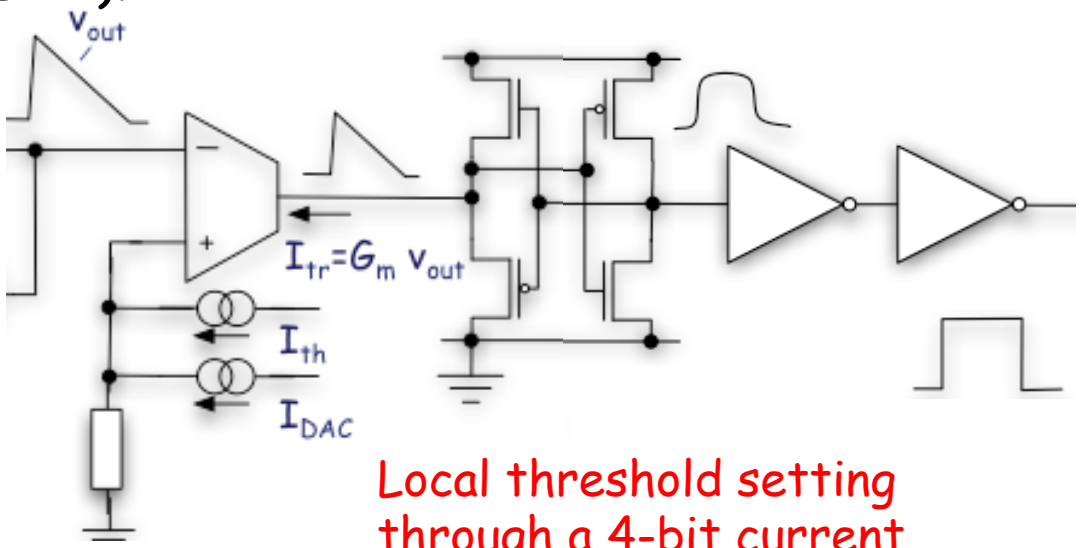
- Based on a transimpedance amplifier providing a low impedance path for fast switching
- Tail current source made with a native transistor
- Power dissipation: ~1.1 uW

INFN-Pavia design

Digital calibration of the discriminator threshold

Nonidealities of nanoscale CMOS transistors may be addressed by appropriate design techniques. This includes the digital calibration of analog circuits. In an analog front-end channel, the discriminator threshold may be finely adjusted by a local digital-to-analog converter (DAC).





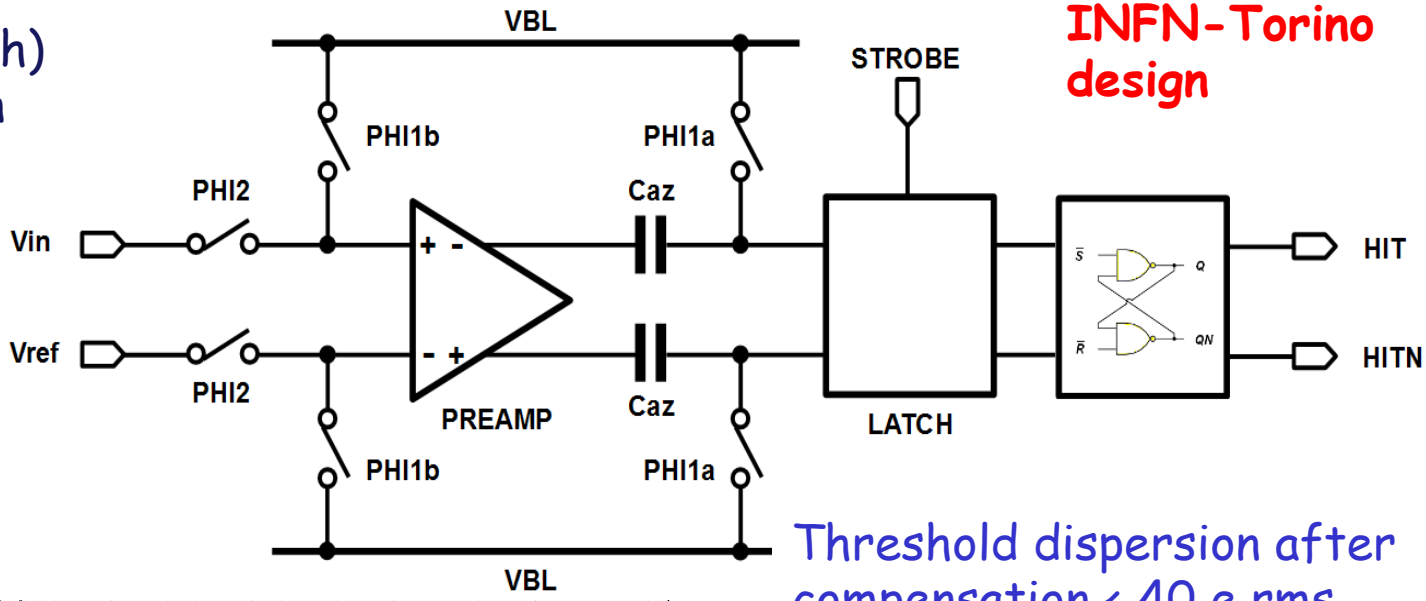
Local threshold setting through a 4-bit current steering DAC

INFN-Pavia design

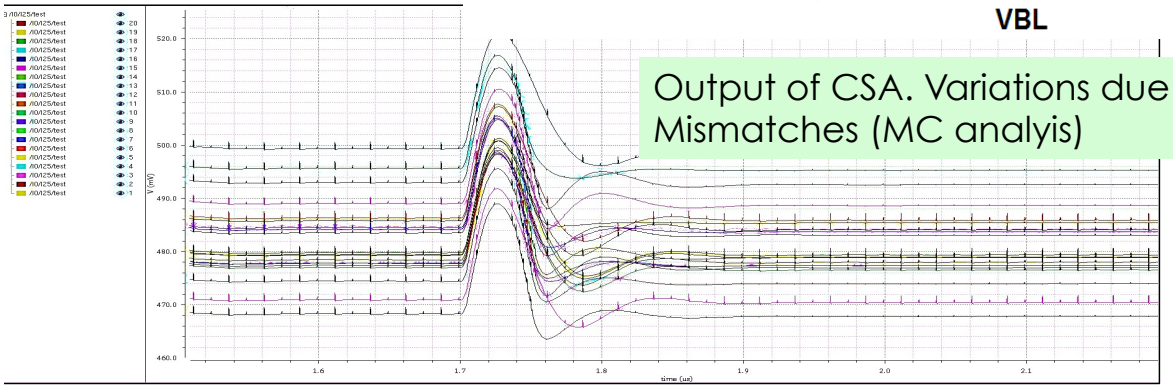
Threshold dispersion:
Before correction 380 e rms
After DAC correction 35 e rms

Synchronous discriminators

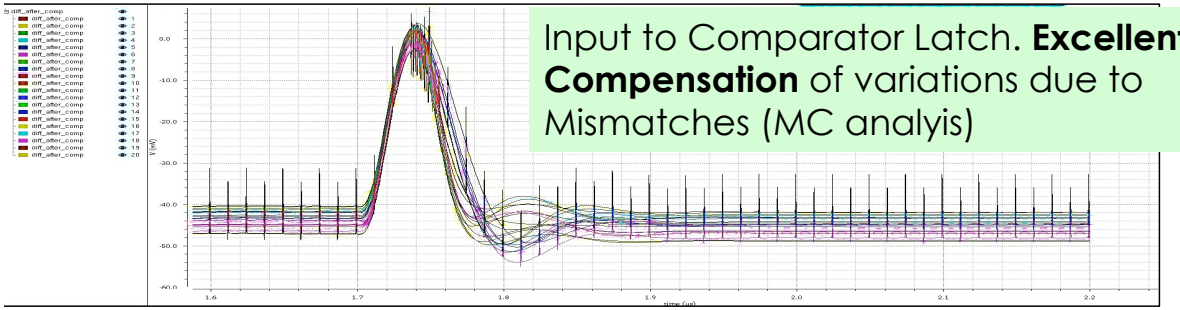
Offset (and mismatch) cancellation based on comparator autozero (store offset on a capacitor, and then substract it from signal +offset)



INFN-Torino design



Output of CSA. Variations due to Mismatches (MC analyis)



Input to Comparator Latch. **Excellent off-set Compensation** of variations due to Mismatches (MC analyis)

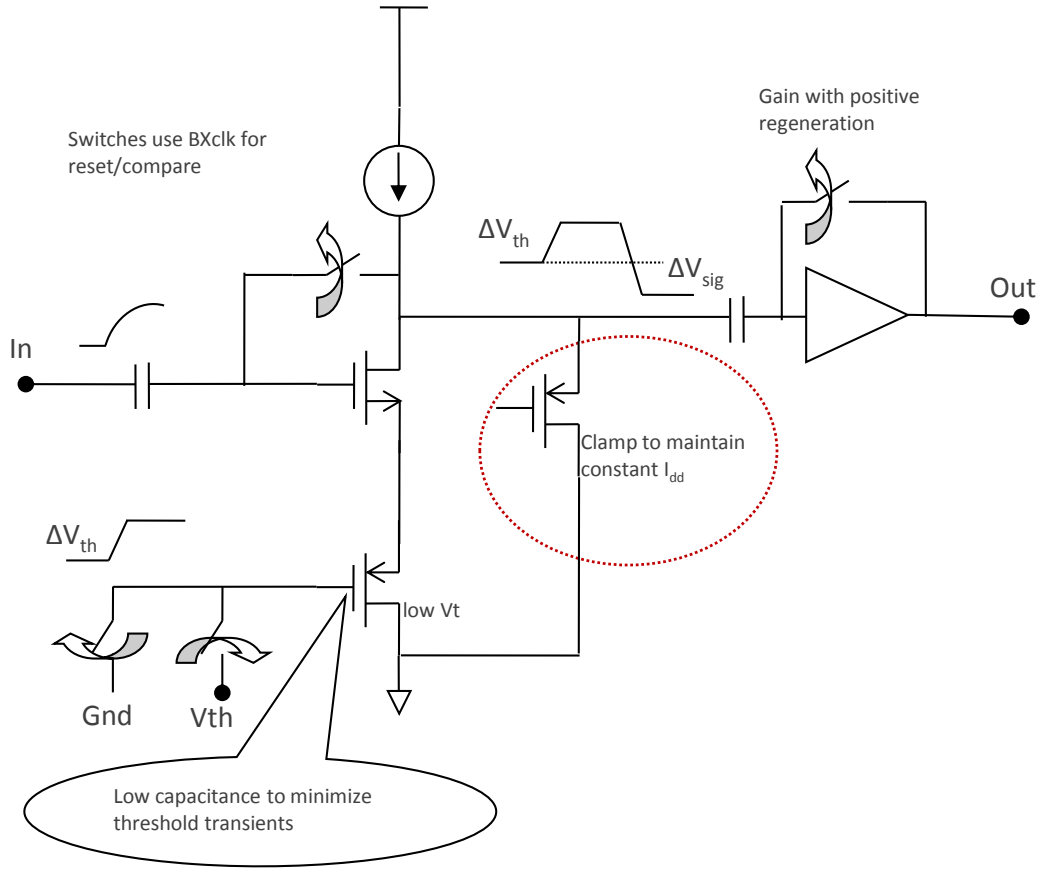
Threshold dispersion after compensation < 40 e rms

Design compatible with Fast-ToT thanks to locally generated clock. Example: for Qin = 30ke$^-$, ToT = 250ns

ENC = 110 e rms @ C_D = 100 fF

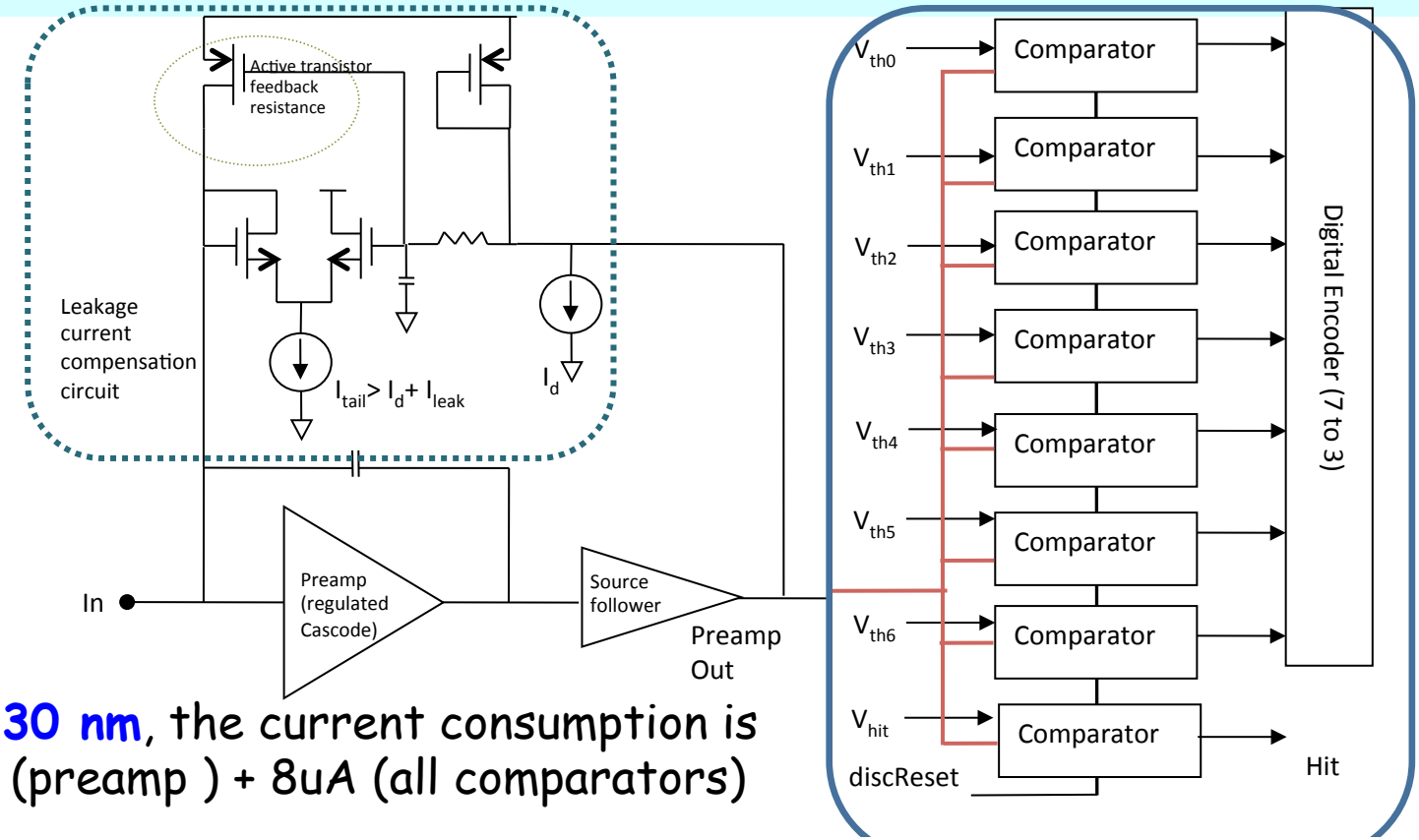
A fast and compact synchronous discriminator

Fermilab design in 130 nm CMOS



- Compact, single-ended architecture
- Correlated double sampling:
  - Auto-zeroed
  - Increased pileup immunity
  - Signal filtering
  - No need for trimming DACs
- 12.5ns reset phase; 12.5ns active comparison
- Low-power, fast, insensitive to corners
- Additional gain and positive regeneration in 2nd stage.
- BXclk must be well controlled across a large chip
- 1.5µW/comparator

Is a Flash ADC affordable in the pixel cell?

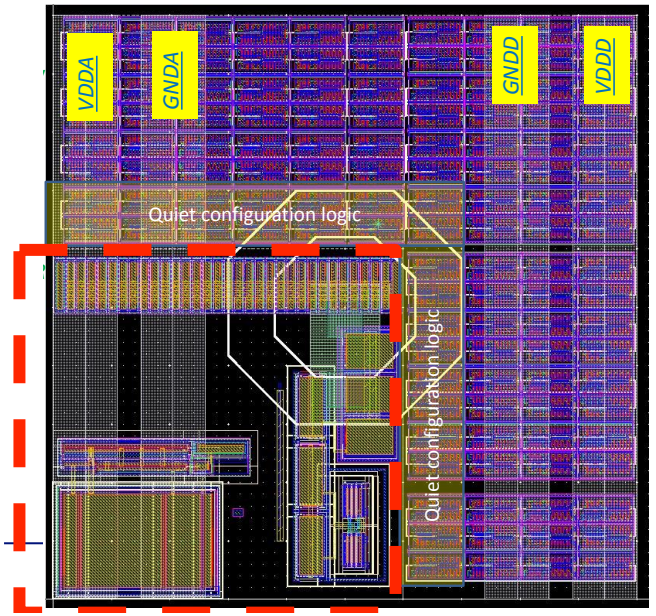


- In **130 nm**, the current consumption is 5uA (preamp) + 8uA (all comparators)
- **Translating to 65 nm (Fermilab-INFN Pavia collaboration)**, preliminary simulation results show that power can be reduced by 40%, improving speed and threshold dispersion performance
- The Flash ADC may be attractive in 65 nm, provided that a 3-bit charge resolution is enough for physics needs. Present specification is ≥ 5 bits, achievable with a ToT counter

Pixel analog front-end inside a large mixed-signal (mostly digital) integrated system

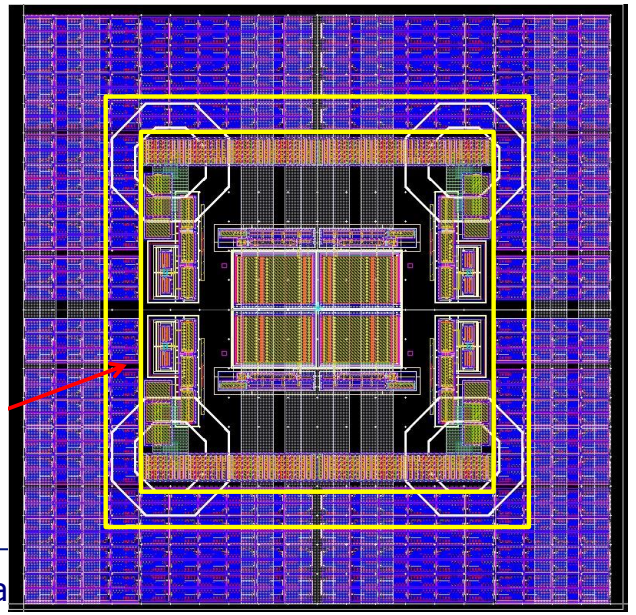
- In modern pixel readout chips, the analog front-end cell is embedded in an extremely complex microelectronic system, where analog and digital circuits coexist in the same small readout cell
- A correct layout is crucial to avoid digital interferences in the low-noise analog front-end; immunity to disturbances on analog supply lines ("PSRR") is also essential
- The "analog island" concept (A.Mekkaoui, LBNL)

50 μm x 50 μm pixel cell



Analog section

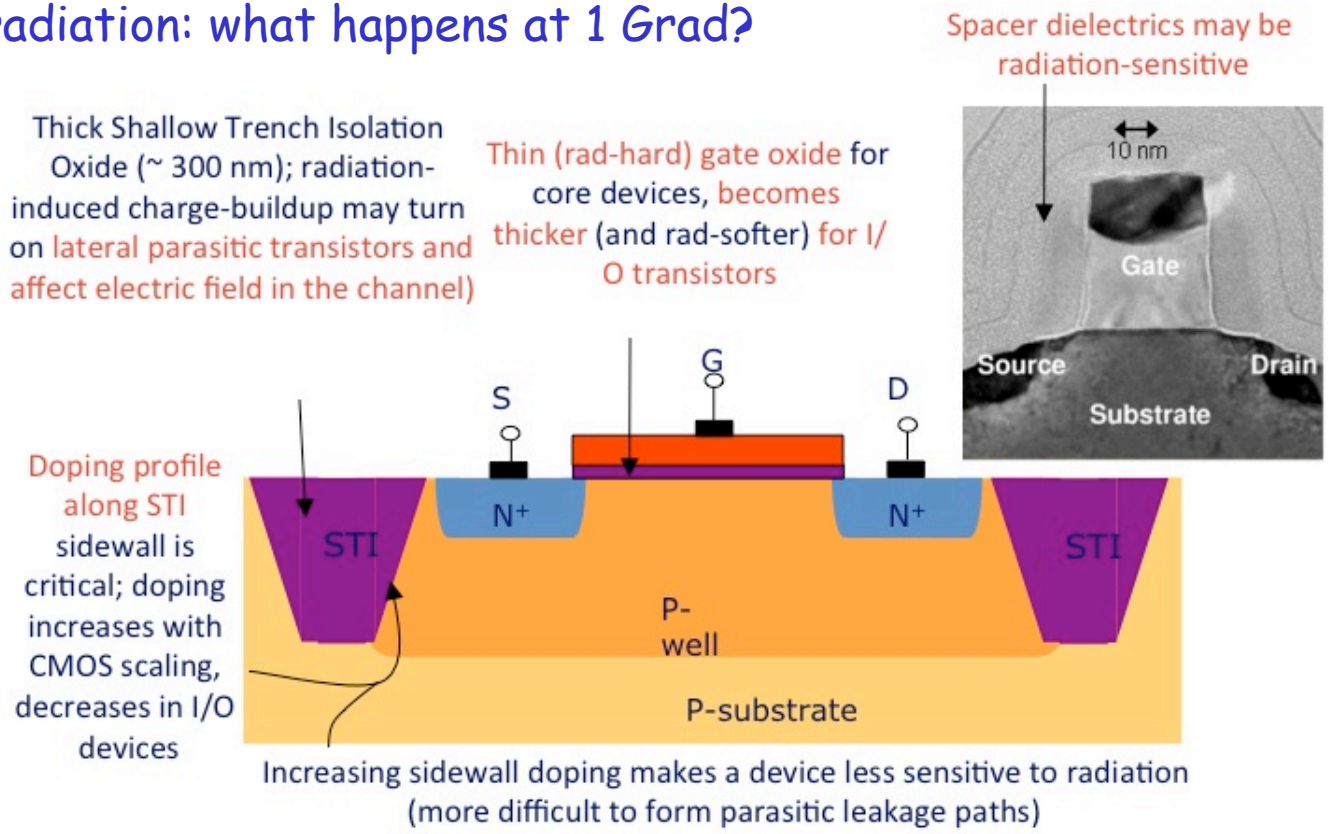
Four 50 μm x 50 μm pixel cells



65 nm CMOS at extreme radiation levels

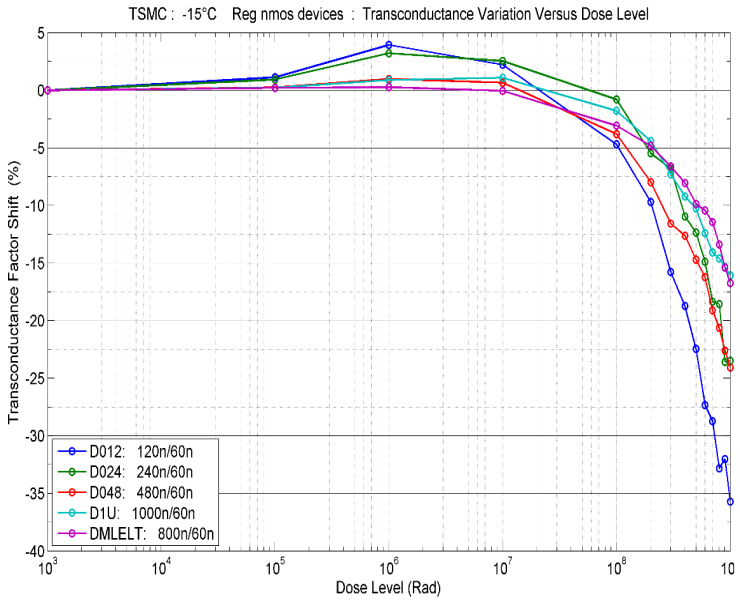
- At the HL-LHC design luminosity, for an operational lifetime of 10 years, the innermost pixel layer will be exposed to a total ionizing dose of 1 Grad, and to an equivalent fluence of 1-MeV neutrons of 2 x 10^{16} n/cm^2.
- If unacceptable degradation, **a replacement strategy** must be applied for inner pixel layers.
- Nanoscale CMOS (with very thin gate oxide) has a large intrinsic degree of tolerance to ionizing radiation: what happens at 1 Grad?

- Radiation induced electric charge is associated with thick lateral isolation oxides
- CMOS is usually not affected by non n-ionizing radiation: what happens at 2 x 10^{16} n/cm^2?

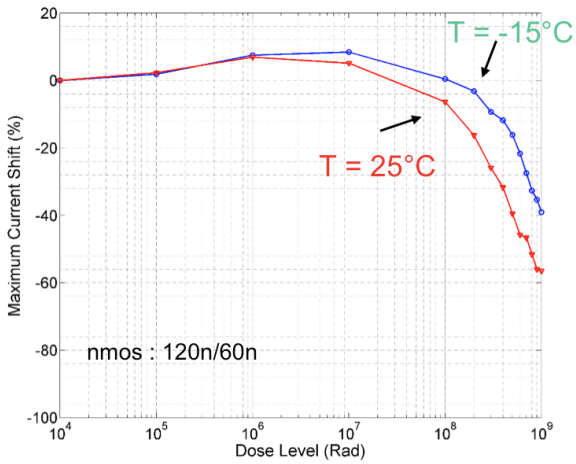


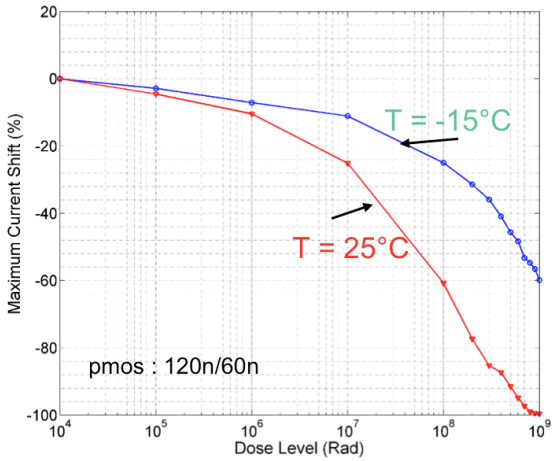
The analog front-end at extreme total ionizing dose

- Among other effects, PMOSFETs (especially minimum size ones) show a large transconductance degradation, which becomes very steep over 100 Mrad (partial recover after annealing)
- This is probably not so critical for the design of analog blocks, where minimum size transistors can be avoided if necessary; the study of radiation effects on noise is ongoing
- Damage mechanisms have yet to be fully understood; they appear to be **less severe at** the foreseen operating temperature of the pixel detector at HL-LHC (**about - 15 °C**)



CPPM data with X-rays
(Fermilab and Padova studying radiation effects with other sources)





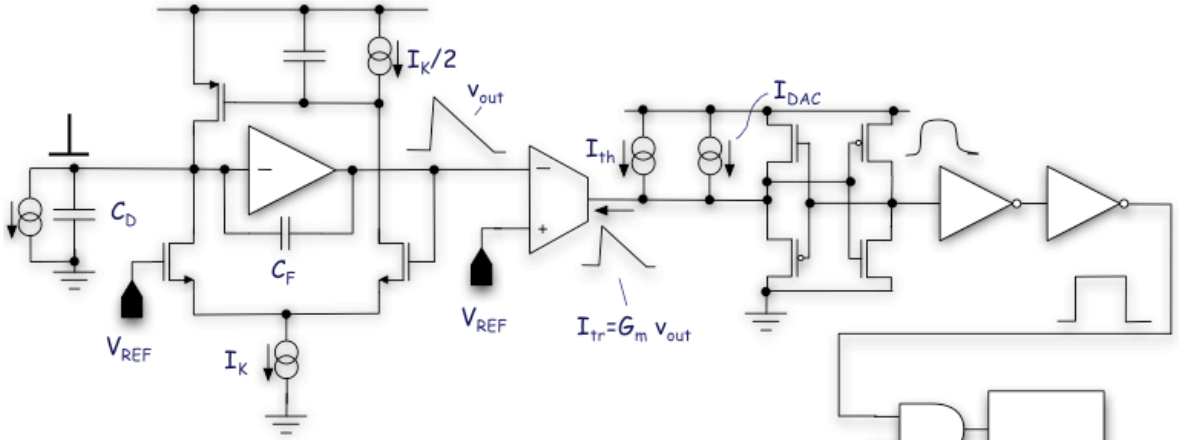
Conclusions

- The challenge of analog design in 65 nm CMOS for pixel readout at the HL-LHC is being tackled by our community of microelectronic designers in a collaborative way (RD53, the INFN project CHIPIX 65)
- Current goal: developing/qualifying technology, tools, architecture and building blocks required to design next generation pixel chips for very high rates and radiation
- First round of submissions in 2014, first prototypes currently being characterized, other submissions in Spring 2015
- These prototypes will allow us to evaluate the best solutions for the architecture of the analog front-end

➔ **Full pixel chip prototype in 2016**

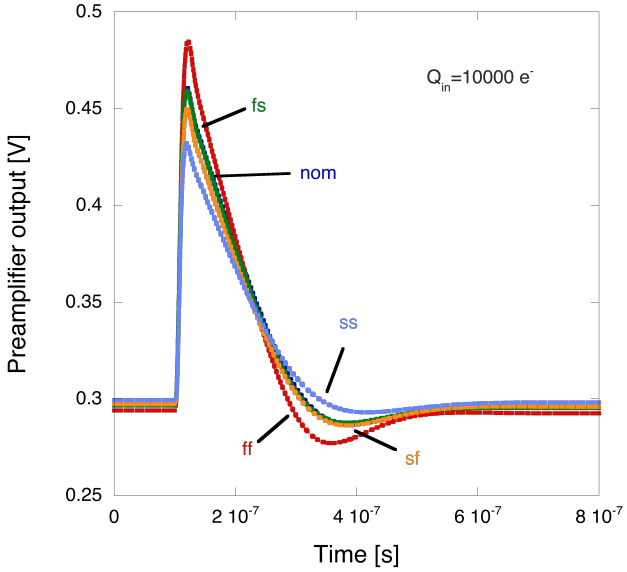
Backup slides

A continuous-time analog channel… (INFN-PV/BG)



- Single amplification stage for minimum power dissipation
- Krummenacher feedback to comply with the expected large increase in the detector leakage current
- High speed, low power current comparator
- Relatively slow ToT clock – 40 (80) MHz
- 4/5 bit counter – 400 ns maximum time over threshold

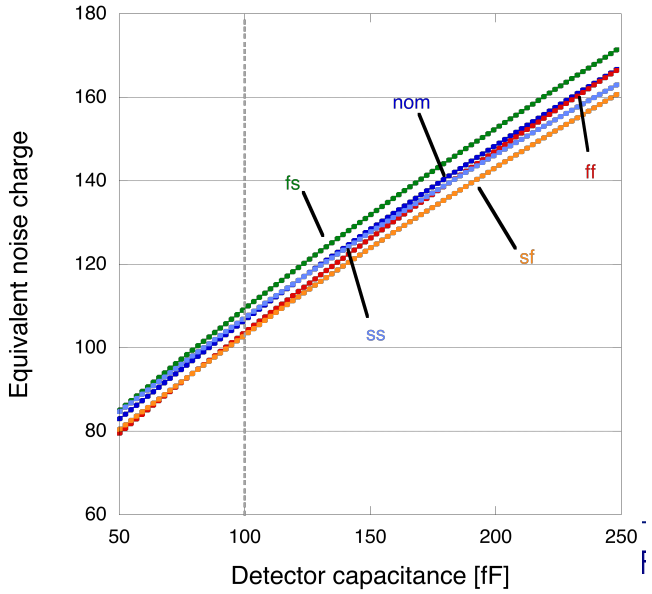
- 30000 electron maximum input charge, ~500 mV preamplifier output dynamic range

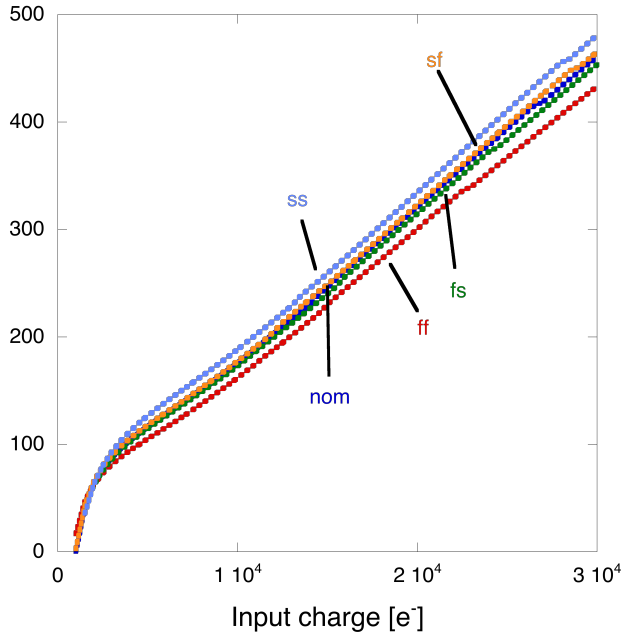


Current consumption:

3 μA in the preamp

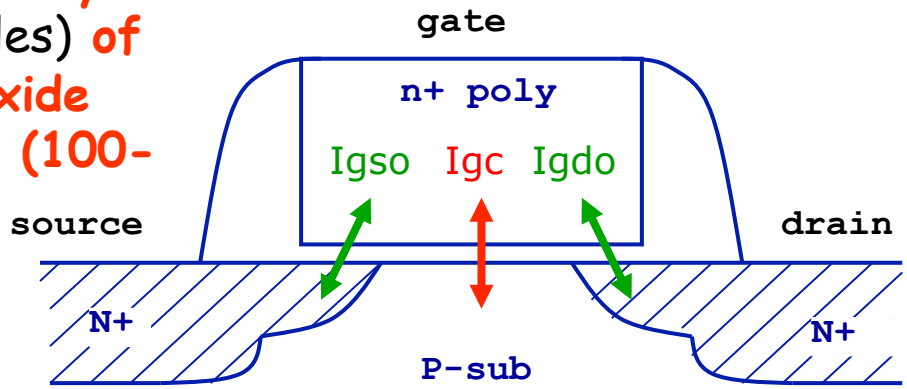
1 – 1.5 μA in the discriminator





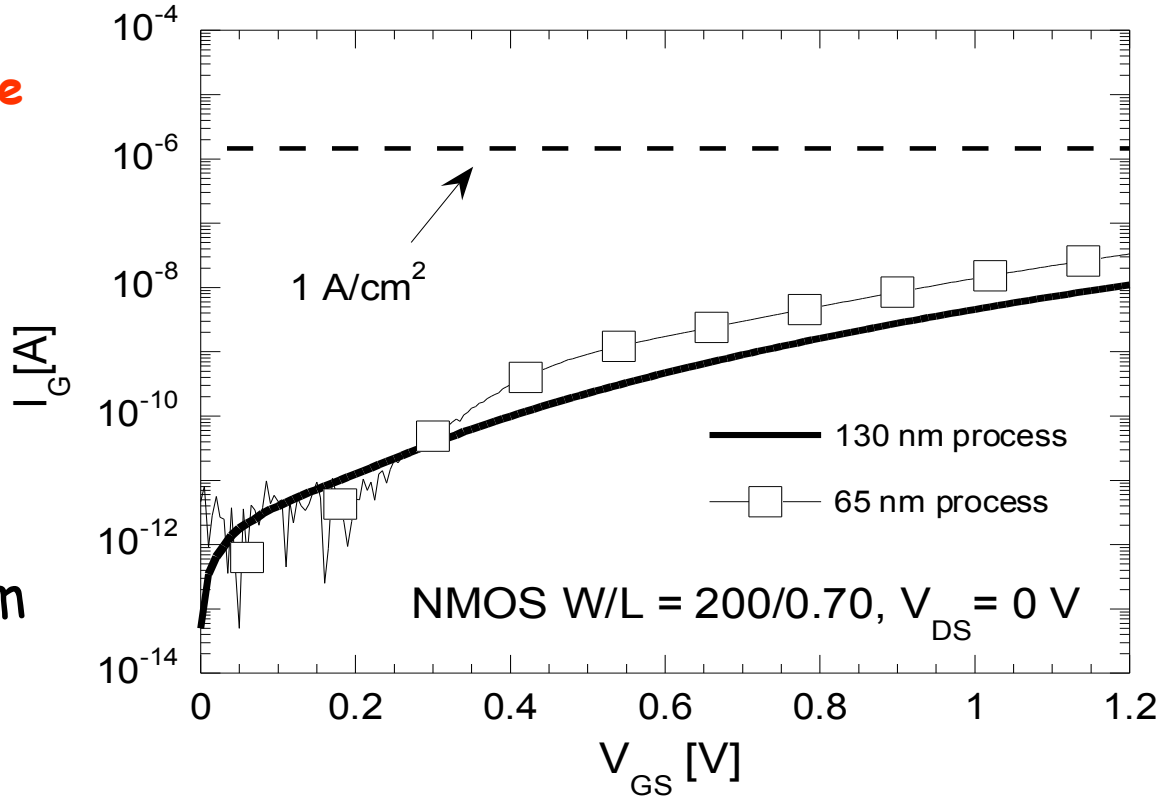
Gate current in LP 65 nm CMOS

- **Charge carriers have a nonzero probability** (larger for electrons with respect to holes) **of directly tunneling through a silicon dioxide layer with a physical thickness < 2 nm (100-nm scale CMOS).**

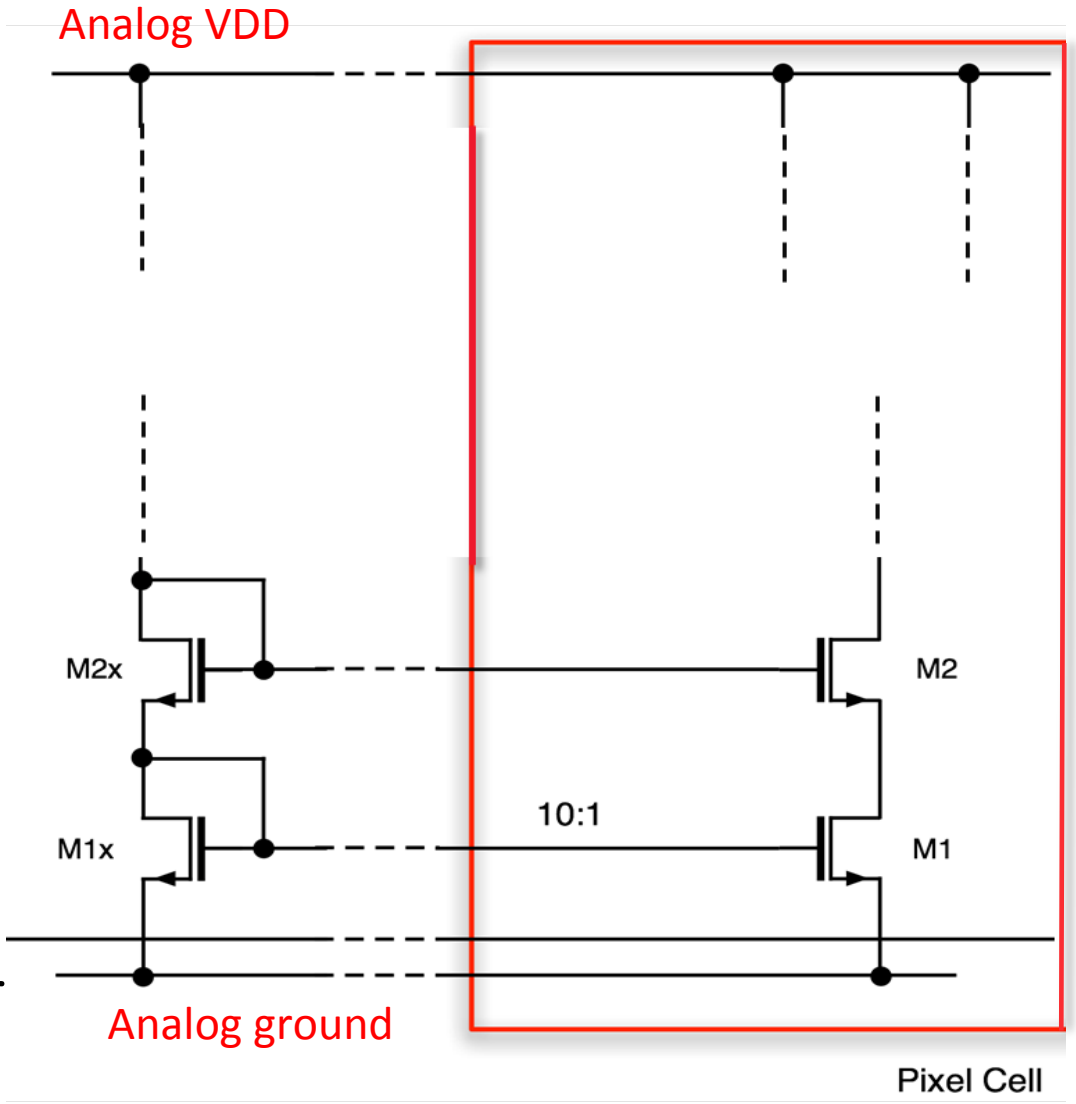


- **In Low Power transistors, aggressive scaling rules are not applied; this also concerns the equivalent gate oxide thickness**

The gate current for LP 65 nm transistors has similar value as for 130 nm devices



Gate current and global design of a CMOS readout chip

In a single transistor in the LP 65 nm process, the gate current has a very small value (of the order of 100 pA/μm^2 for the NMOS, 10 pA/μm^2 for the PMOS).

However, when bias voltages for analog front-end circuits have to be distributed across a large chip (e.g., a 4 cm^2 pixel readout integrated circuit), the total gate leakage current has to be taken into account in the design of reference voltage and current generators (typically, DACs) and current mirrors.