Contribution ID: **22** Type: **not specified**

Analog circuit design in 65 nm CMOS for the readout of silicon pixel detectors

Tuesday 17 February 2015 09:50 (25 minutes)

The next generation of silicon pixel detectors at high energy physics and photon science experiments sets unprecedented and extreme requirements to the microelectronic systems that are used to read out the sensors. Front-end integrated circuits have to provide advanced analog and digital signal processing functions in pixel readout cells with a pitch of a few tens of a μm. They have to handle huge data rates and stand extreme levels of radiation without degrading their performance. Presently, the community of designers is studying the 65 nm CMOS technology as a tool to achieve the ambitious goals of future pixel systems, and has organized itself in the RD53 project to tackle the specific challenges associated with the development of readout chips for the innermost pixel layers of experiments at the High Luminosity LHC. This talk is focused on the specific features of the design of the analog front-end circuits for pixel sensors in a nanoscale CMOS process, taking into account typical constraints such as low power dissipation and small available silicon area. It provides an overview of the architectures that are currently being explored for signal amplification and filtering, hit detection and analog-to-digital conversion. A comparison is given with the different solutions that are developed in the same technology for the readout of pixel sensors for imaging at advanced X-ray sources. This makes it possible to appreciate how analog design in 65 nm CMOS can be tailored to very demanding specifications in a broad range of pixel detector applications.

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Session Classification: Introduction