Test-Beam Results of the AMS 180 HVCMOS prototypes

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On behalf of: CERN, Genova INFN, Karlsruhe Institute of Technology, Liverpool University, University of Bern and University of Geneva

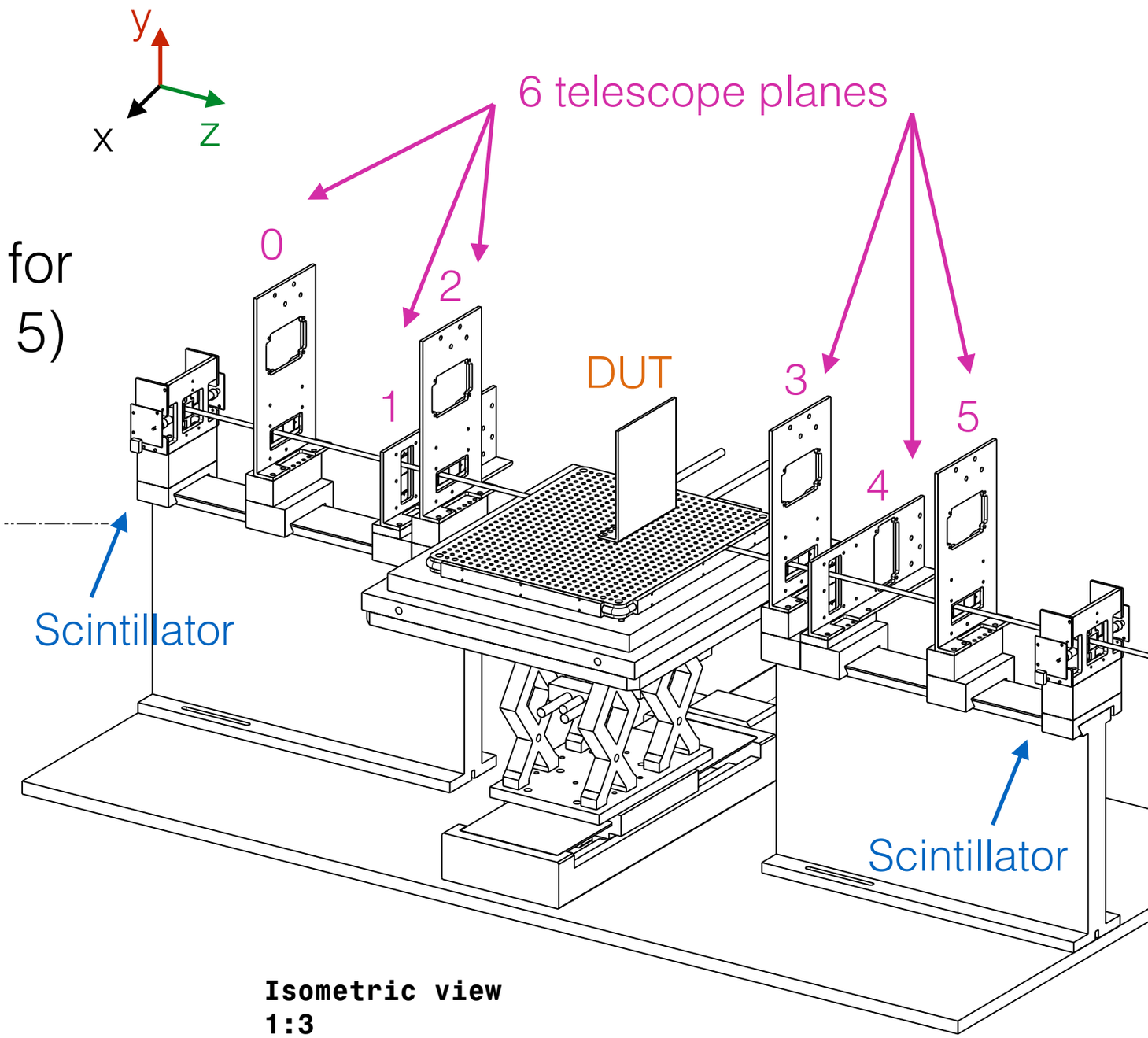
Trento workshop
17/02/15

Overview

- Telescope overview
- HVCMOS v2 and v4 designs and samples
- Efficiency, timing and ToT results
- Threshold and Bias scans

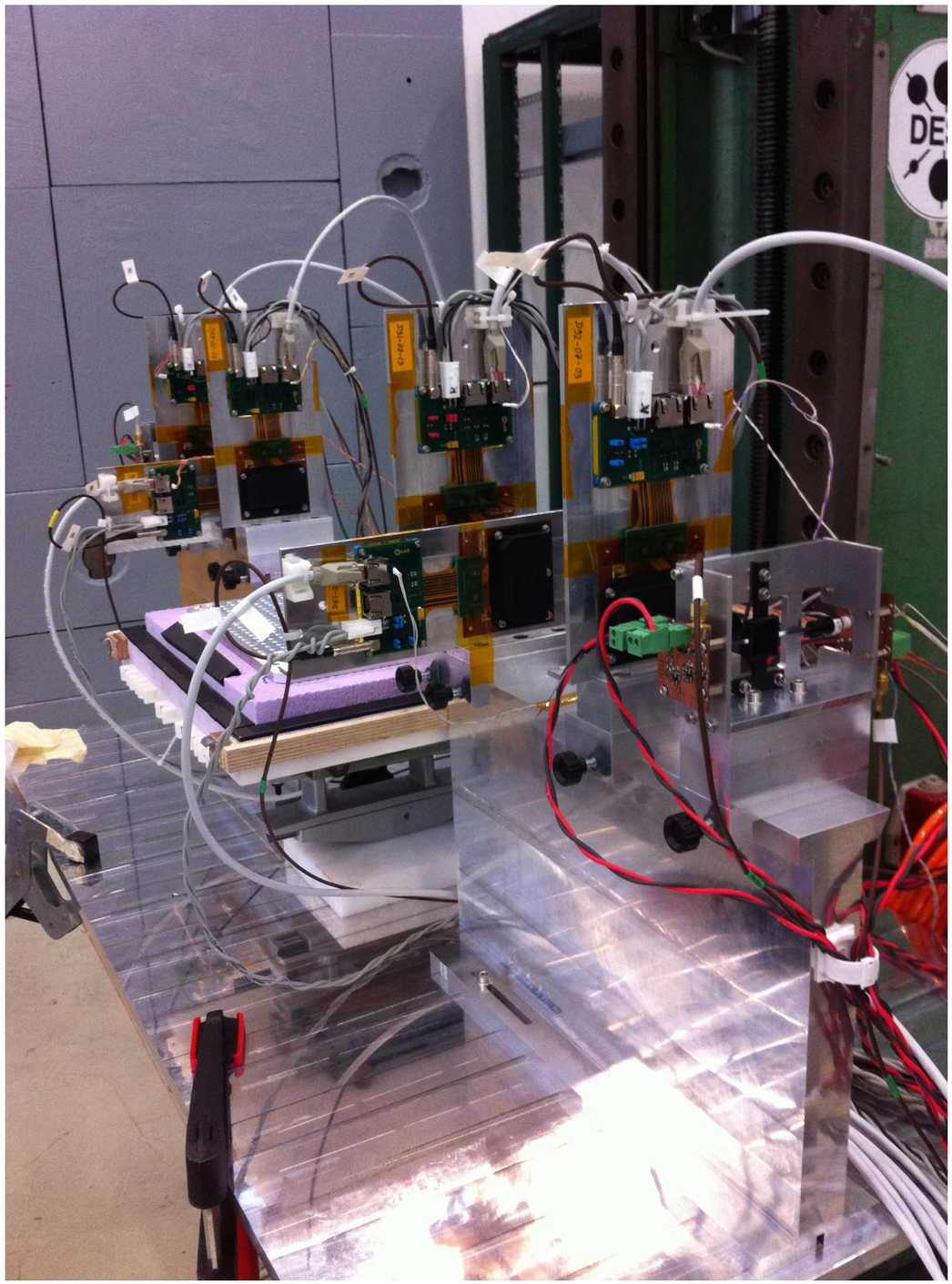
IBL Modules Telescope

- 6 DoubleChip IBL modules (2 x 2 cm^2/FE)
- Pixel size of 250 x 50 μm (x-y) for non rotated planes (0,2,3 and 5)
- Trigger on planes 0 and 5 or Scintillators
- ROI can be defined on planes 0 and 5
- RCE readout up to 8 FE (6 telescope planes + 2 DUT) giving thanks to SLAC for the support.



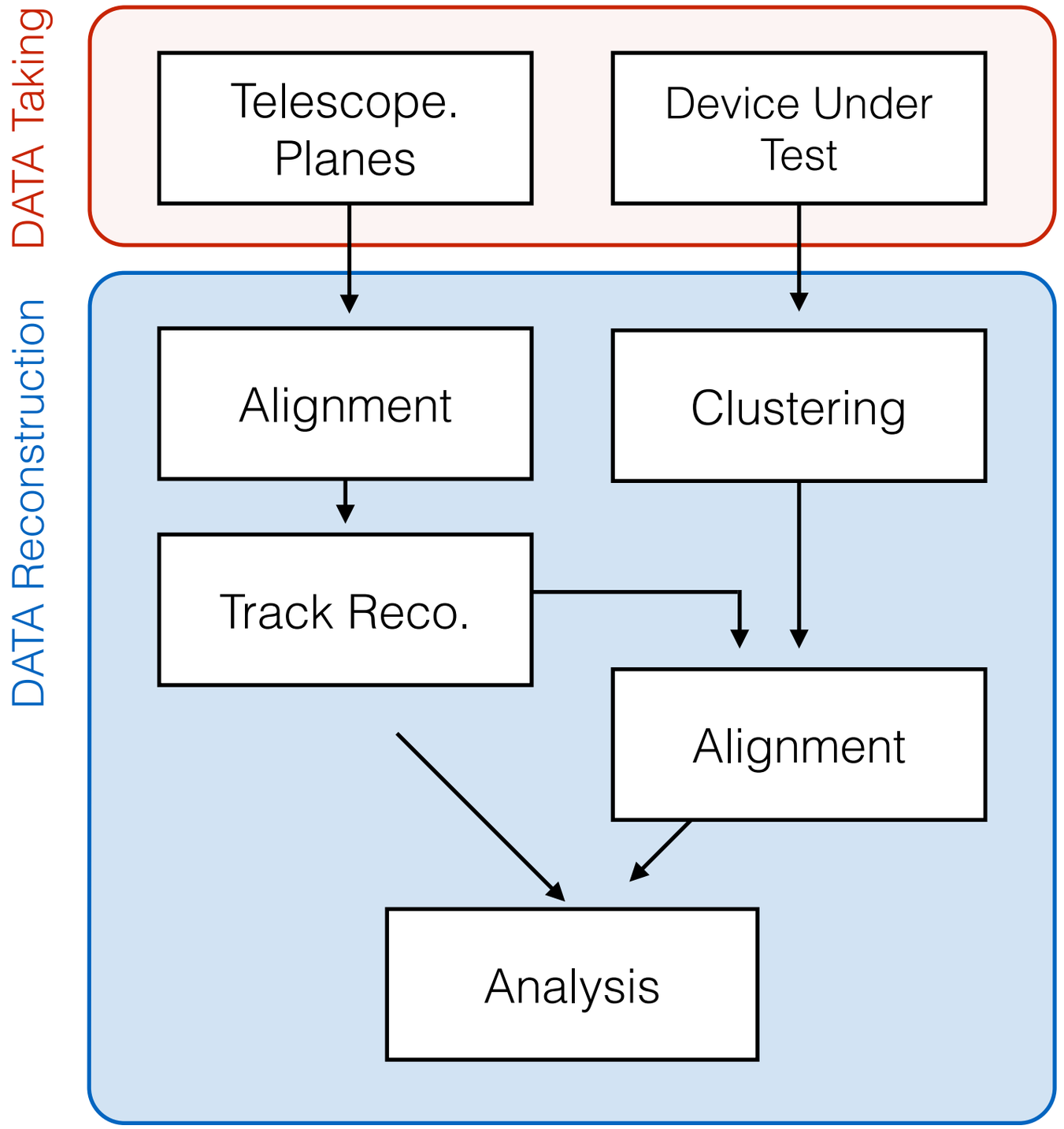
IBL Modules Telescope

- 100 kHz trigger rate during data taking
- >10% of triggers had a hit on the DUT thanks to the ROI definition



Reconstruction Software

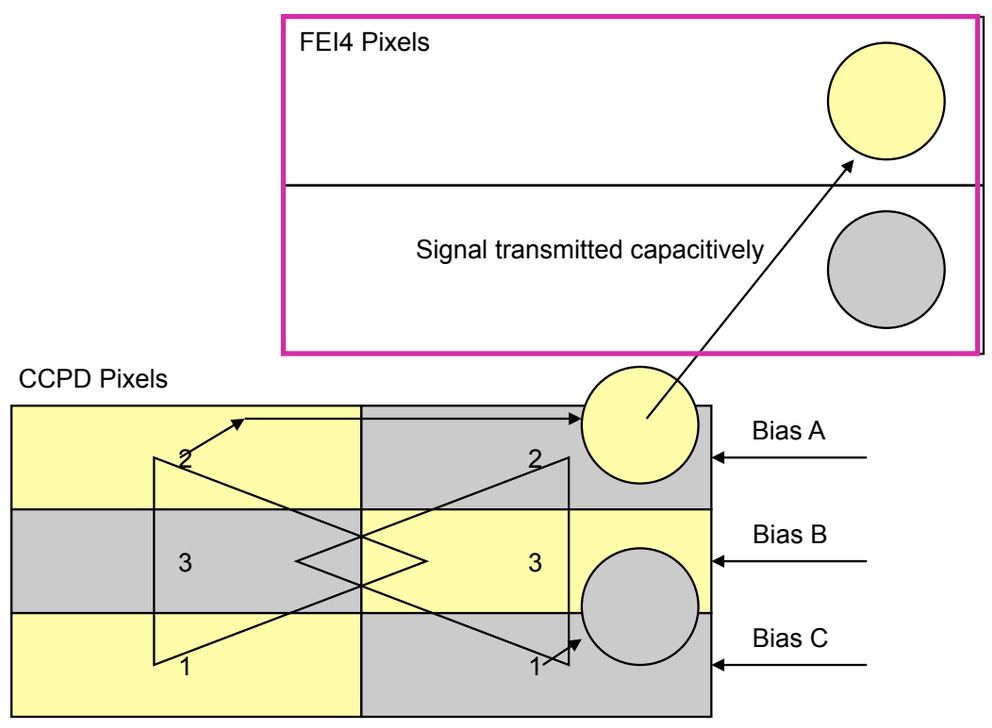
- Reconstruction software: JUDITH
- Adapted to handle the telescope geometry (pixel asymmetry and plane rotations) and additional control plots



HVCMOS v2

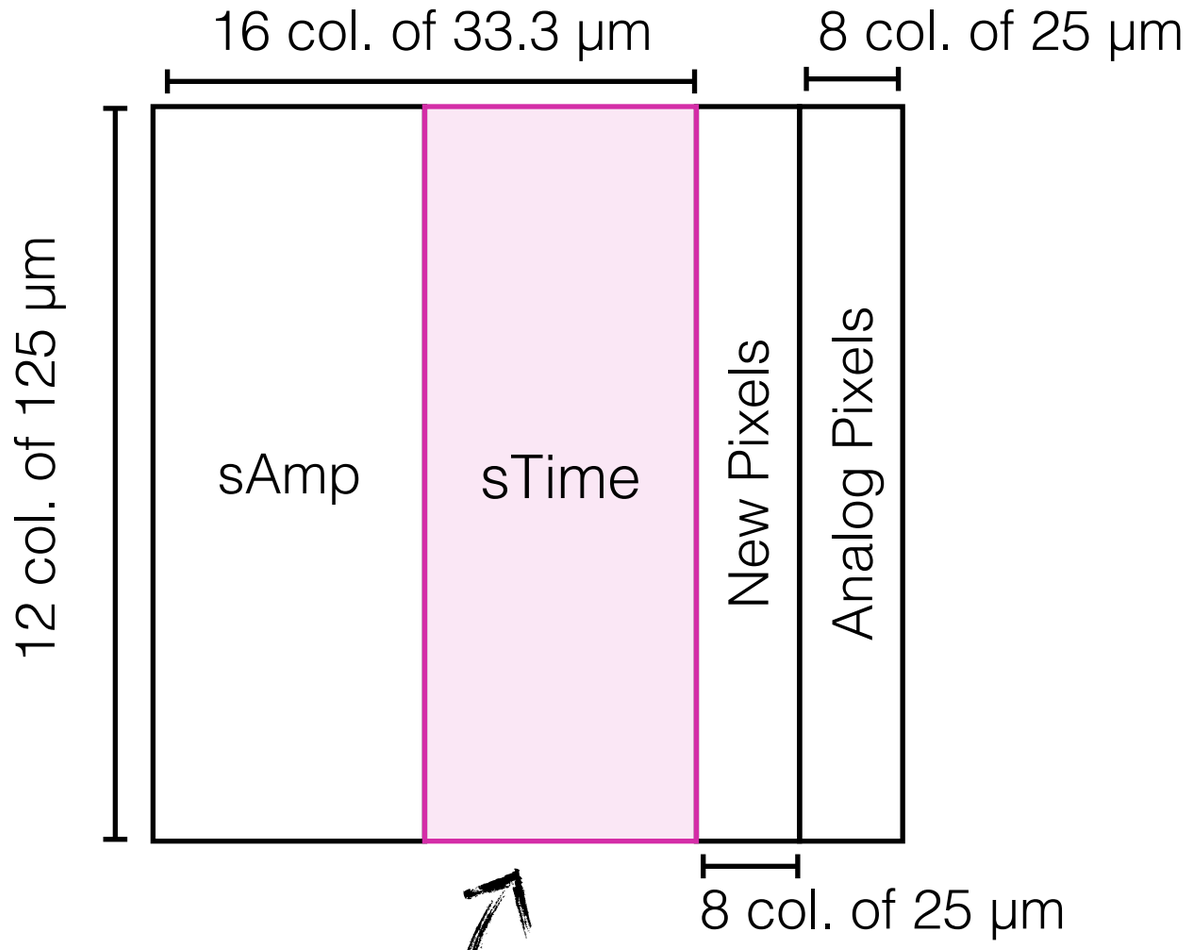
- HV-CMOS version 2
- Sensor Size (2.2 x 4.4 mm^2):
  - 36 x 36 sub-pixels (864) each pixel of 33 x 125 μm
- Merged pixels during reconstruction to handle “chest” structure

Pixels of 100 x 250
Unit cell



v4 structure

- Several HVCMOS pixels flavours in the HVCMOS v4 structure:

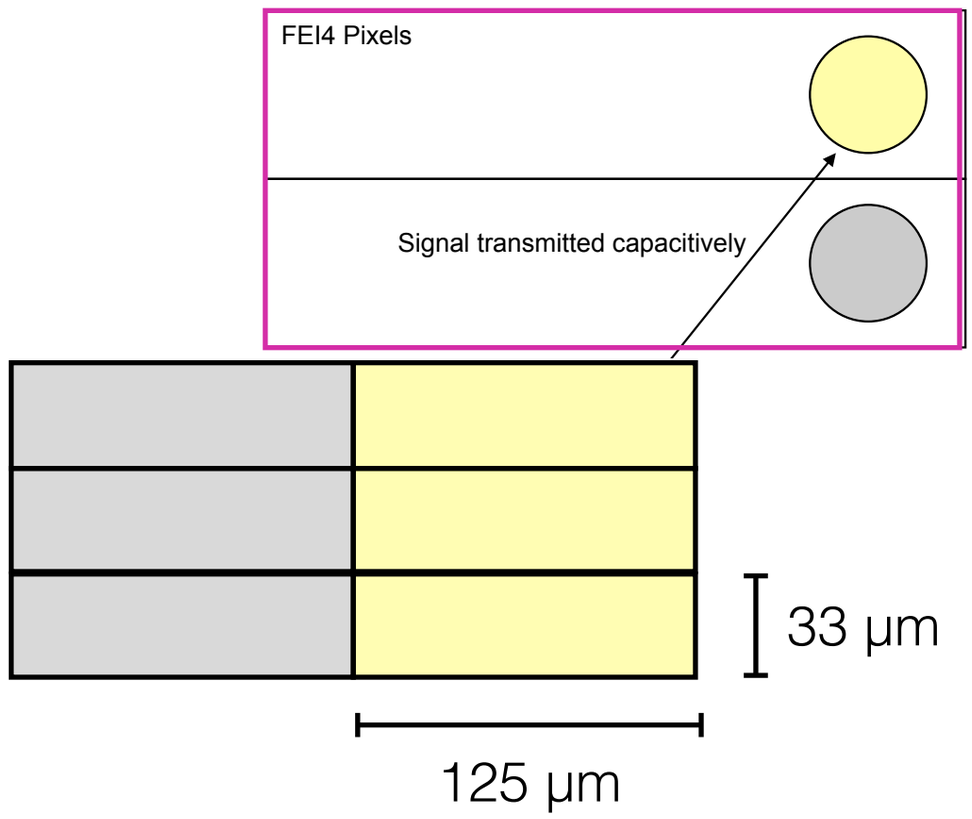


Studied pixels and presented results

v4 structure

- Stime HVCMOS pixels
- Standard pixels with new voltage-mode amplitude or pulse length coding
- 16 x 5 unit cell, containing 6 HVCMOS pixels 33 x 125 μm
- Different inner pixel connection with respect to v2. Not needed to be taken into account on the reconstruction thanks to the merging

Pixels of 100 x 250
Unit cell



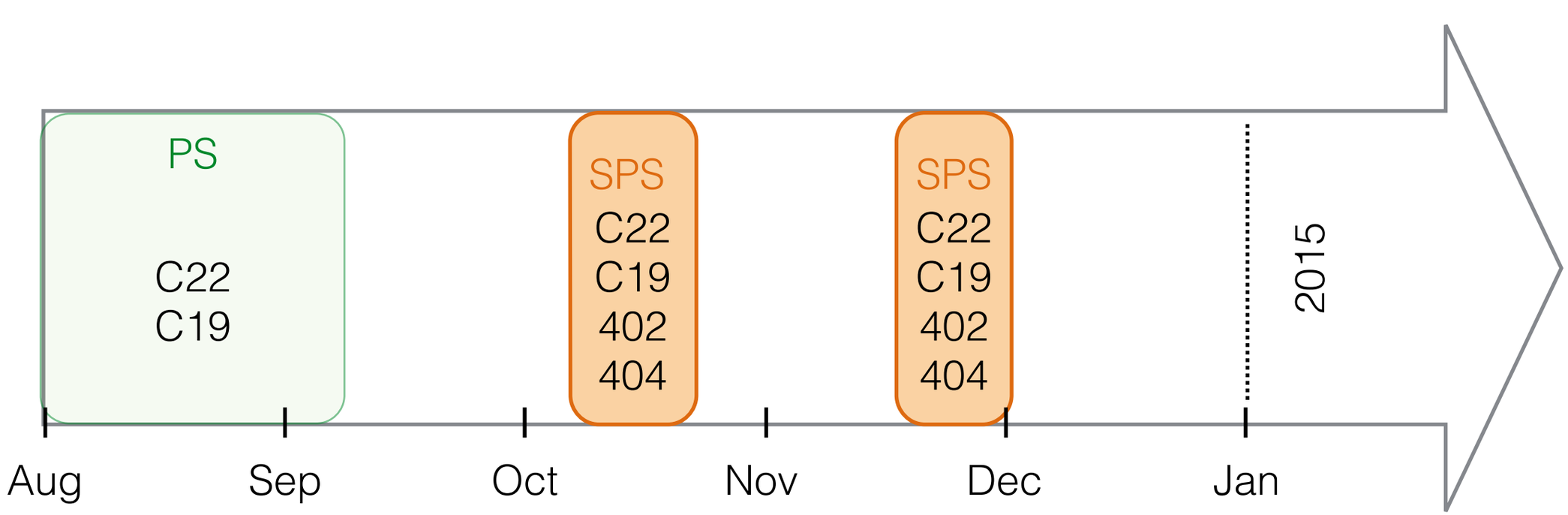
HVCMOS samples

Non Irradiated:

v2: C22
v4: 402

Irradiated:

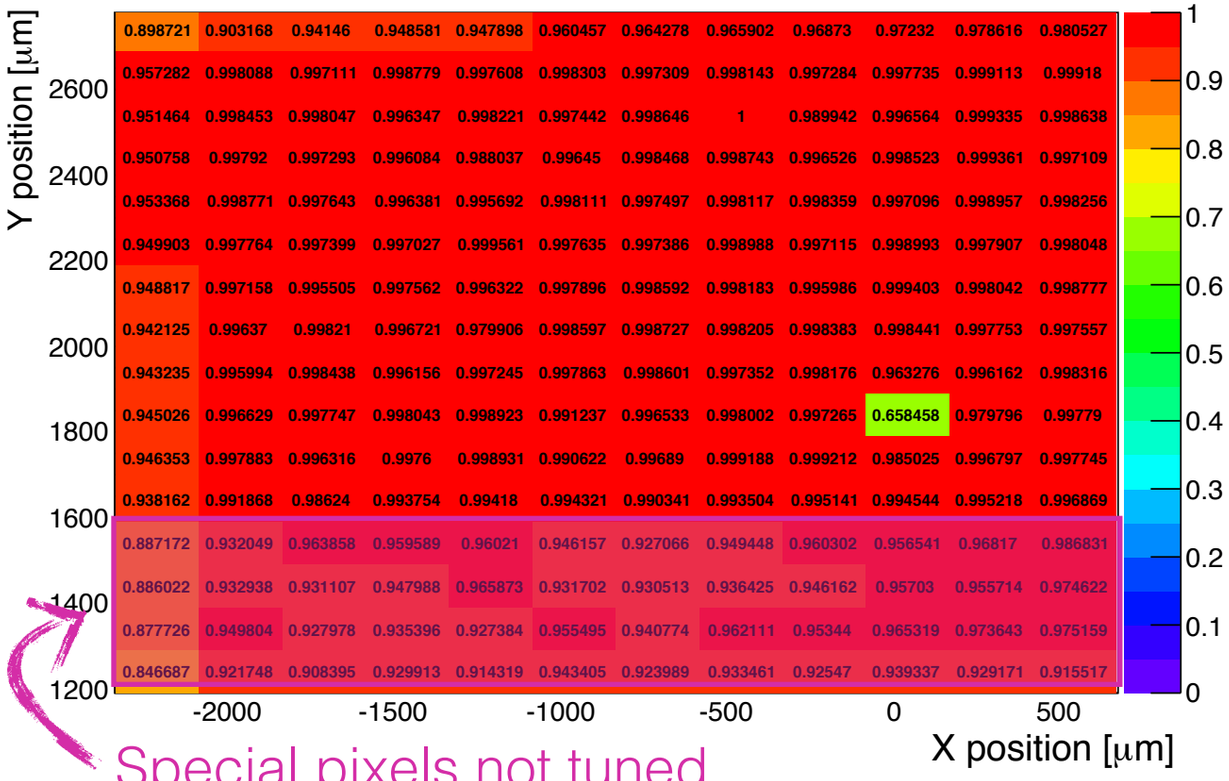
v2: C19
v4: 404



12 Billion triggers during 2014 SPS data taking

AMS 180 v2 efficiency

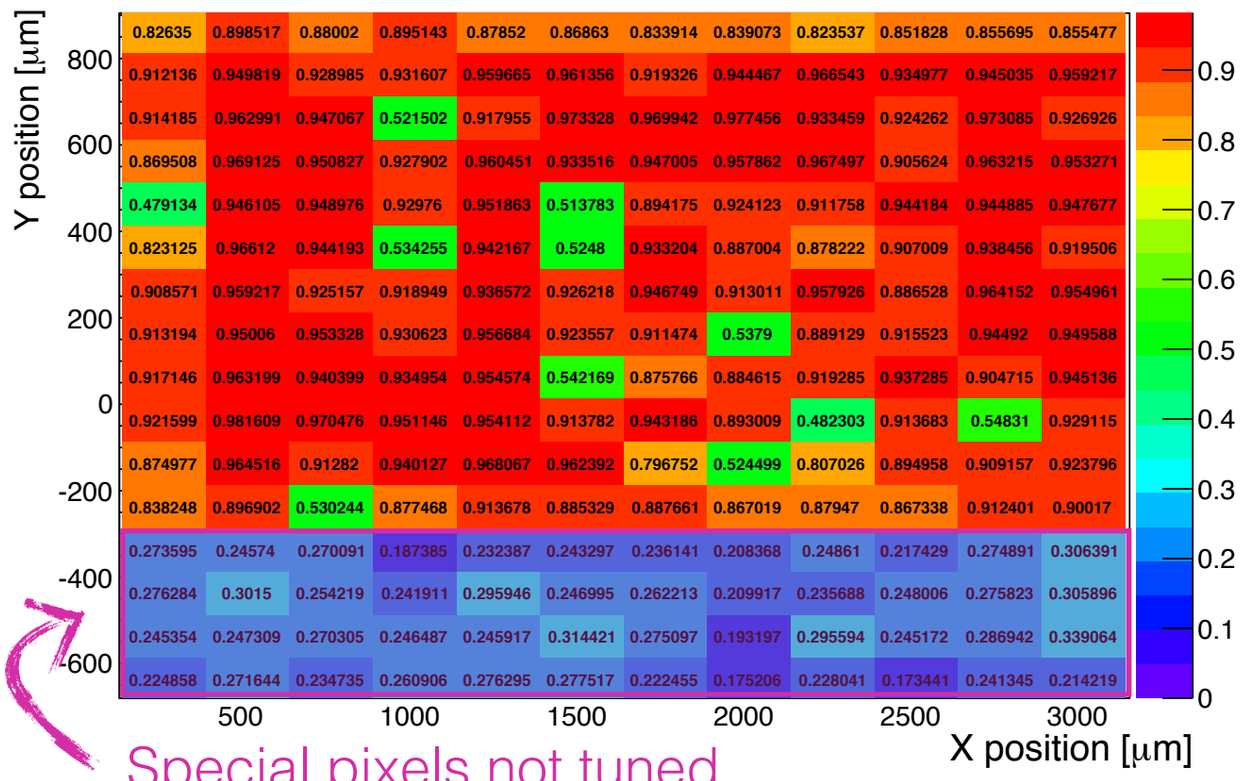
C19, unIrradiated
Bias 90 V, Th 0.94 V



Special pixels not tuned

C22, 10^{15} n_{eq}/cm^2
Bias 80 V, Th 0.94 V

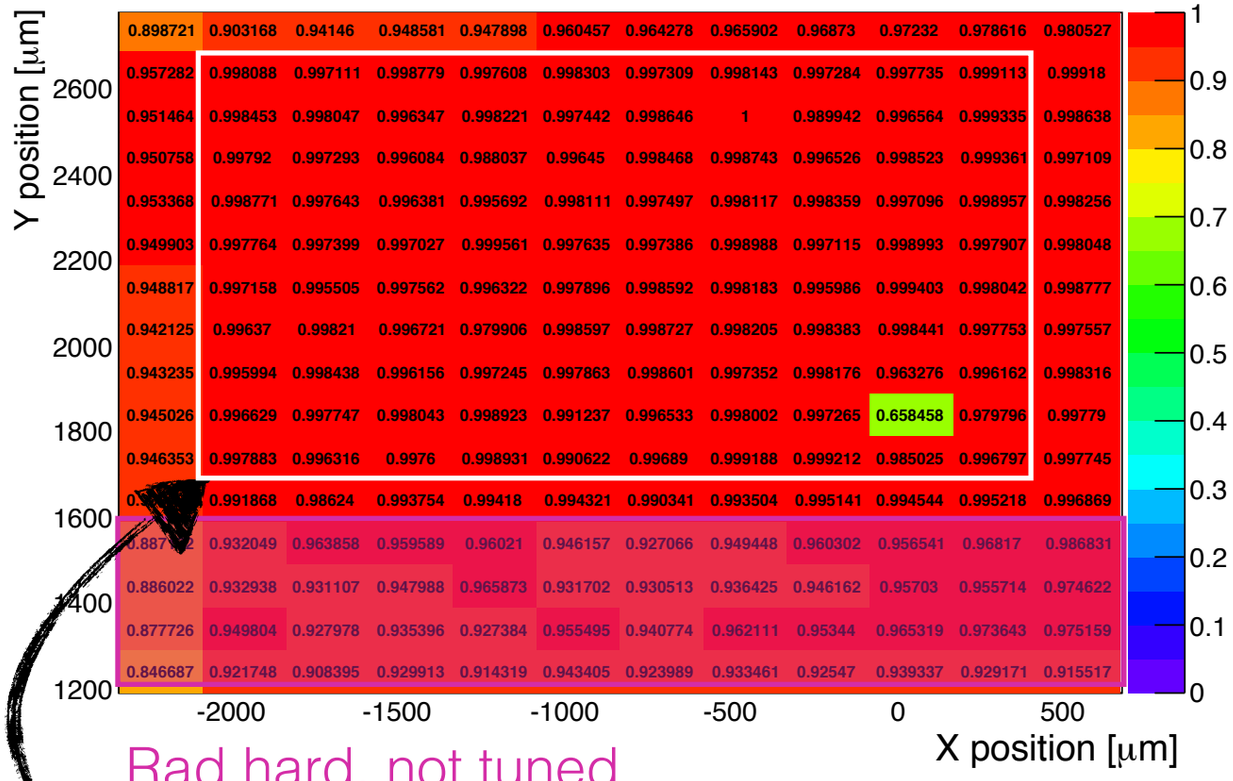
Few HVCMOS pixels showed no output signal



Special pixels not tuned

AMS 180 v2 efficiency

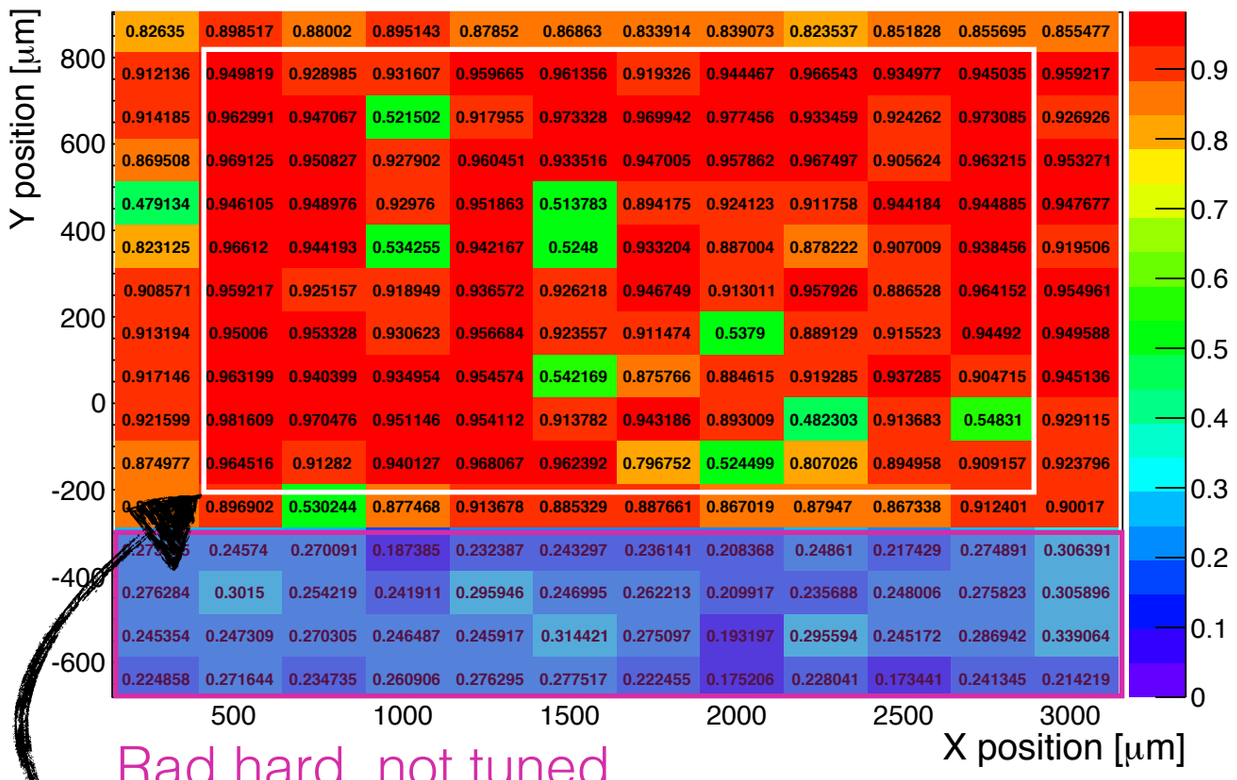
C19, unIrradiated
Bias 90 V, Th 0.94 V



Rad hard, not tuned

eff. all Lv1: 99.7%

C22, 10^{15} n_{eq}/cm^2
Bias 80 V, Th 0.94 V



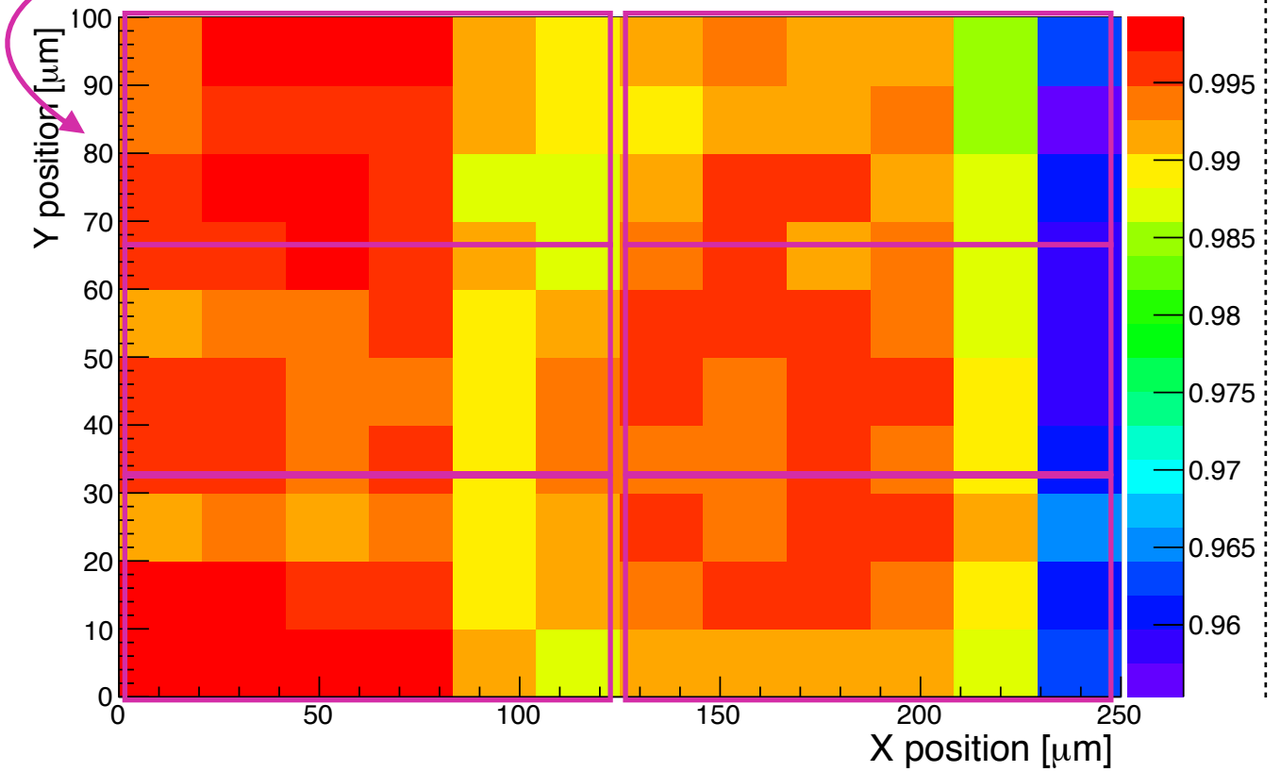
Rad hard, not tuned

eff. all Lv1: 93%

v2 InPixel eff.

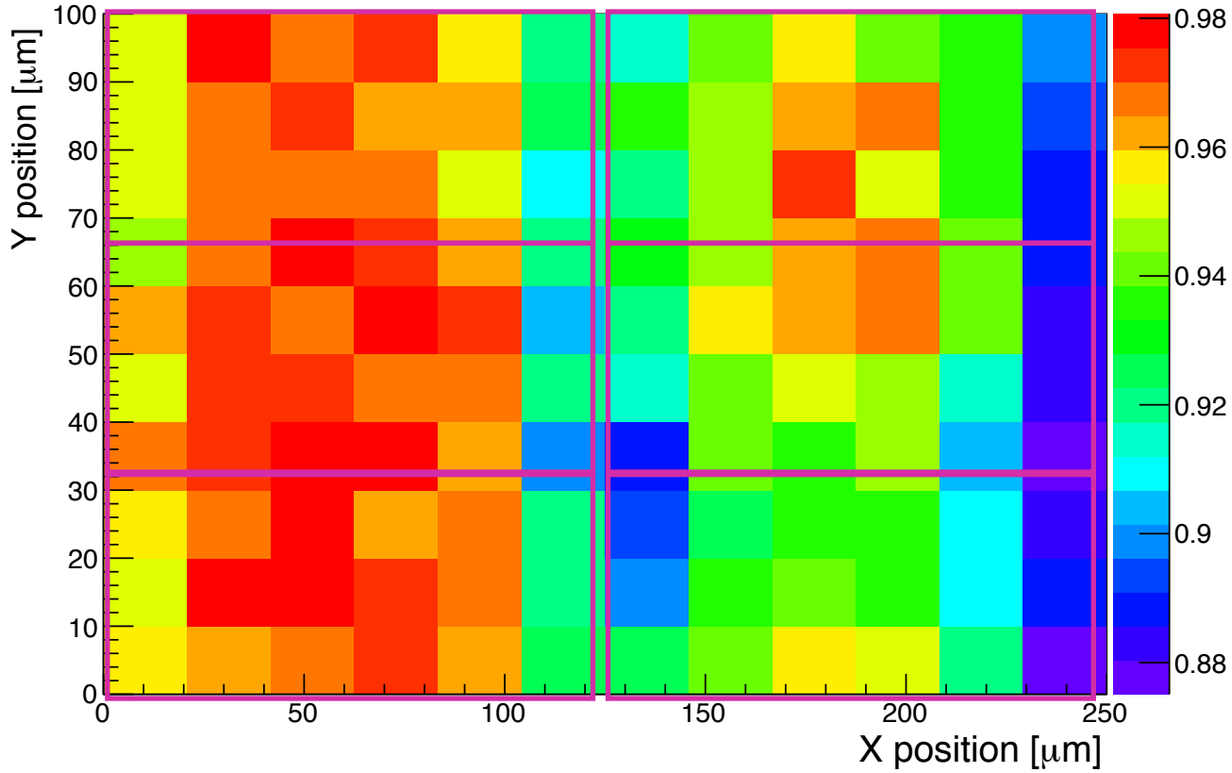
C19, unIrradiated
Bias 90 V, Th 0.94 V

2x3 HVCMOS pixels in 1 unit-cell



eff. all Lv1: 99.7%

C22, 10^{15} n_{eq}/cm^2
Bias 80 V, Th 0.94 V

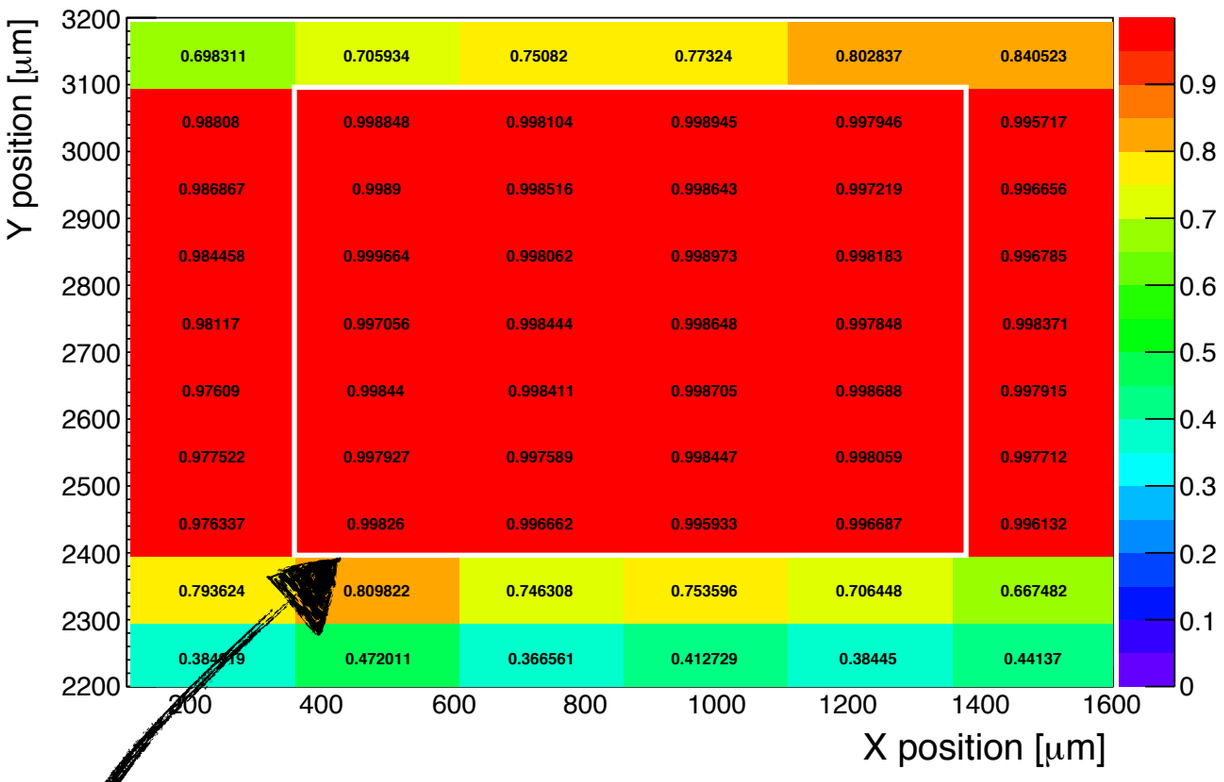


eff. all Lv1: 93%

v4 Global eff.

402, unIrradiated
Bias 12 V, Th 0.84 V

10M events

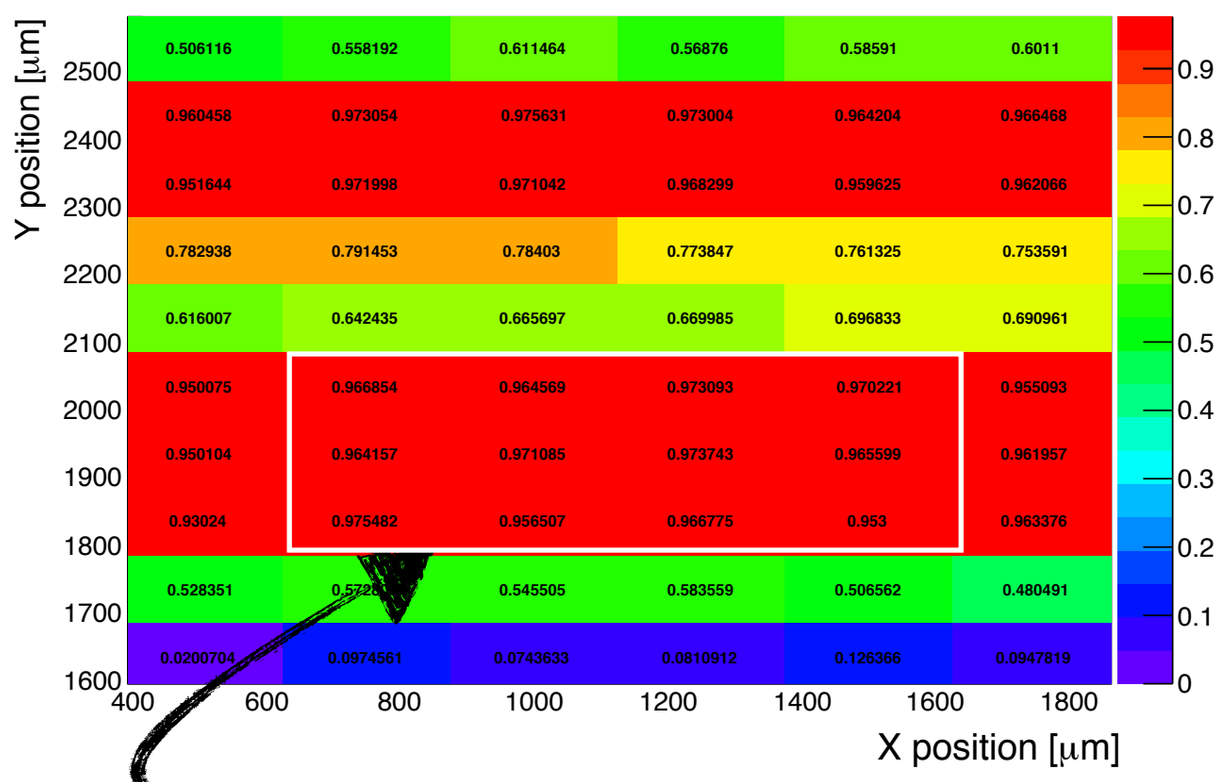


eff. all Lv1: 99.7%

404, 10^{15} n_{eq}/cm^2
Bias 30 V, Th 0.84V

2M events

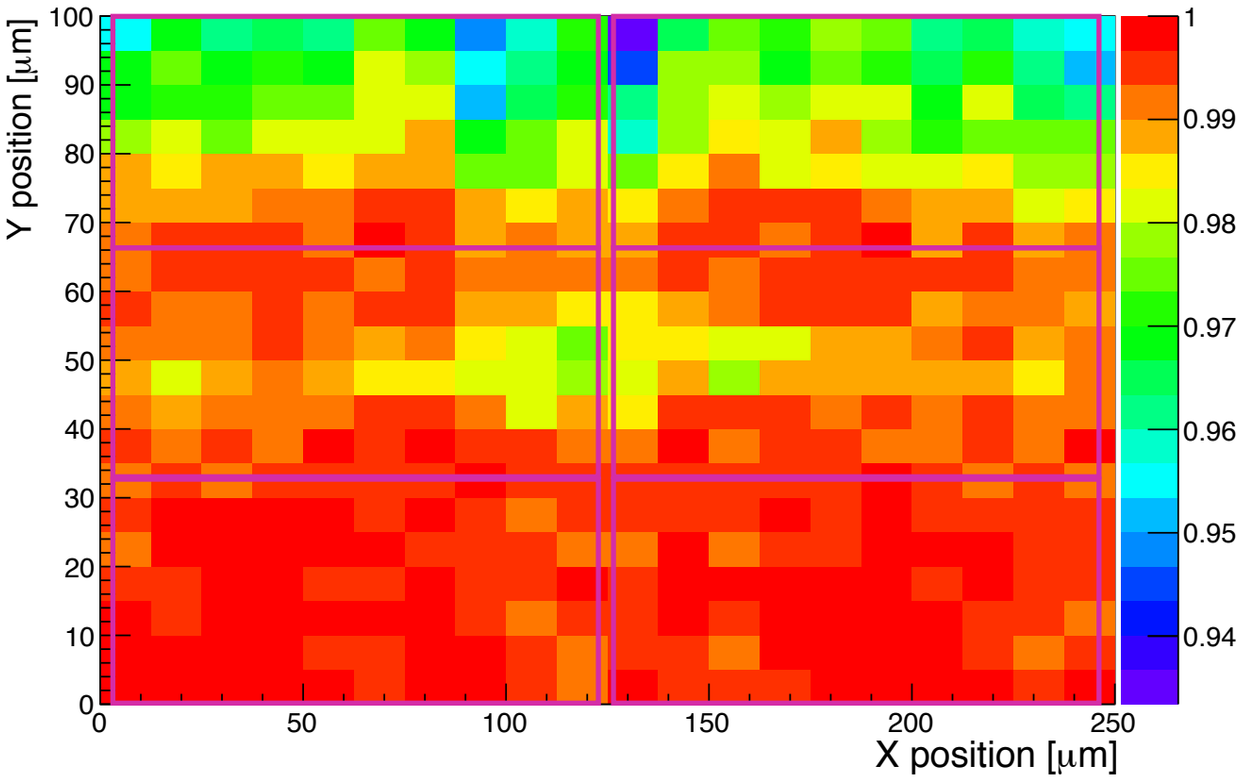
1 HVCMOS Row was off during data taking



eff. all Lv1: 96.2%

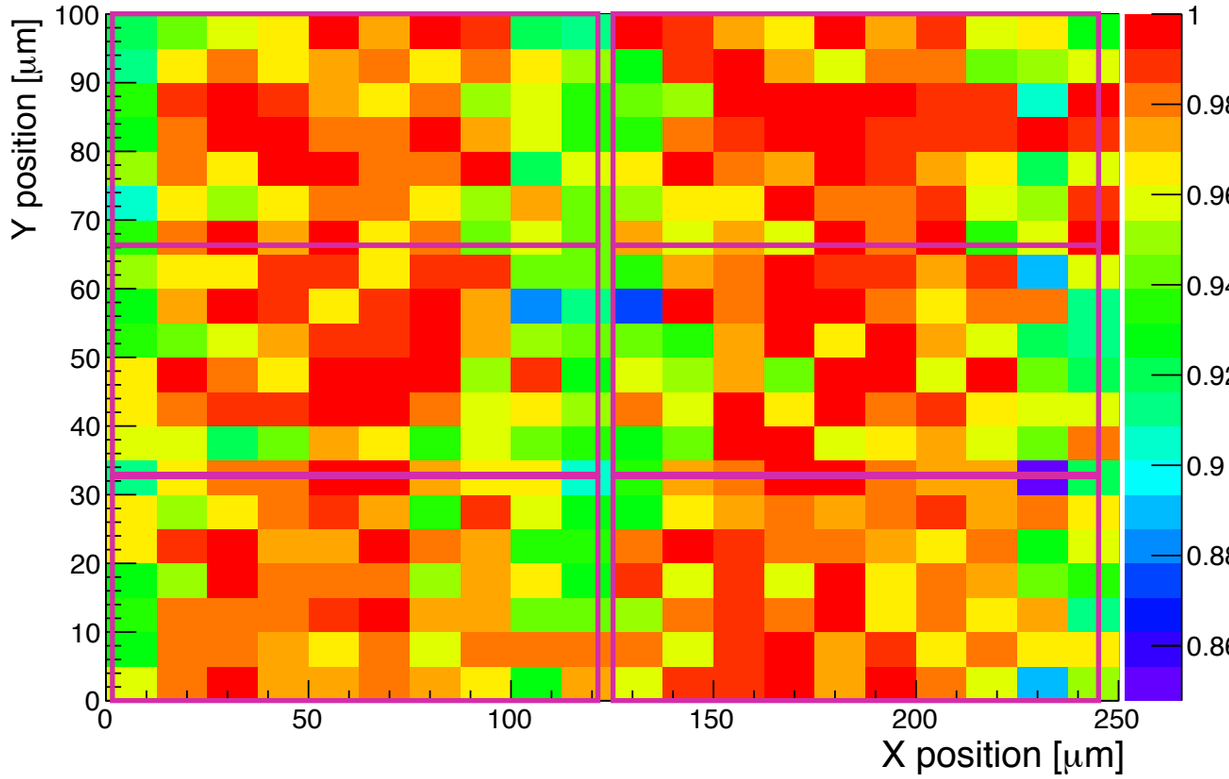
v4 InPixel eff.

402, unIrradiated
Bias 12 V, Th 0.84 V



Possible misalignment on Y axis observed

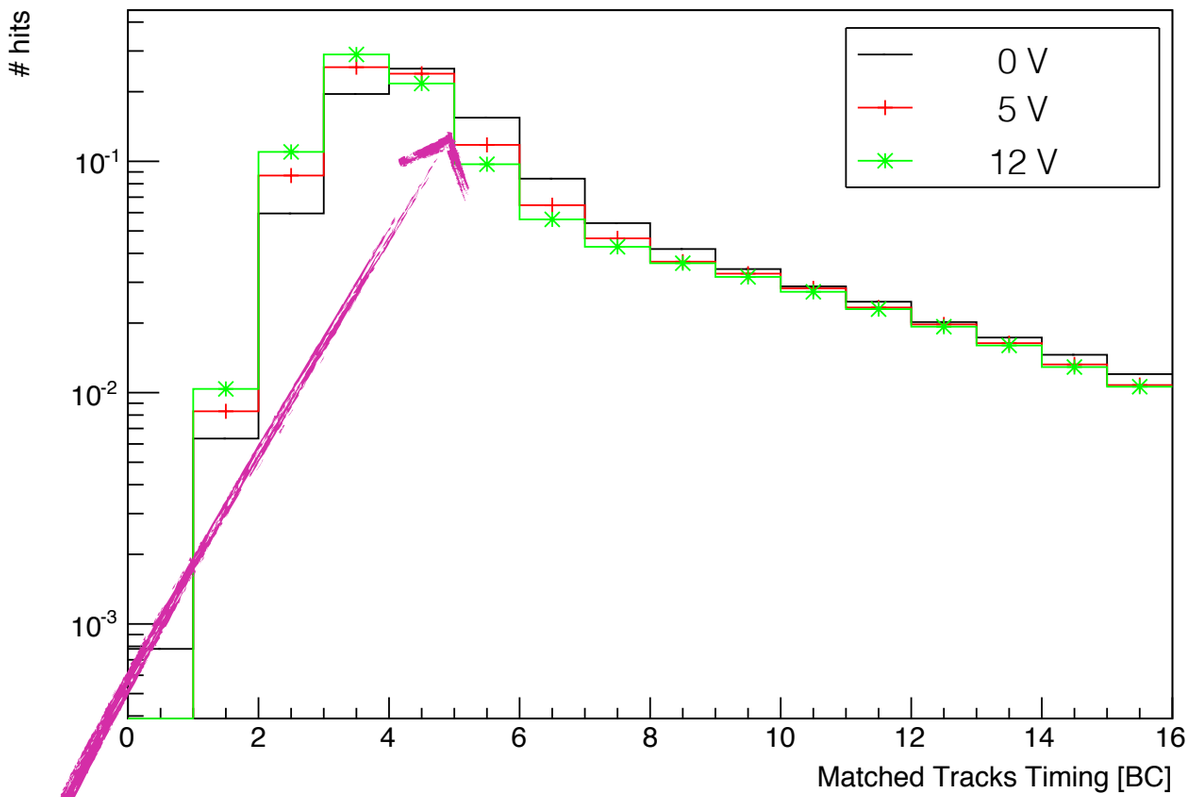
404, 10^{15} n_{eq}/cm^2
Bias 30 V, Th 0.84V



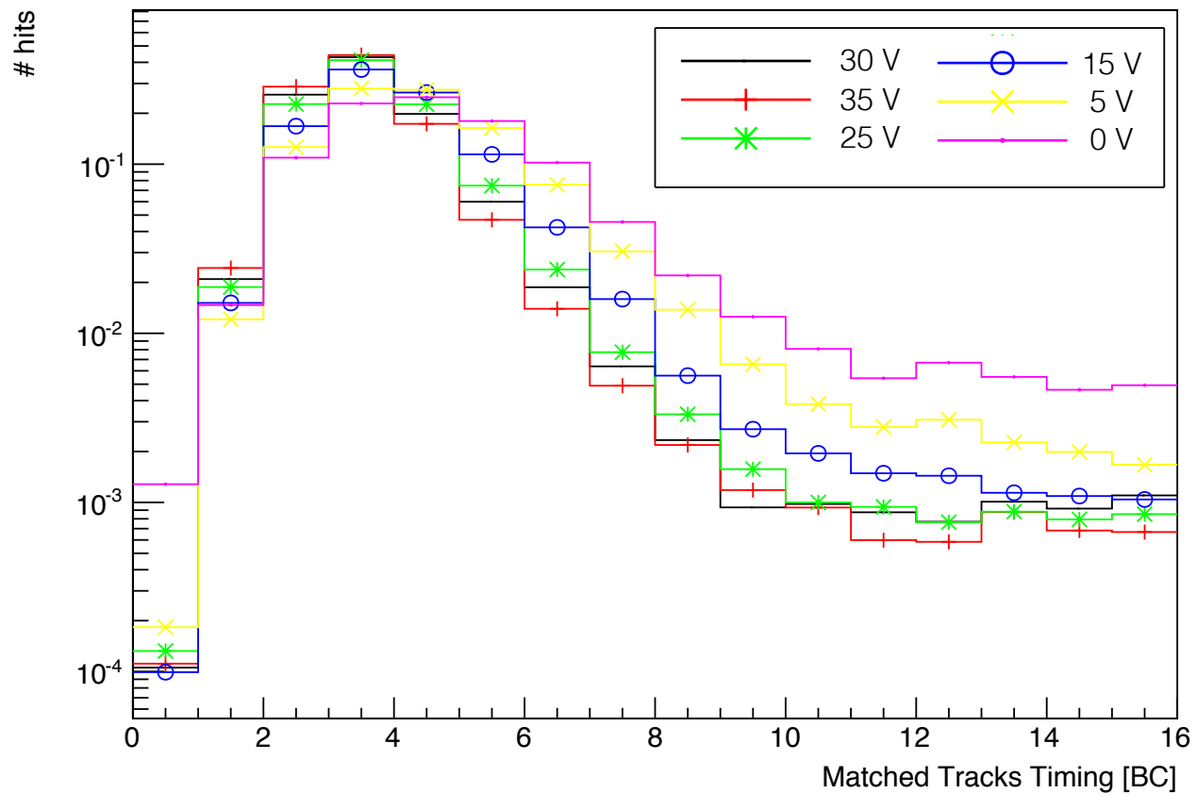
InPixel lower efficiency in the HVCMOS pixel boundaries

v4 Timing vs Bias V.

402, unIrradiated
Th 0.84 V



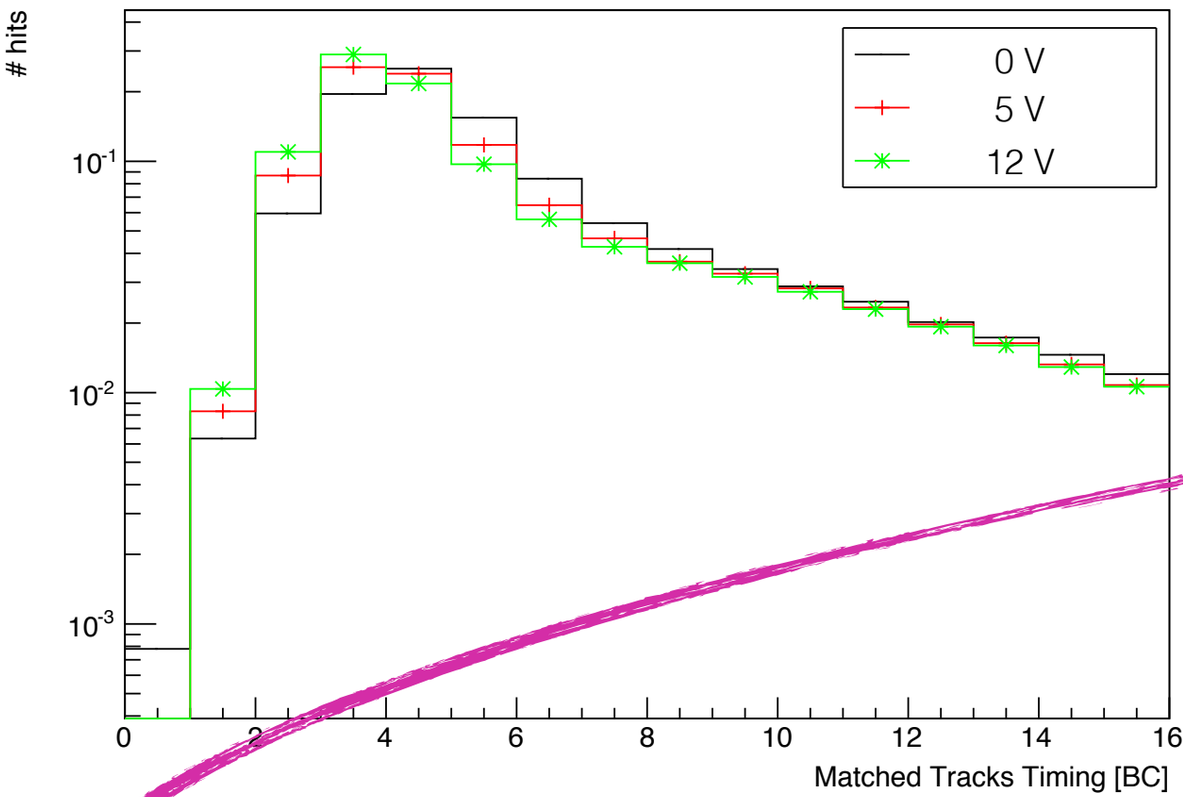
404, 10^{15} n_{eq}/cm^2
Th 0.84V



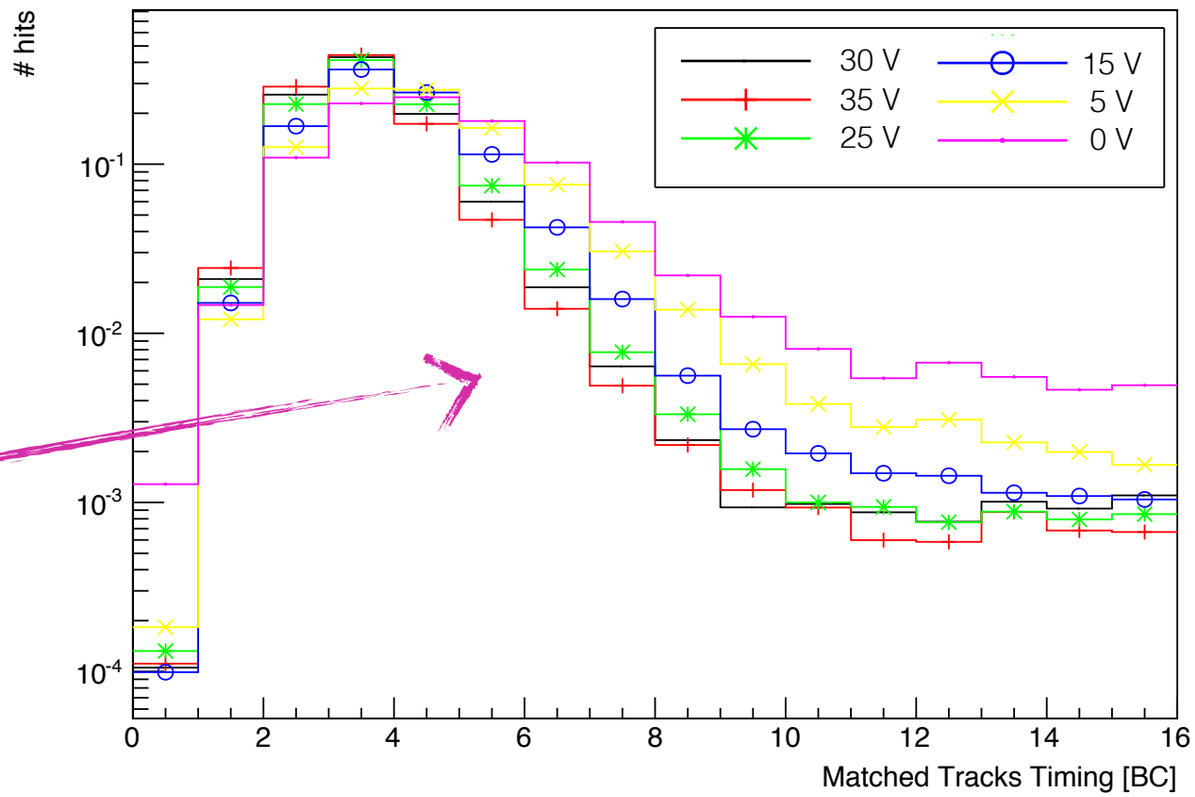
Higher Bias show sharper timing distributions

v4 Timing vs Bias V.

402, unIrradiated
Th 0.84 V



404, 10^{15} n_{eq}/cm^2
Th 0.84V

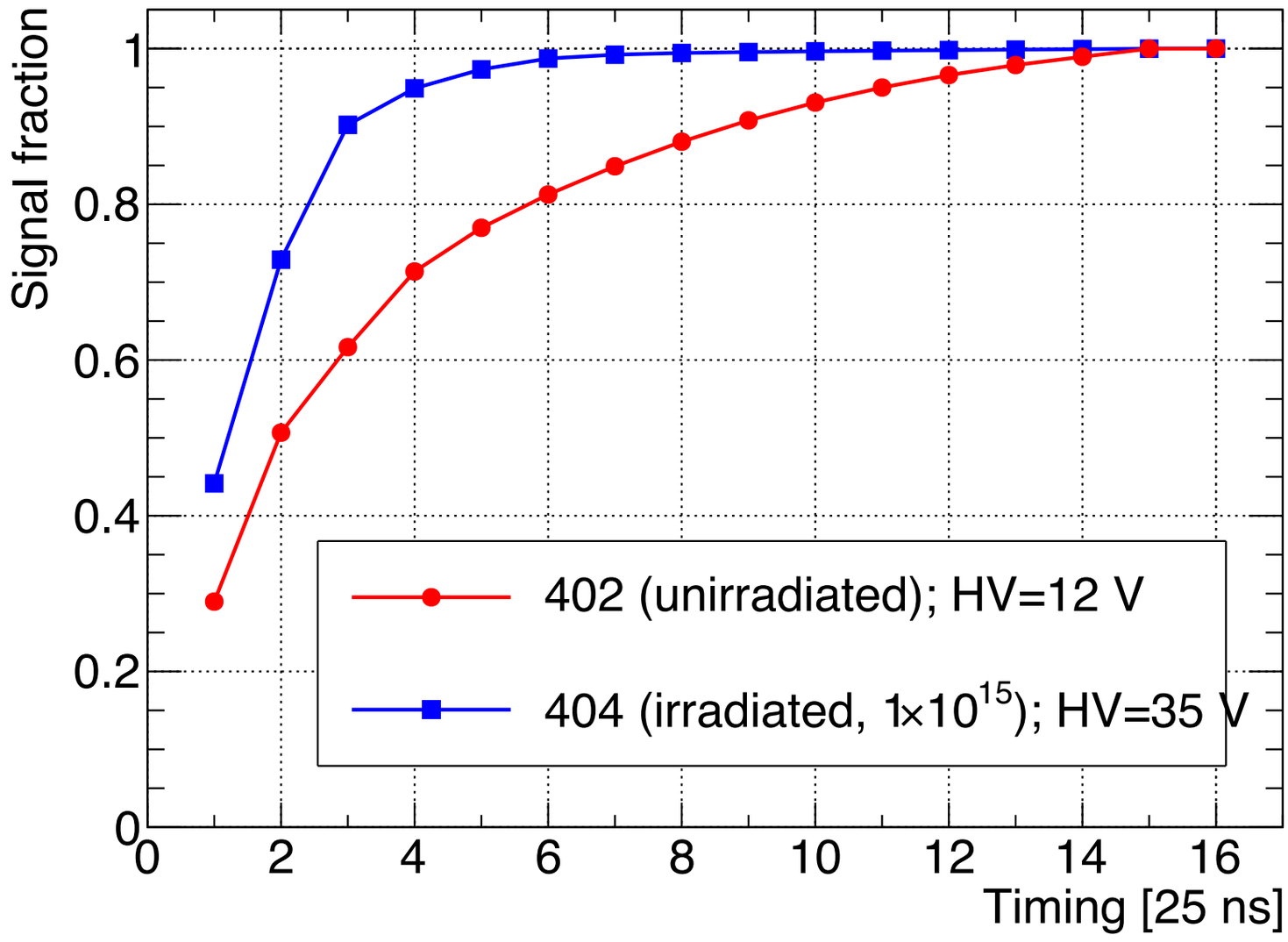


Higher Bias show sharper timing distributions

Higher Bias show smaller tails, Indication for possible diffusion effect.

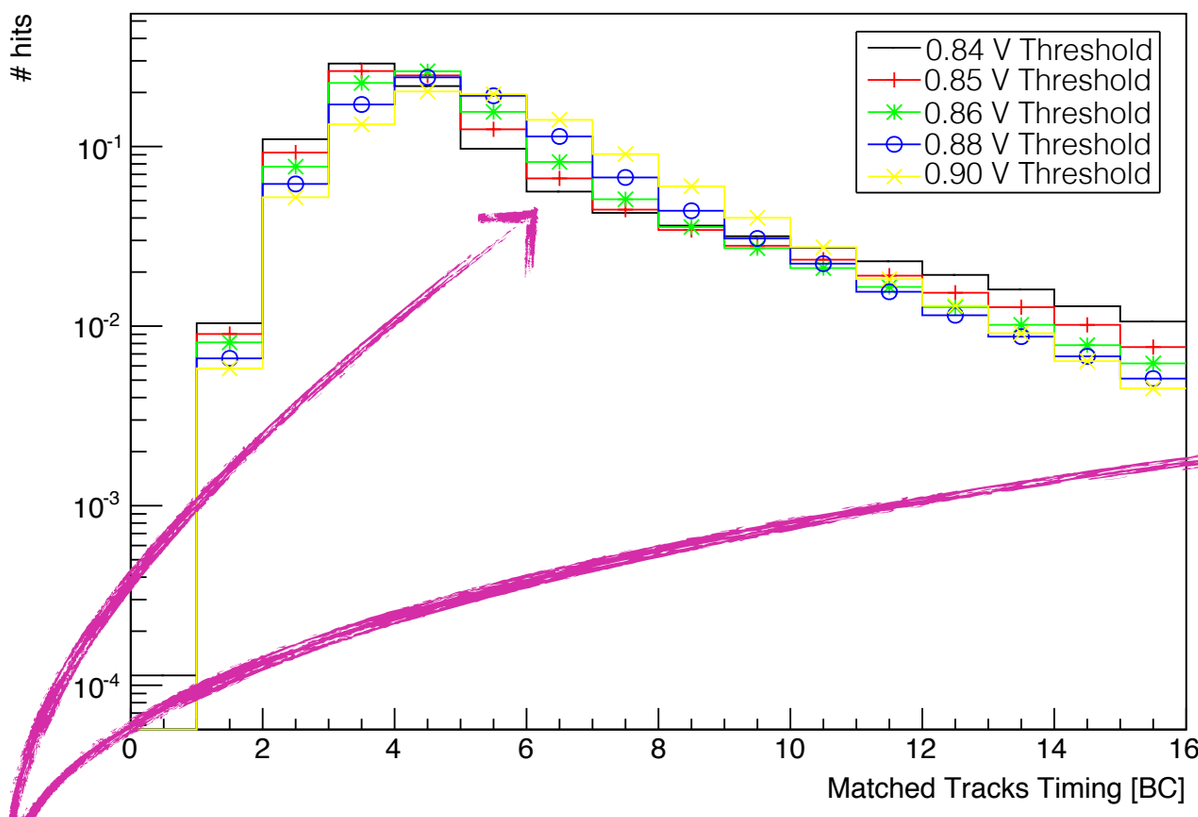
v4 Timing vs Bias V.

Integrated signal fraction over X of the most populated bins, from 1 single BC to 16 BC in 25 ns units

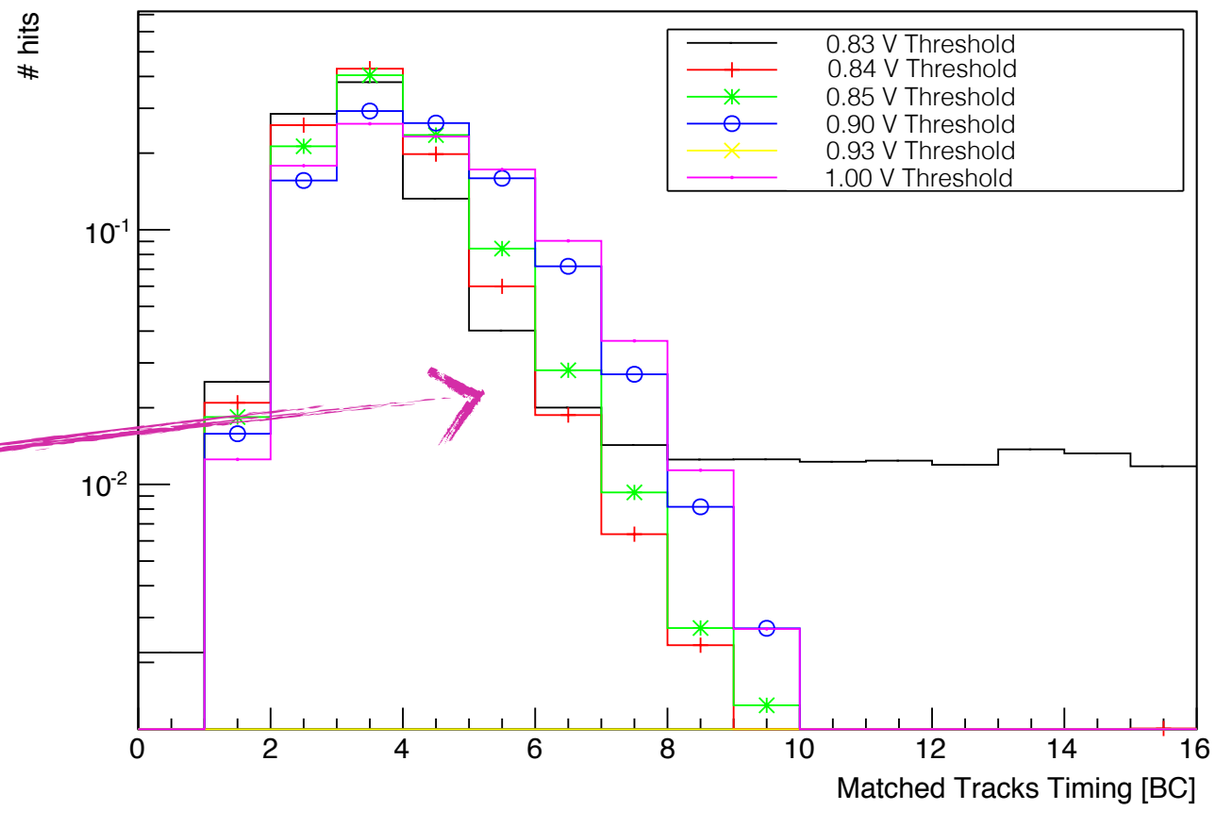


v4 Timing vs Threshold.

402, unIrradiated
Th 0.84 V



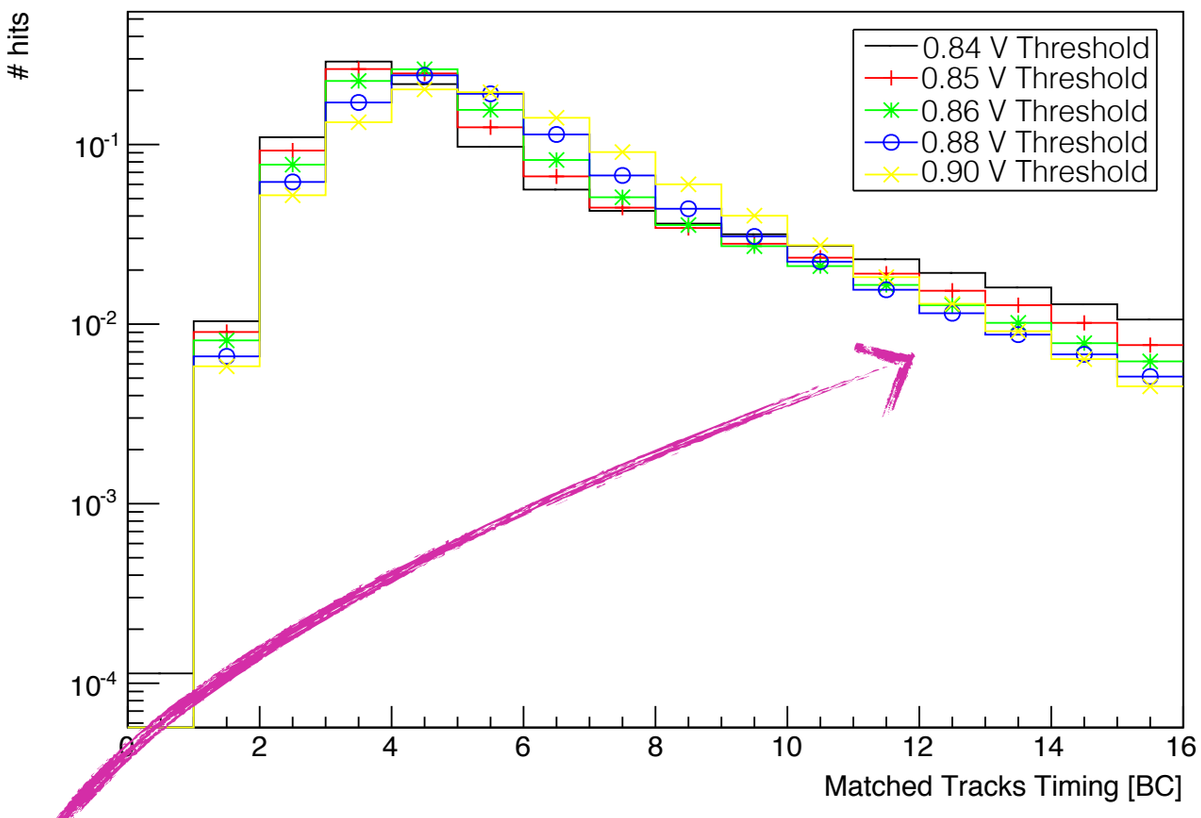
404, 10^{15} n_{eq}/cm^2, Bias 30 V



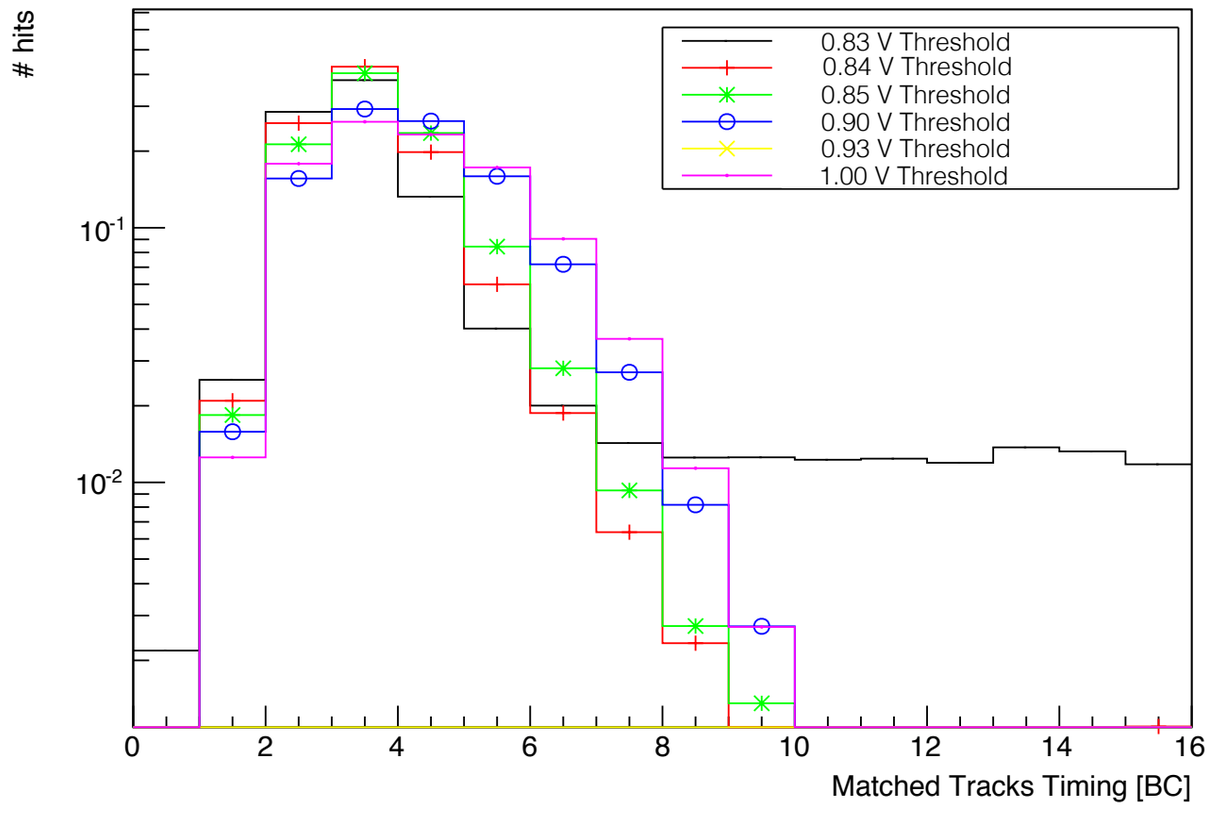
Low threshold show smaller tails, indication of a time-walk effect.

v4 Timing vs Threshold.

402, unIrradiated
Th 0.84 V

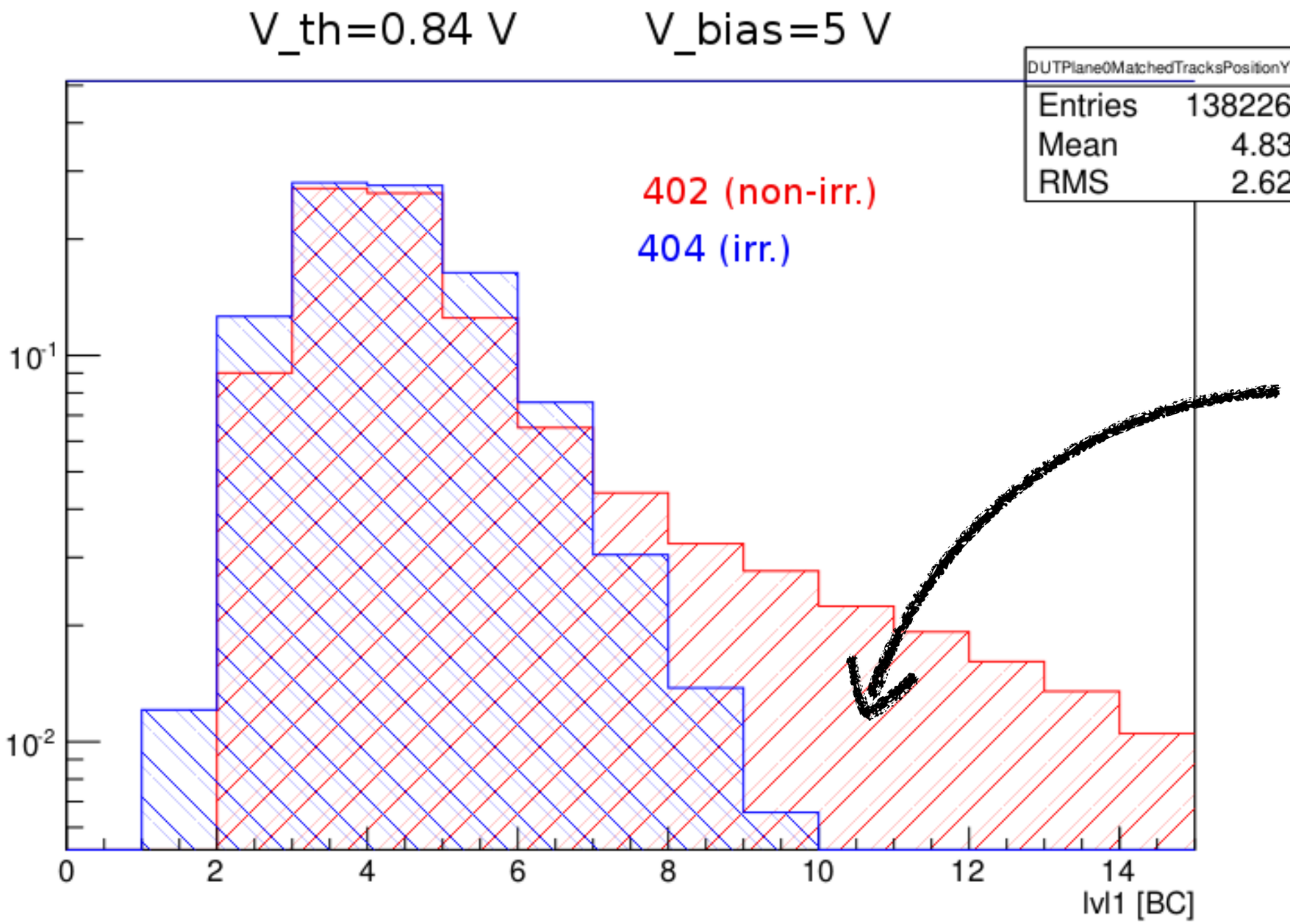


404, 10^{15} n_{eq}/cm^2, Bias 30 V



Low threshold show smaller tails, indication of a time-walk effect.
High threshold reduces the diffusion contribution (low Amplitude).

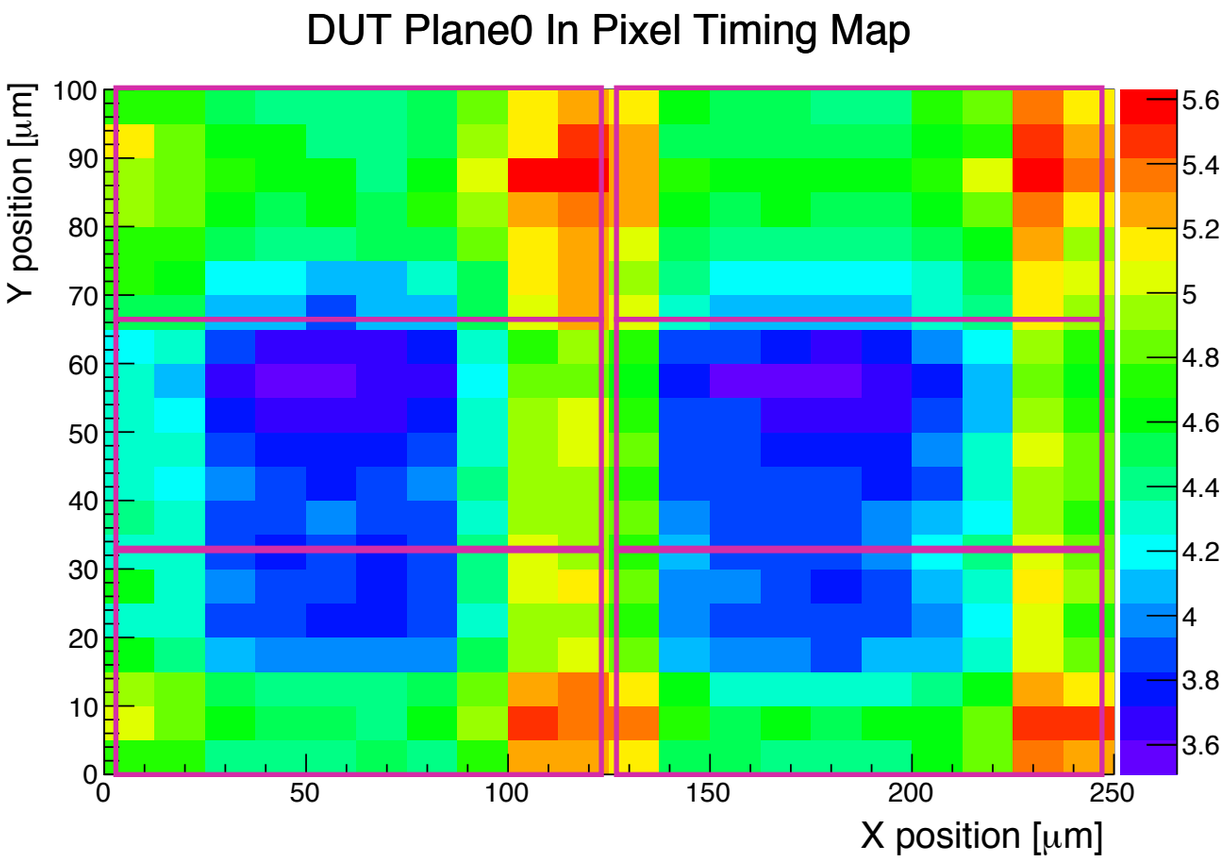
v4 Timing comparison



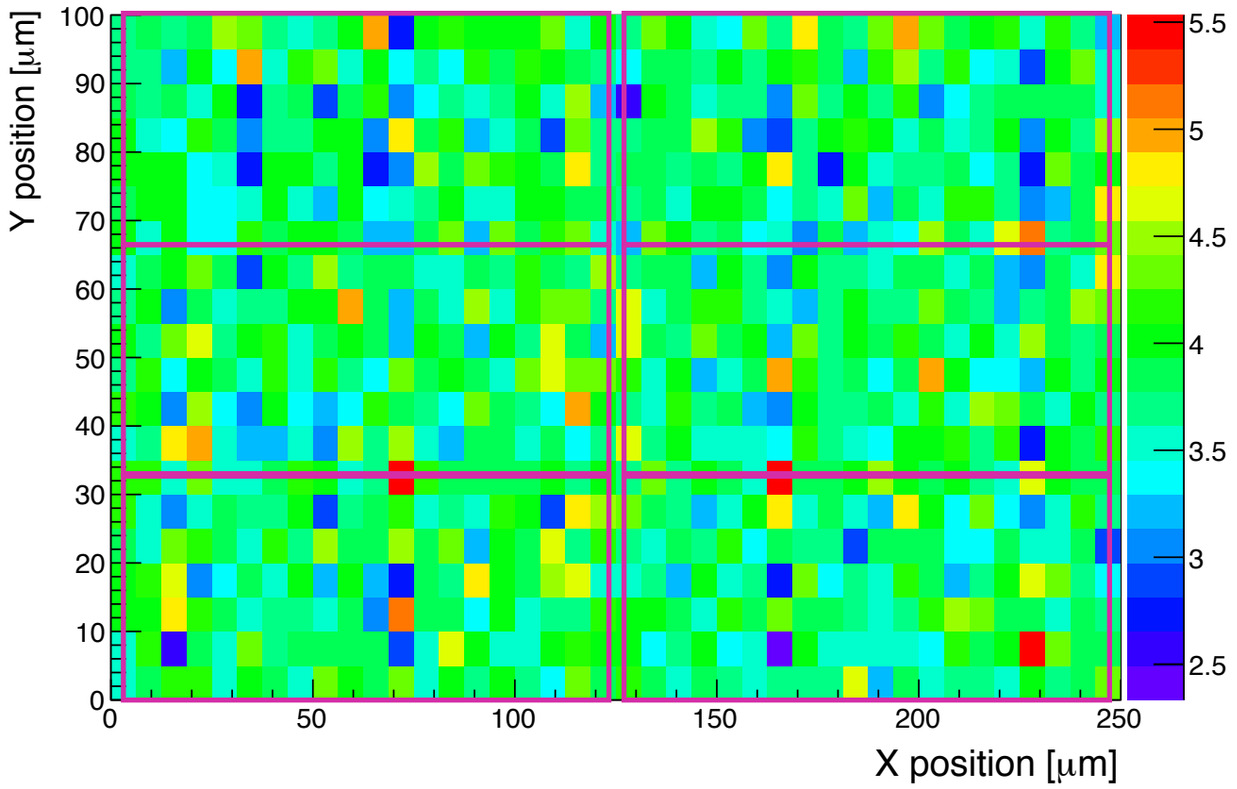
Diffusion component

v4 InPixel Timing

402, unIrradiated
Bias 12 V, Th 0.84 V



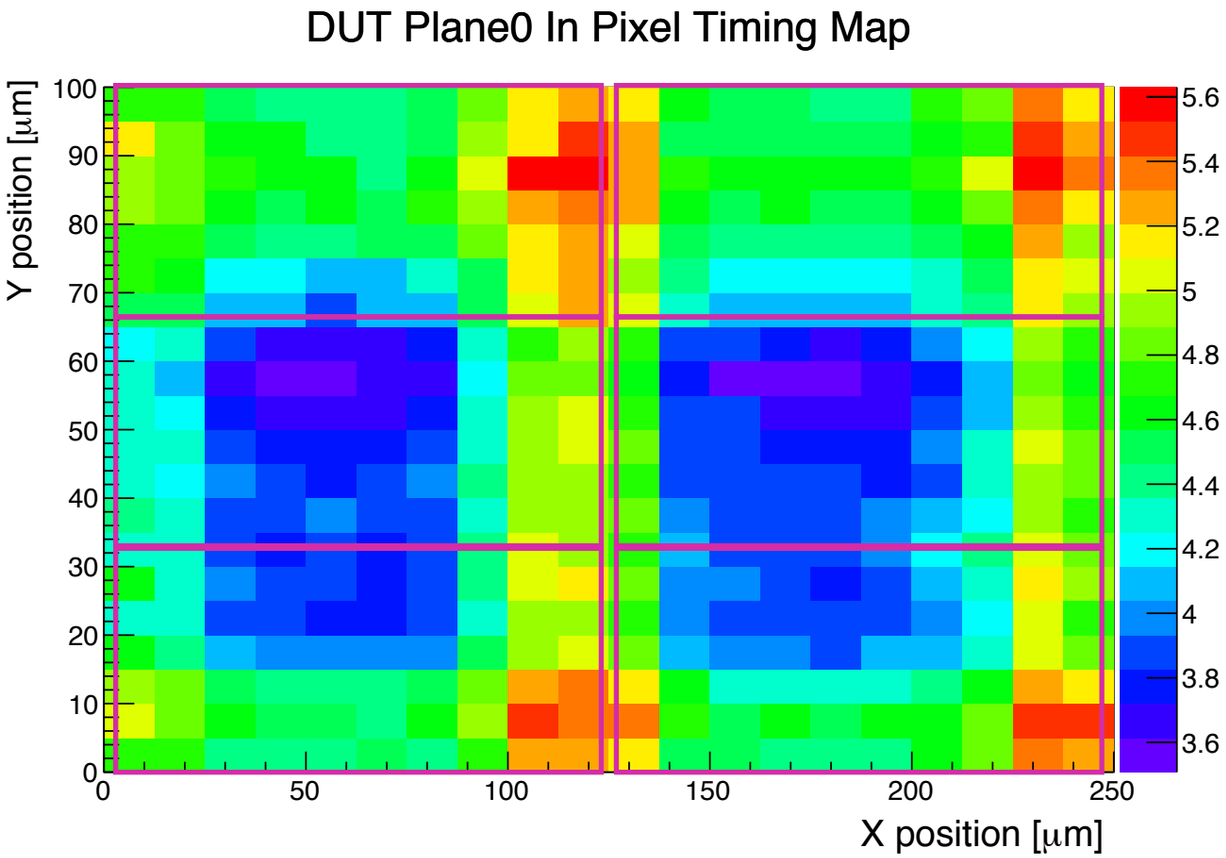
404, 10^{15} n_{eq}/cm^2
Bias 30 V, Th 0.84V

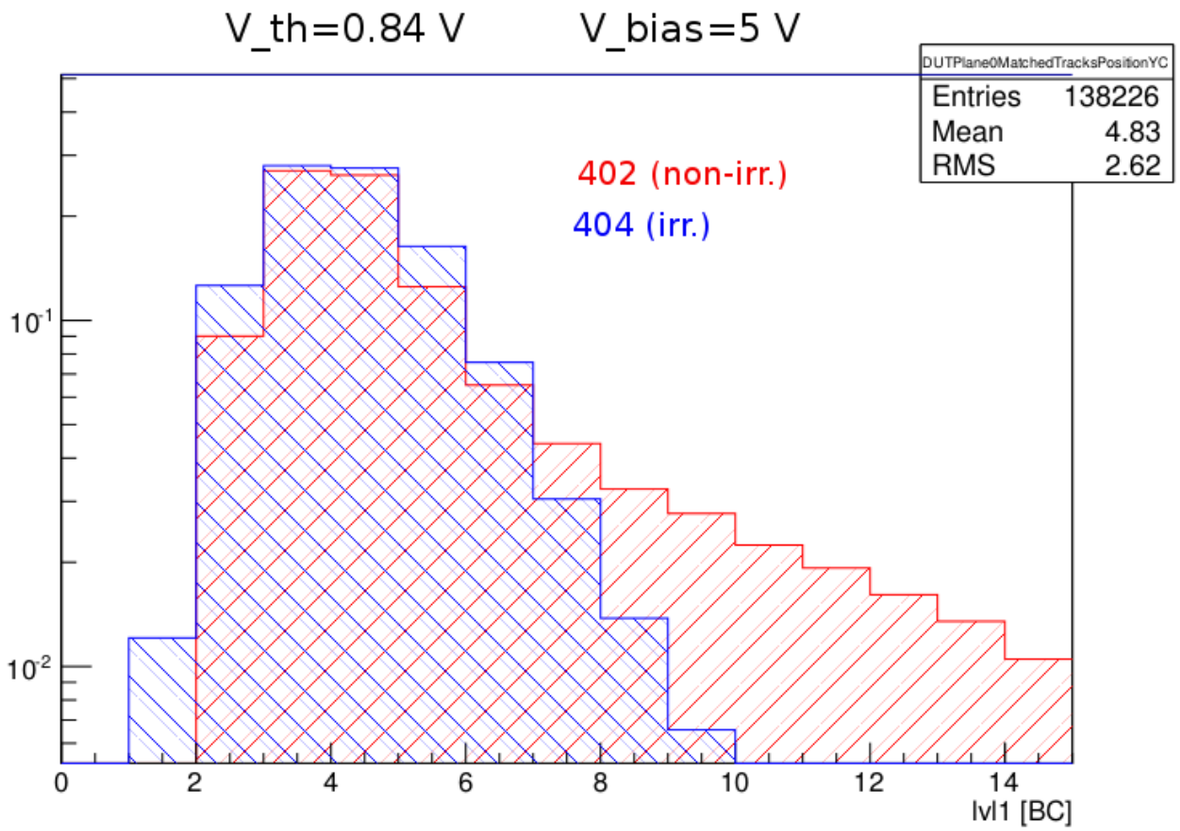


InPixel Timing inhomogeneities showing later events in the HVCMOS pixel boundaries. Not present on irradiated sample

v4 InPixel Timing

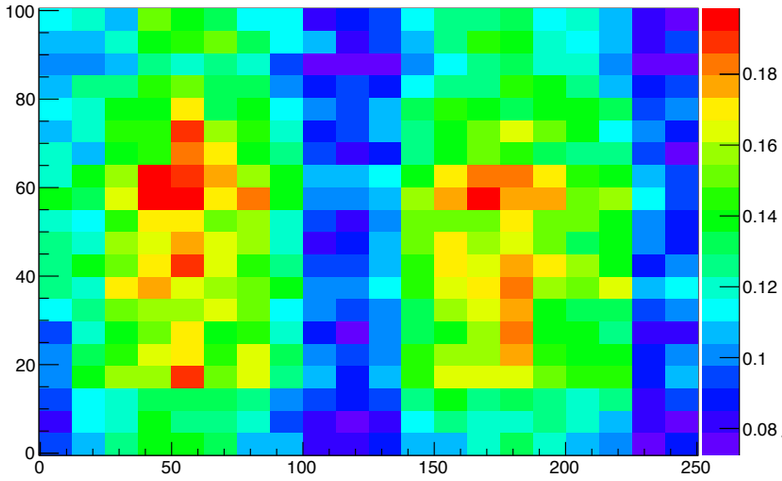
402, unIrradiated
Bias 12 V, Th 0.84 V

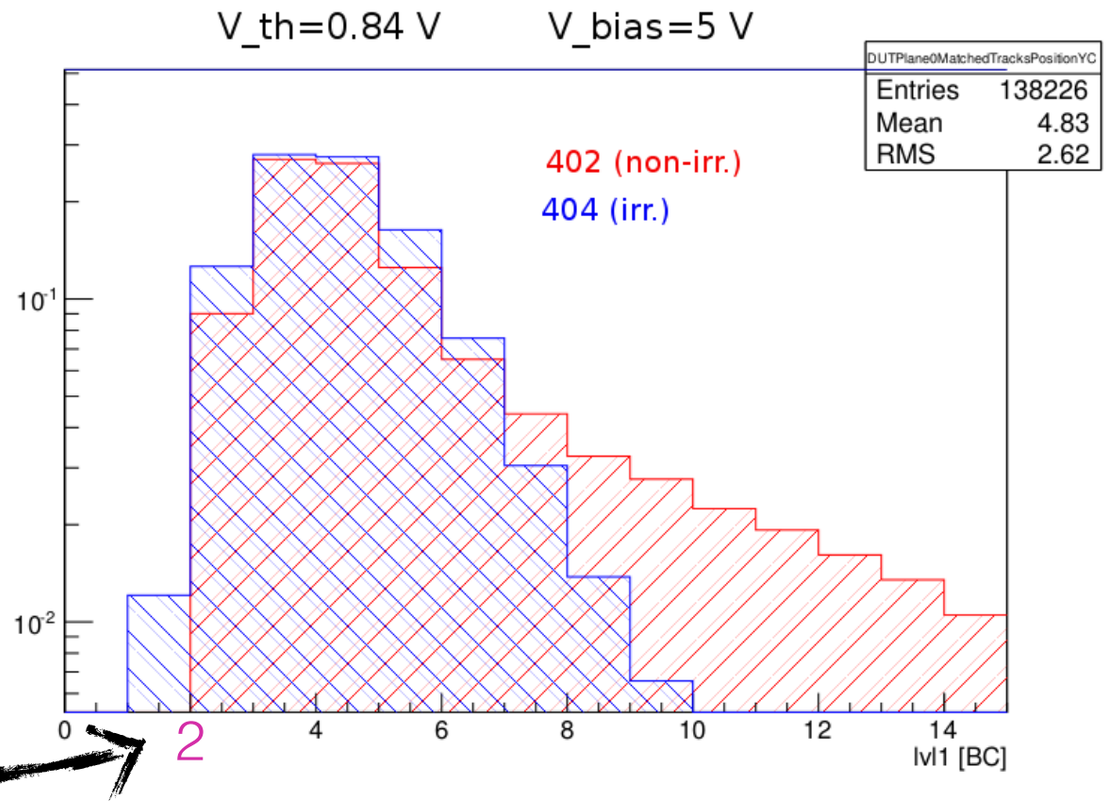




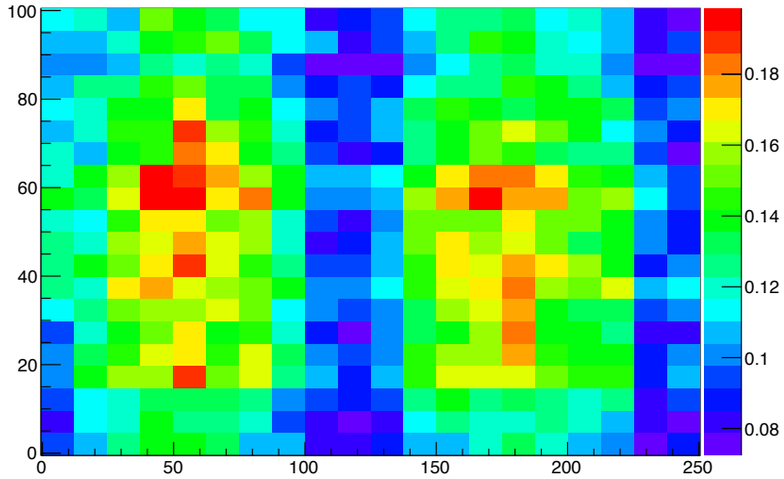
Observing this in pixel timing inhomogeneity for the unIrradiated sample and the presence of a tail at higher Lv1 values, we've decomposed the in pixel eft for each Lv1:

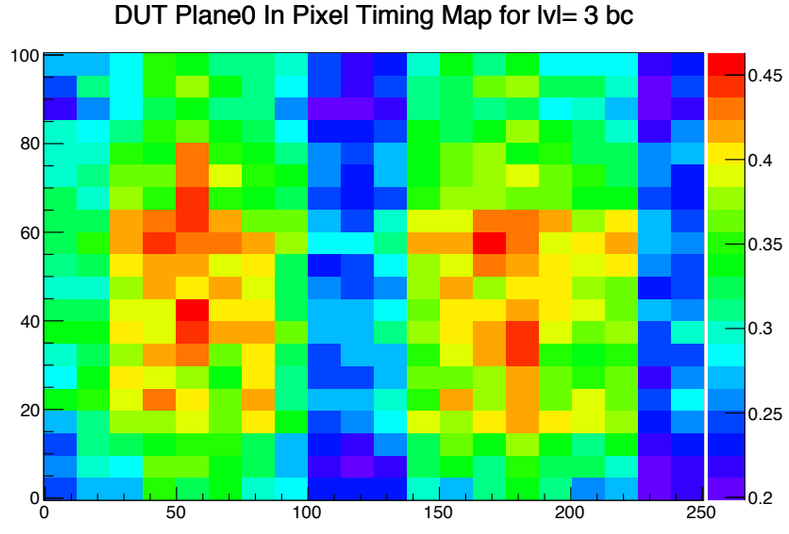
v4 InPixel Timing

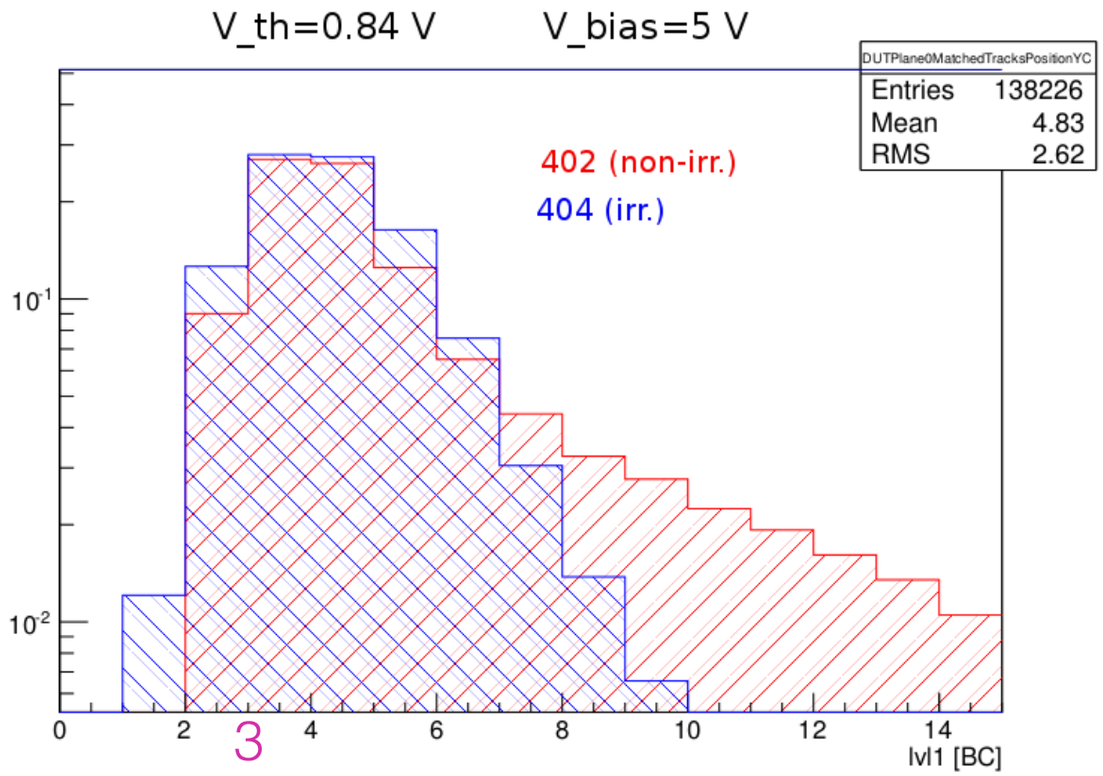




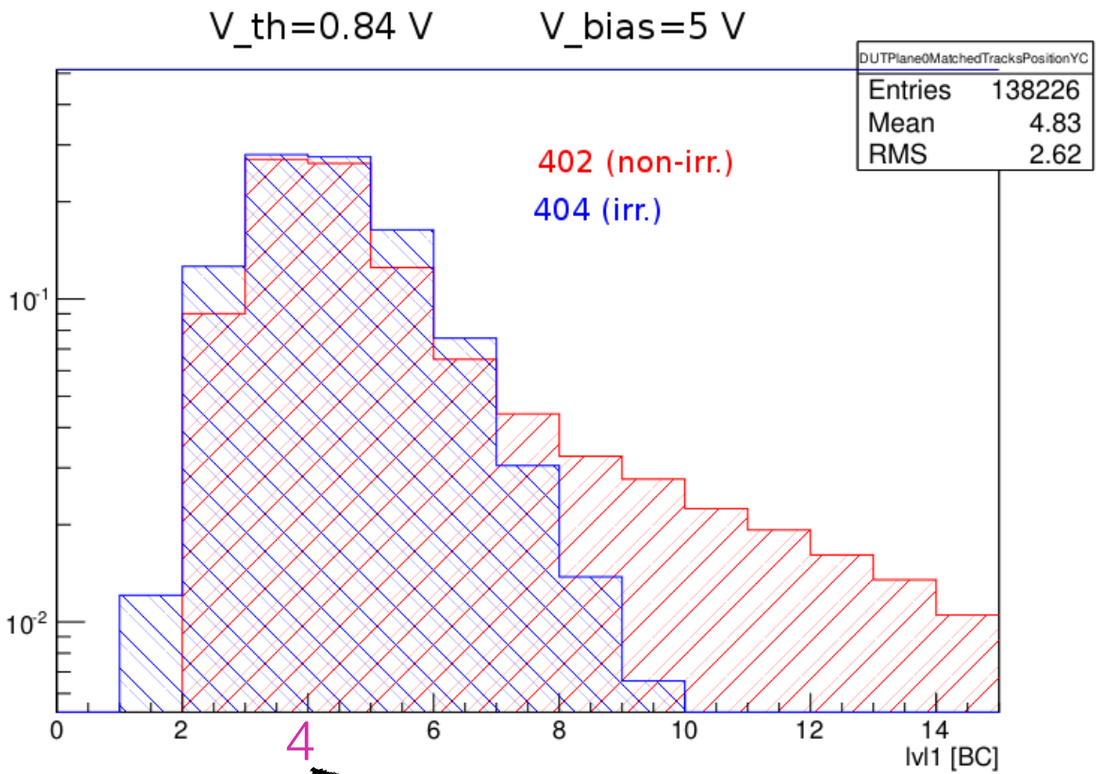
v4 InPixel Timing

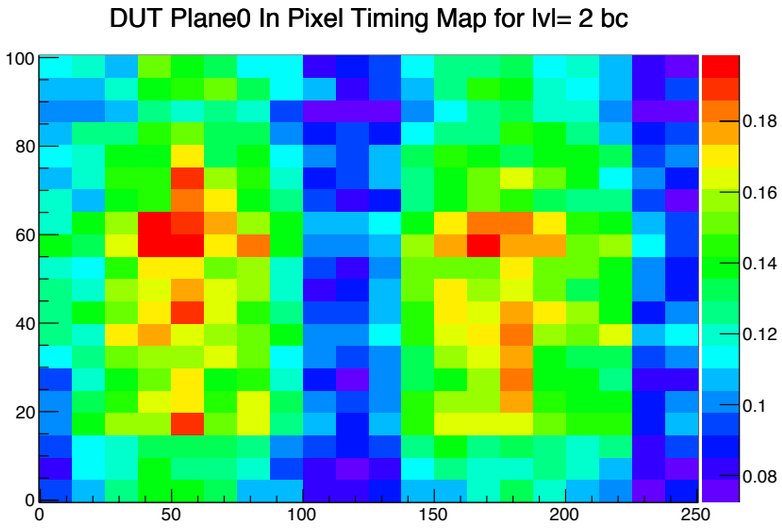


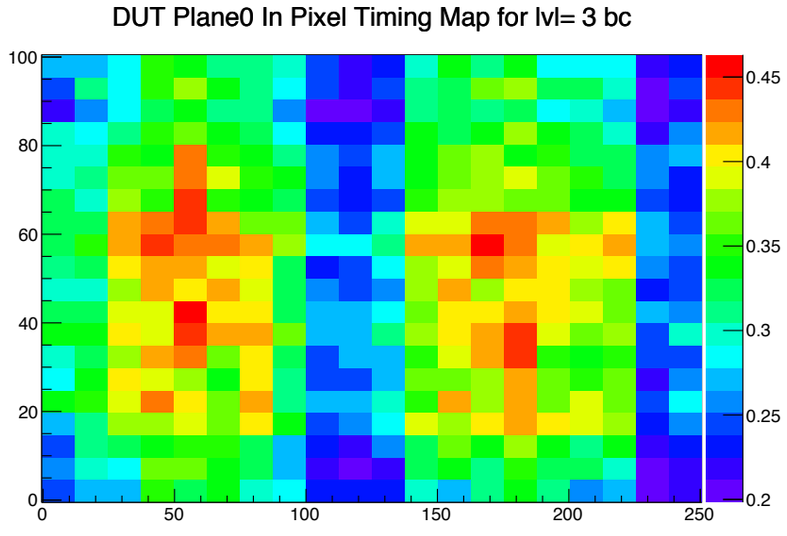


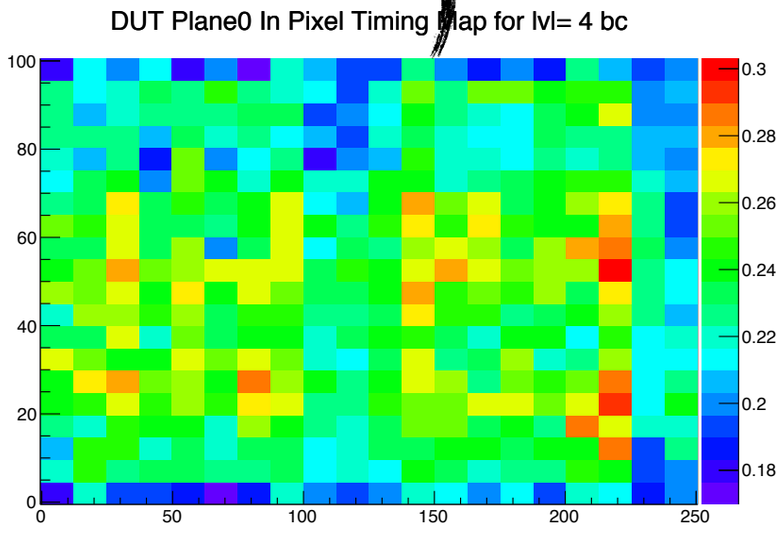


v4 InPixel Timing

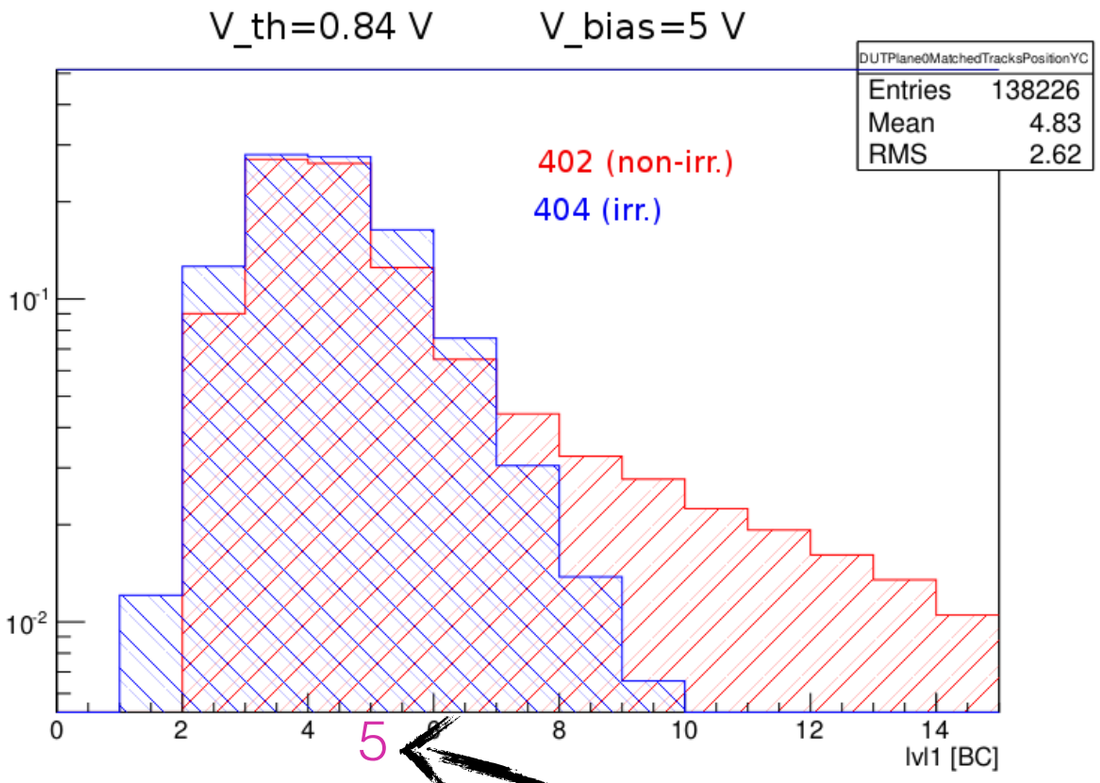


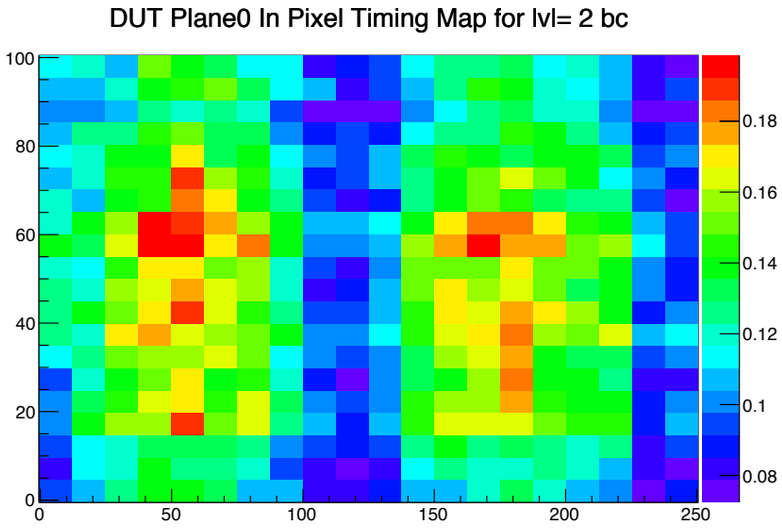


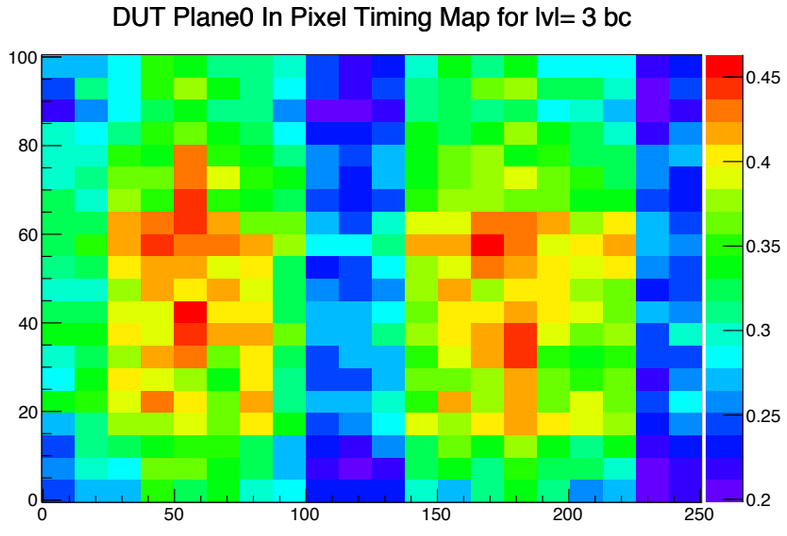


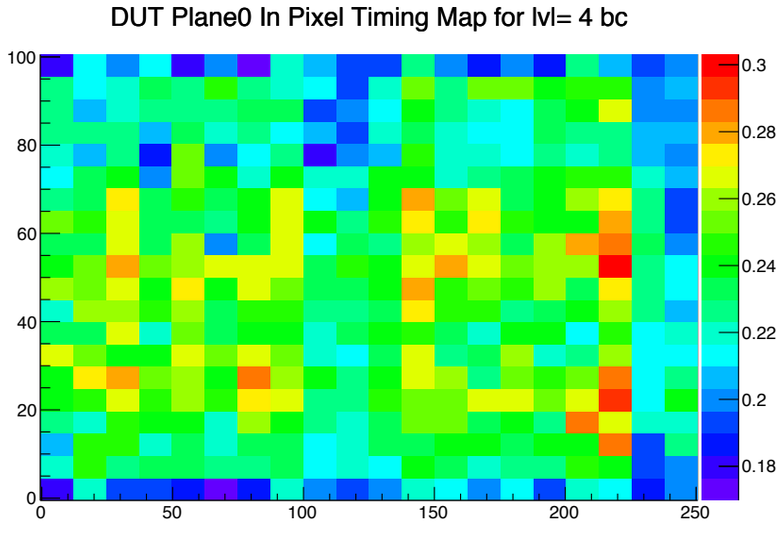


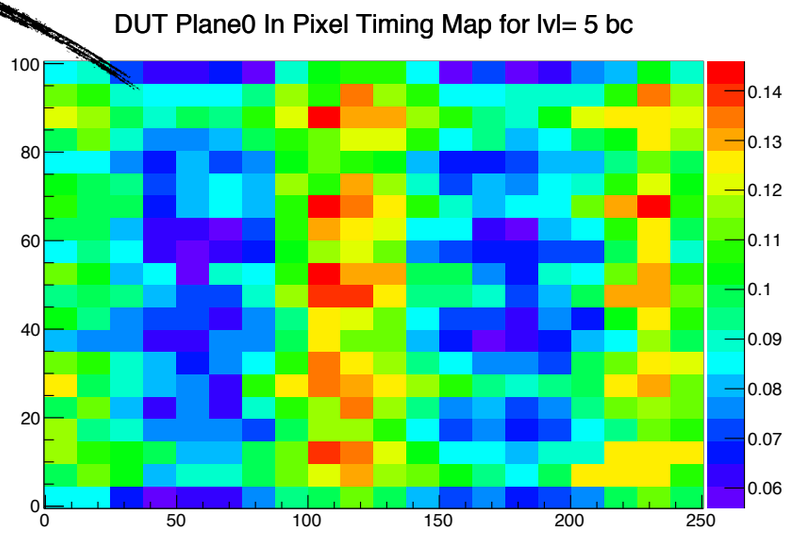
v4 InPixel Timing



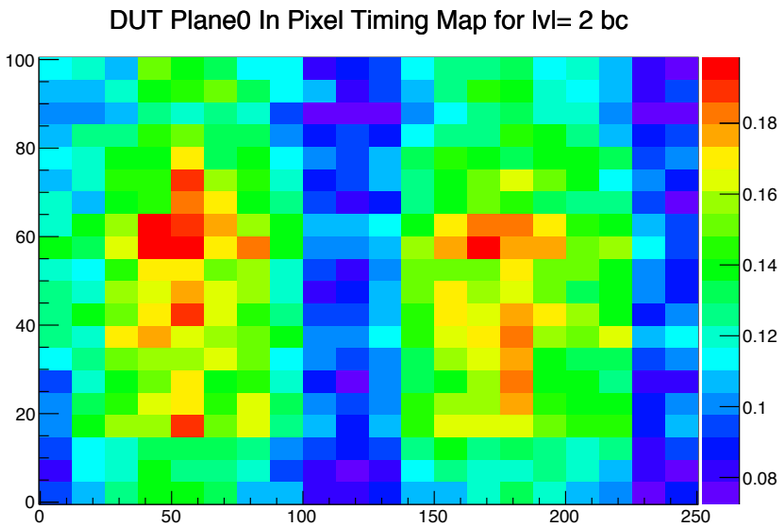




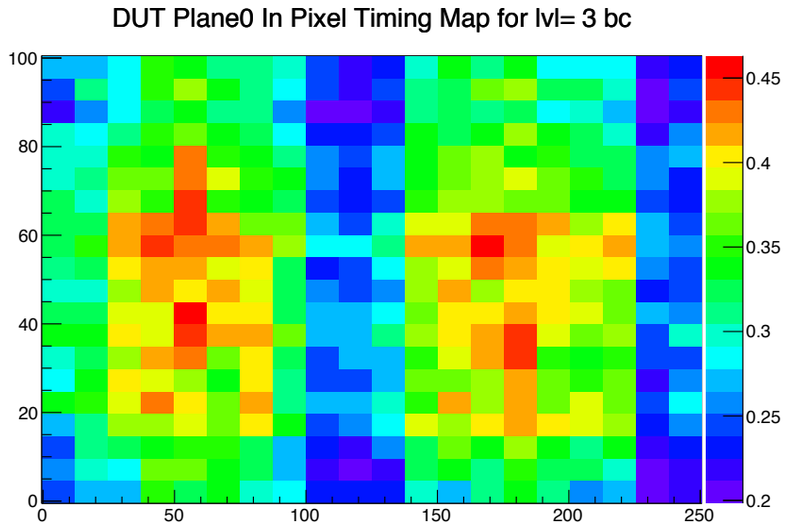


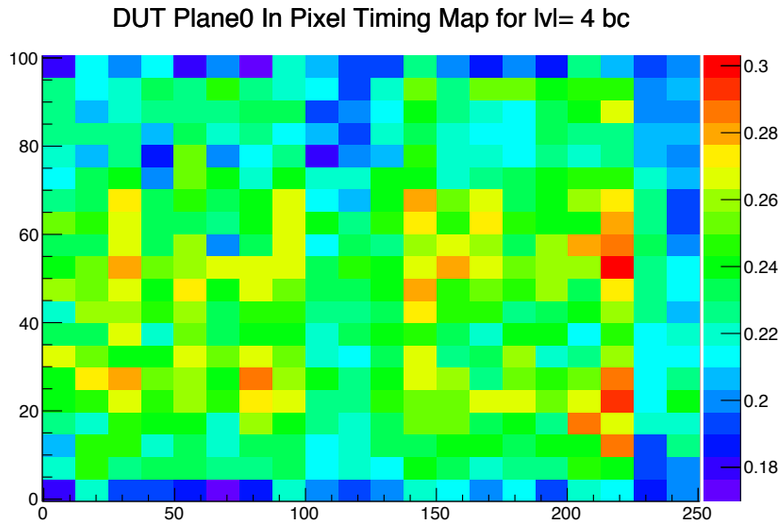


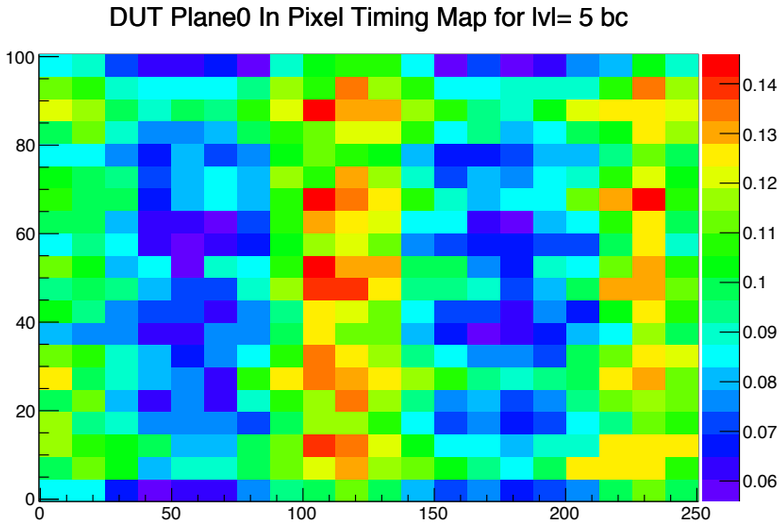
v4 InPixel Timing



Contribution from the pixel edges for the non-irradiated sample. Consistent with diffusion effects.

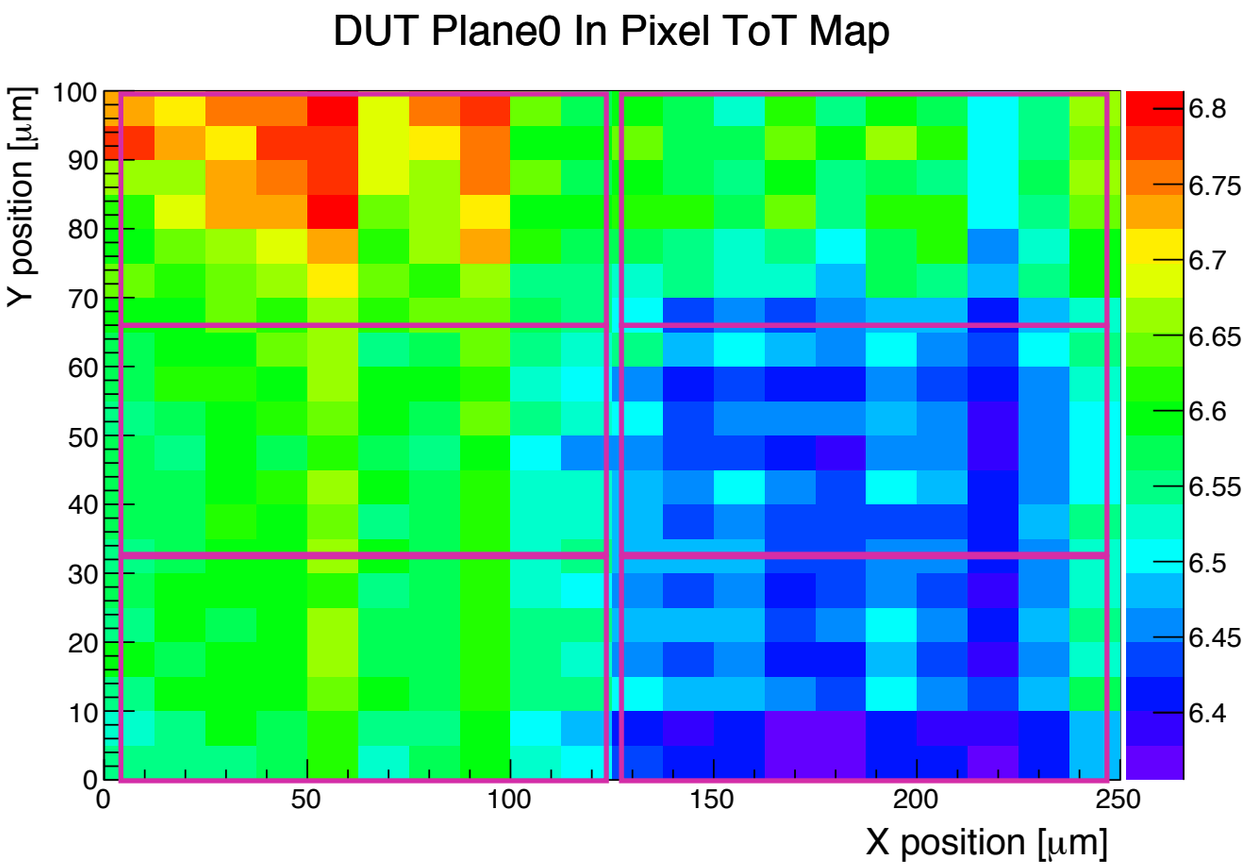




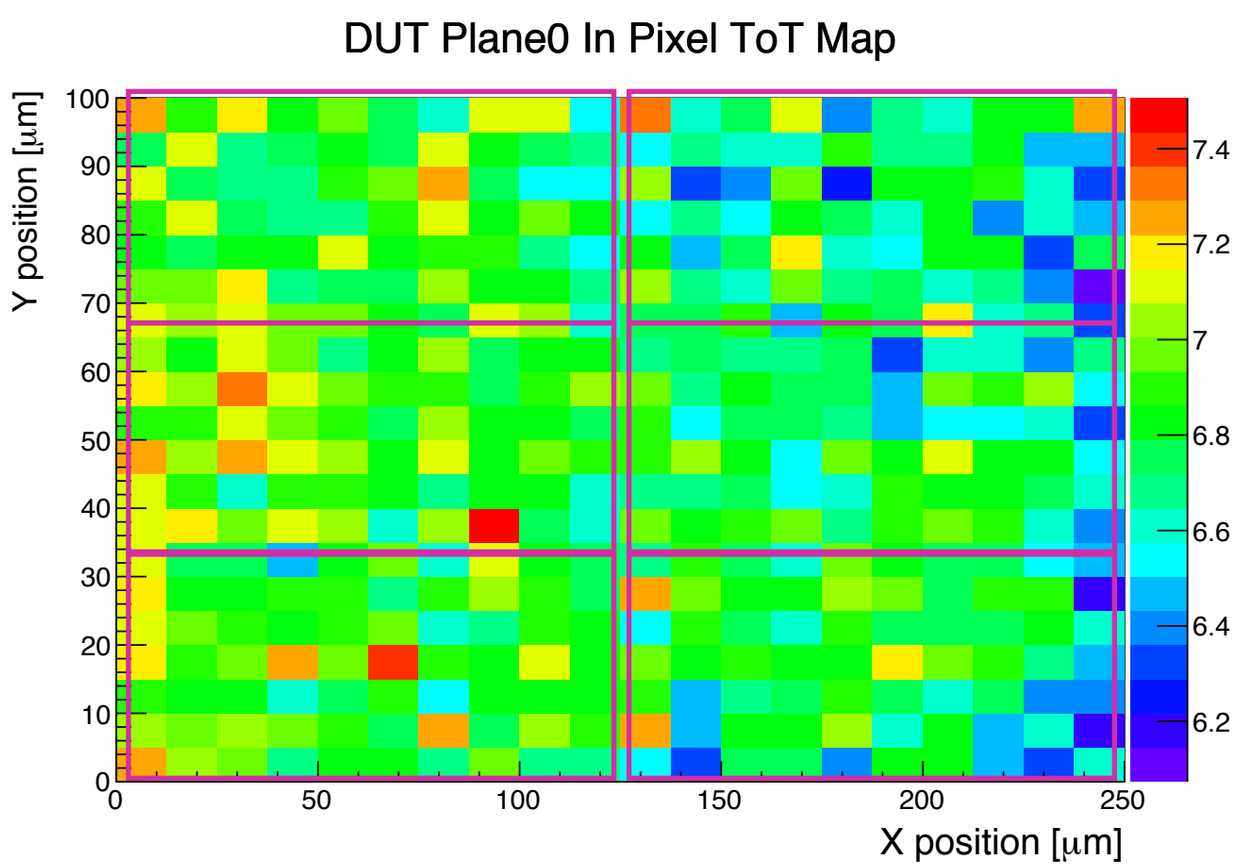


v4 ToT inPixel

402, unIrradiated
Bias 12 V, Th 0.84 V
Run: 3911 - 3915



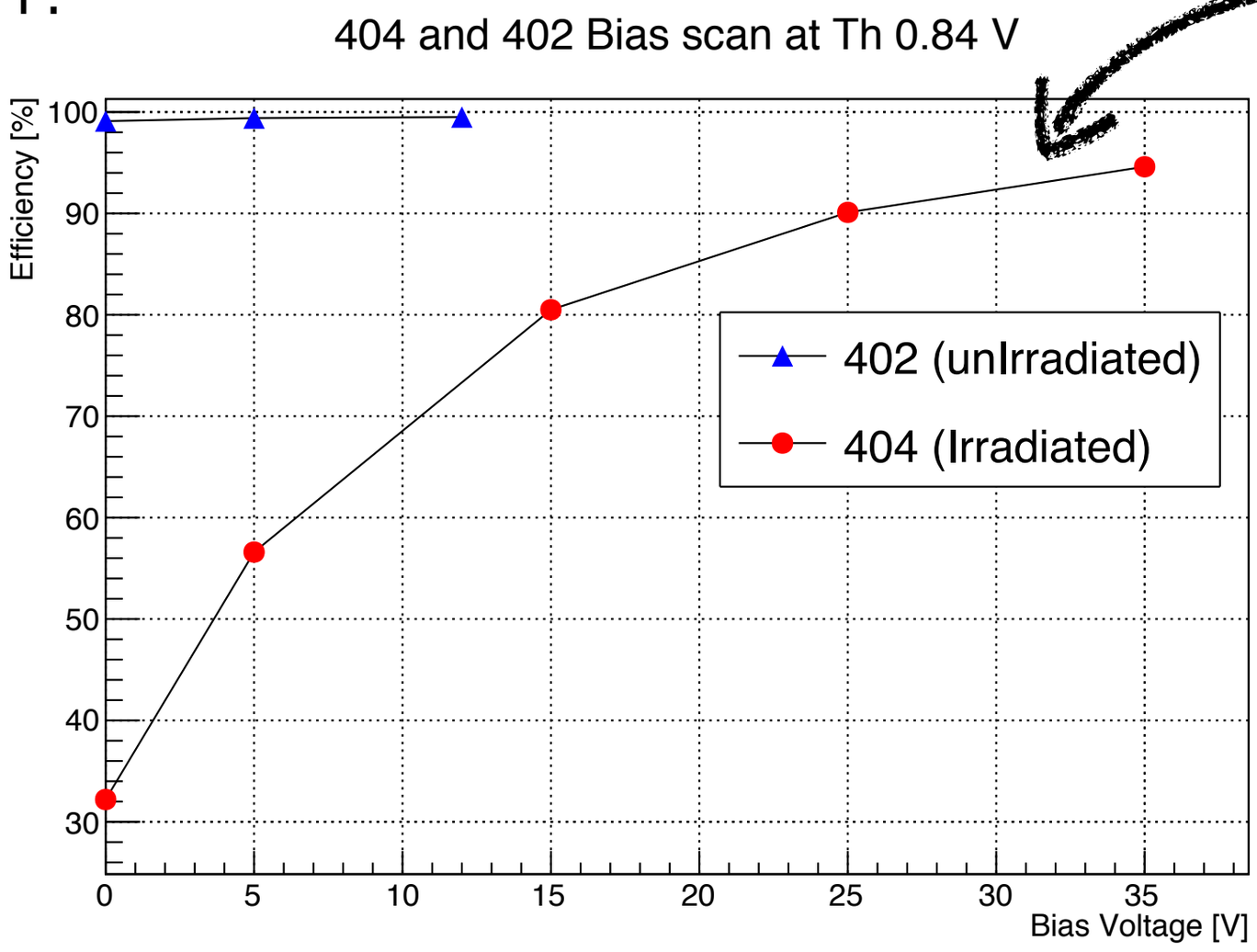
404, 10^{15} n_{eq}/cm^2
Bias 30 V, Th 0.84V
Run: 4074



InPixel ToT inhomogeneities, under investigation with the unit-cell design

Bias Scan

eff. for all Lv1:



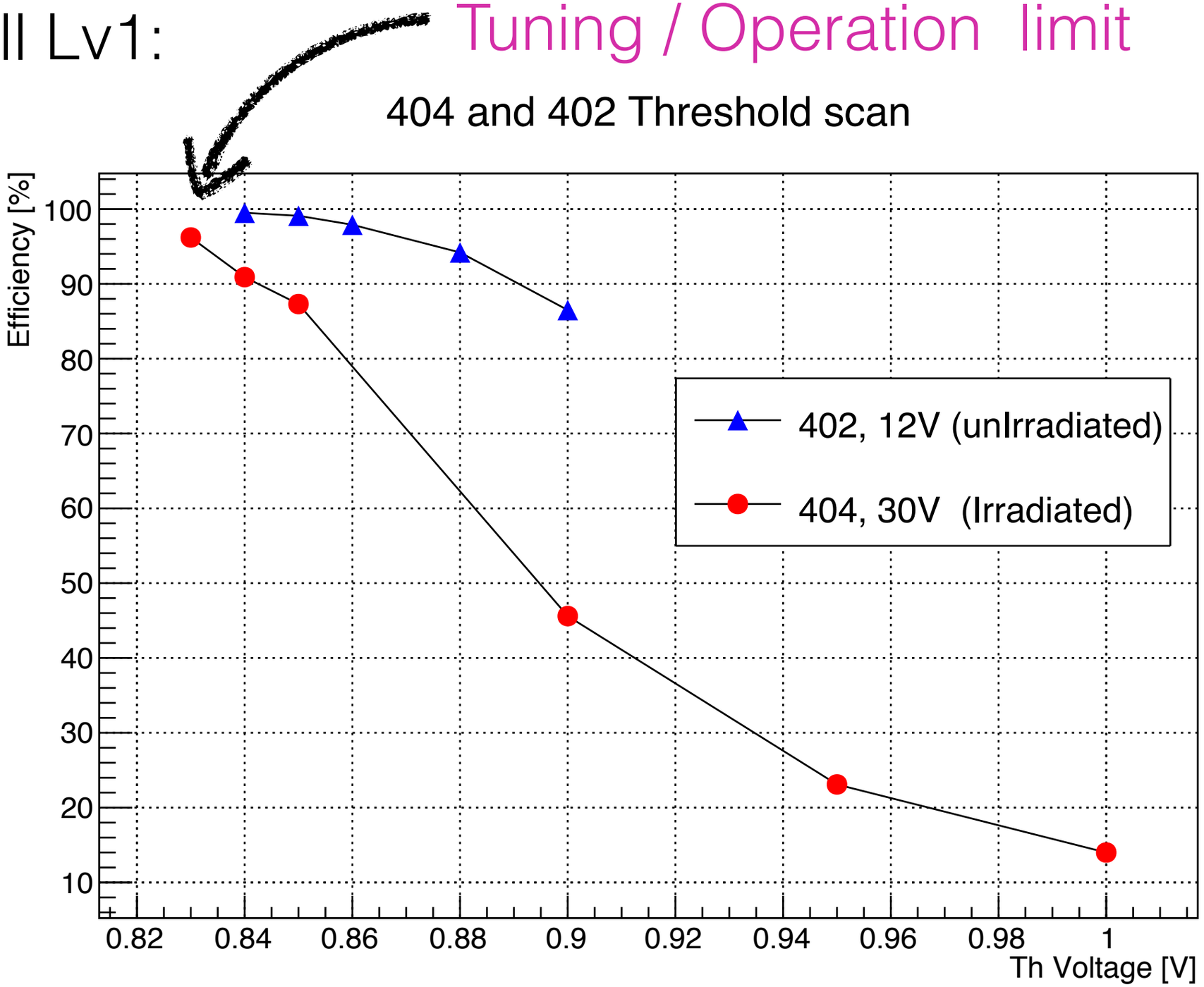
Need to reach the plateau ?

- Need to reach higher depletion voltages. Limited availability of prototypes during data taking.
- Full range will be scanned with source measurements on new samples.

Threshold Scan

eff. for all Lv1:

Tuning / Operation limit



Conclusions

- Efficiency before irradiation >99%

- Decrease of efficiency to 96% at 10^{15} n_{eq}/cm^2, irradiated samples efficiency can be increased with higher depletion voltages.

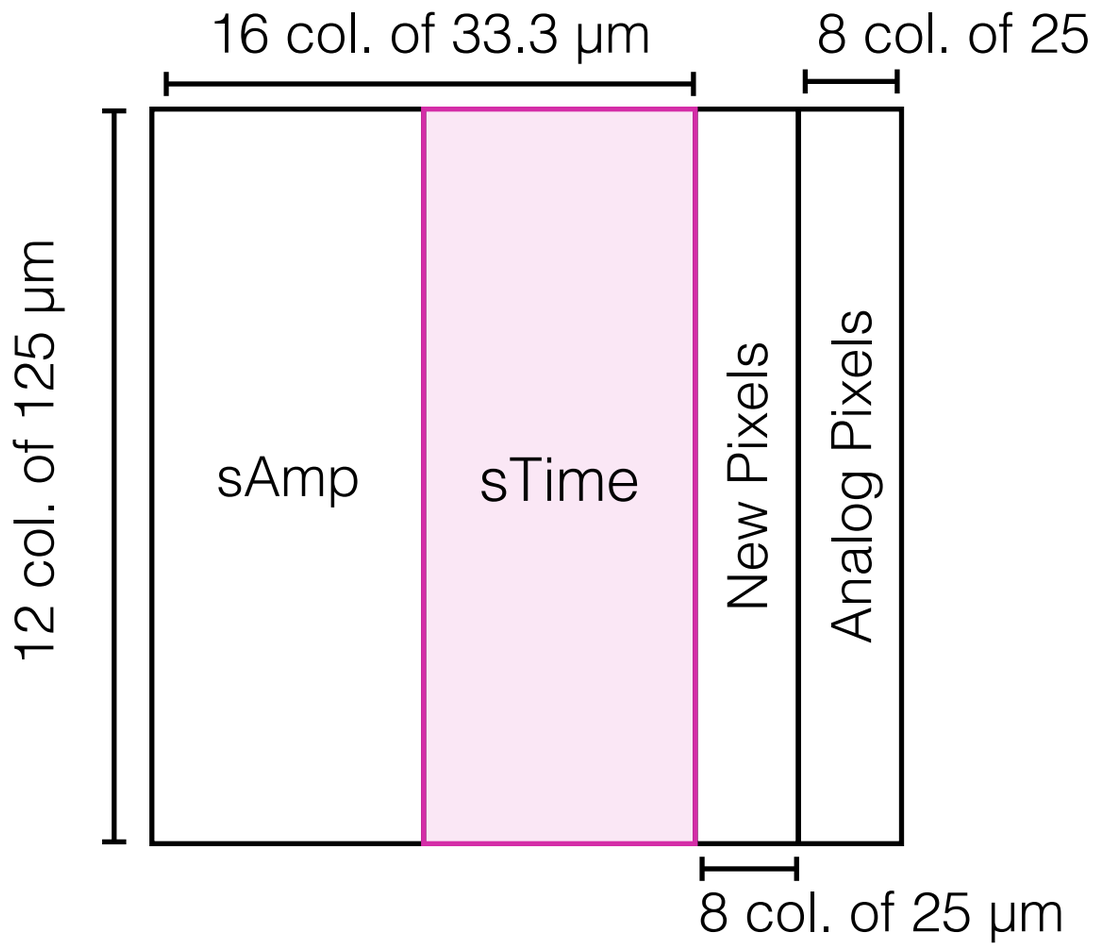
- Diffusion component seen for the unirradiated sample.

- Timing dependence on Threshold tuning indicates some time walk

- This time features will be addressed in next AMS prototypes.

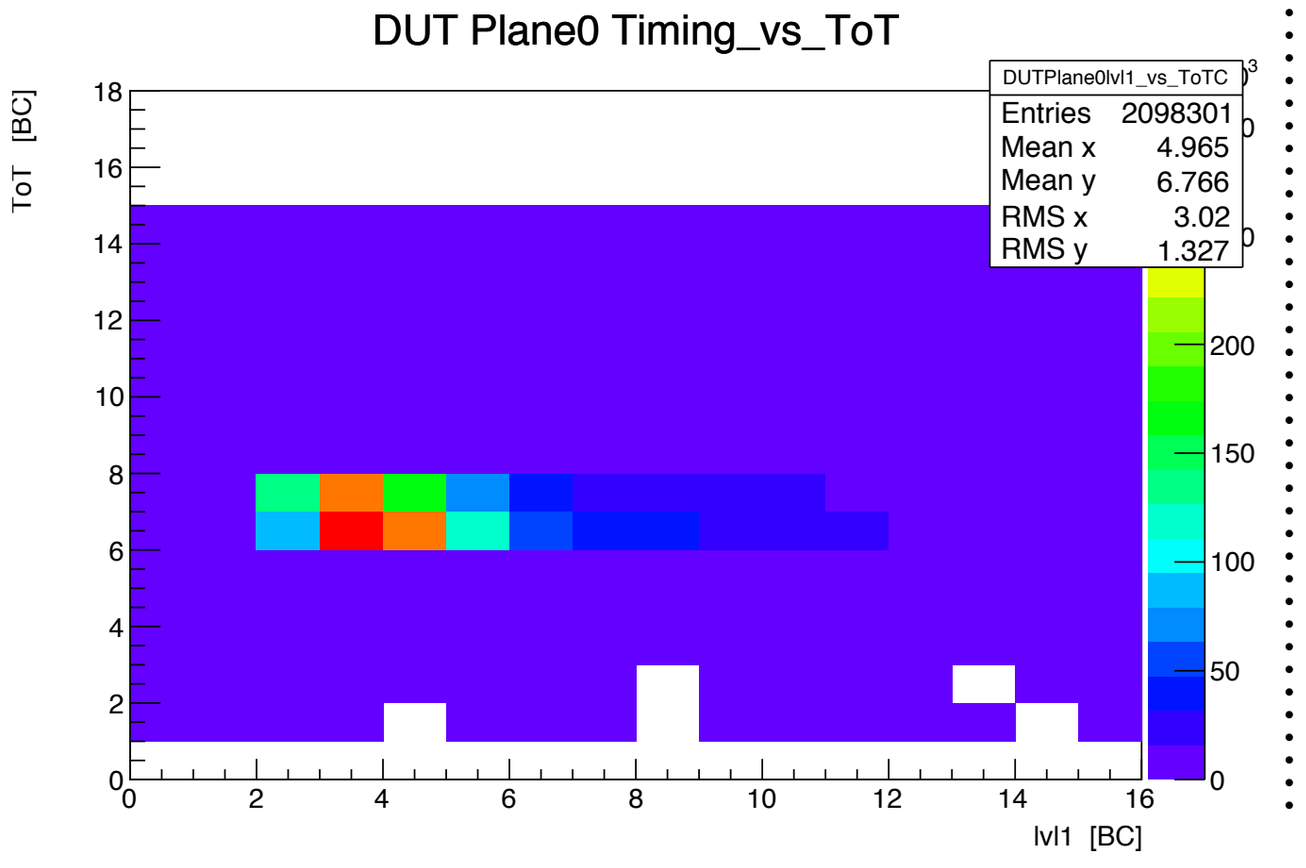
v4 structure

- Several HVCMOS pixels flavours

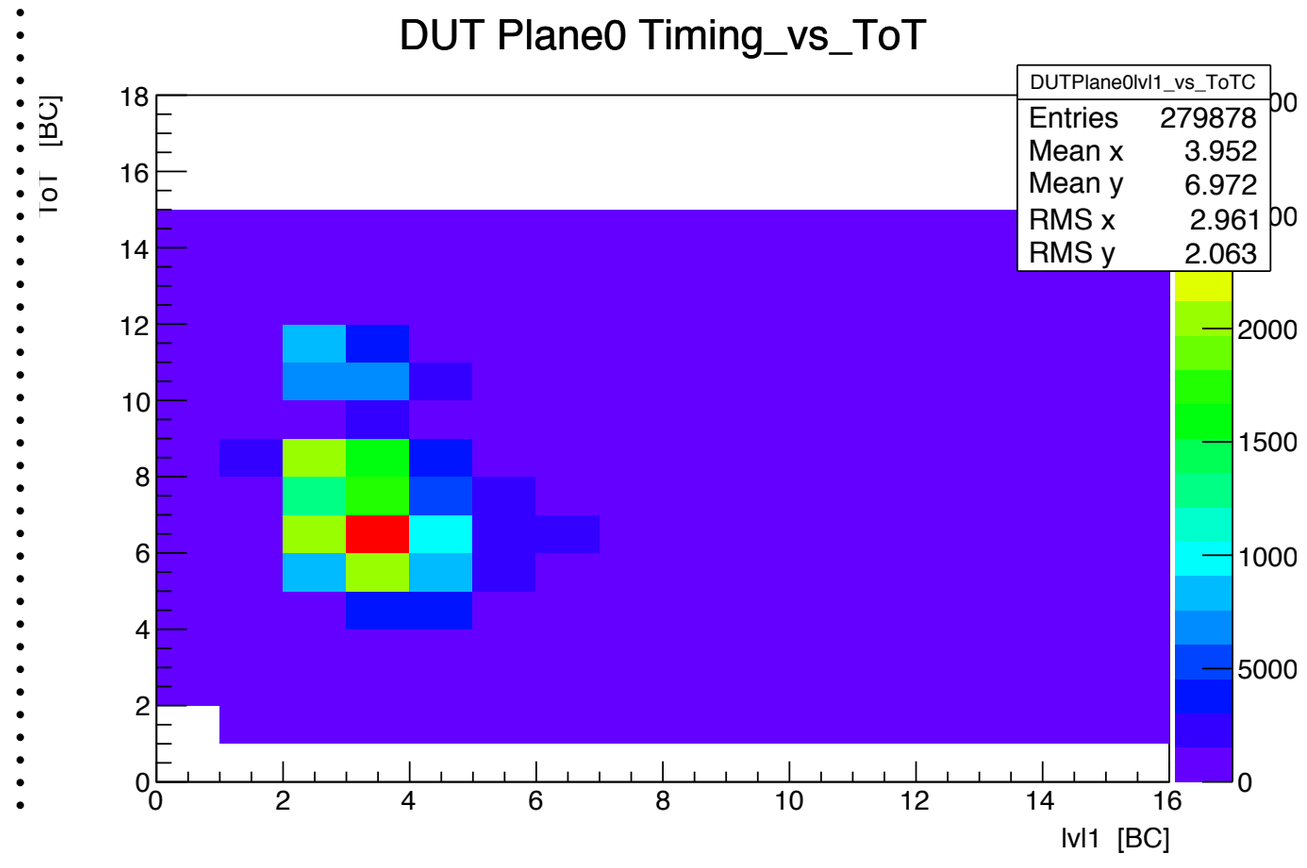


v4 ToT vs Lv1

402, unIrradiated
Bias 12 V, Th 0.84 V
Run: 3911 - 3915

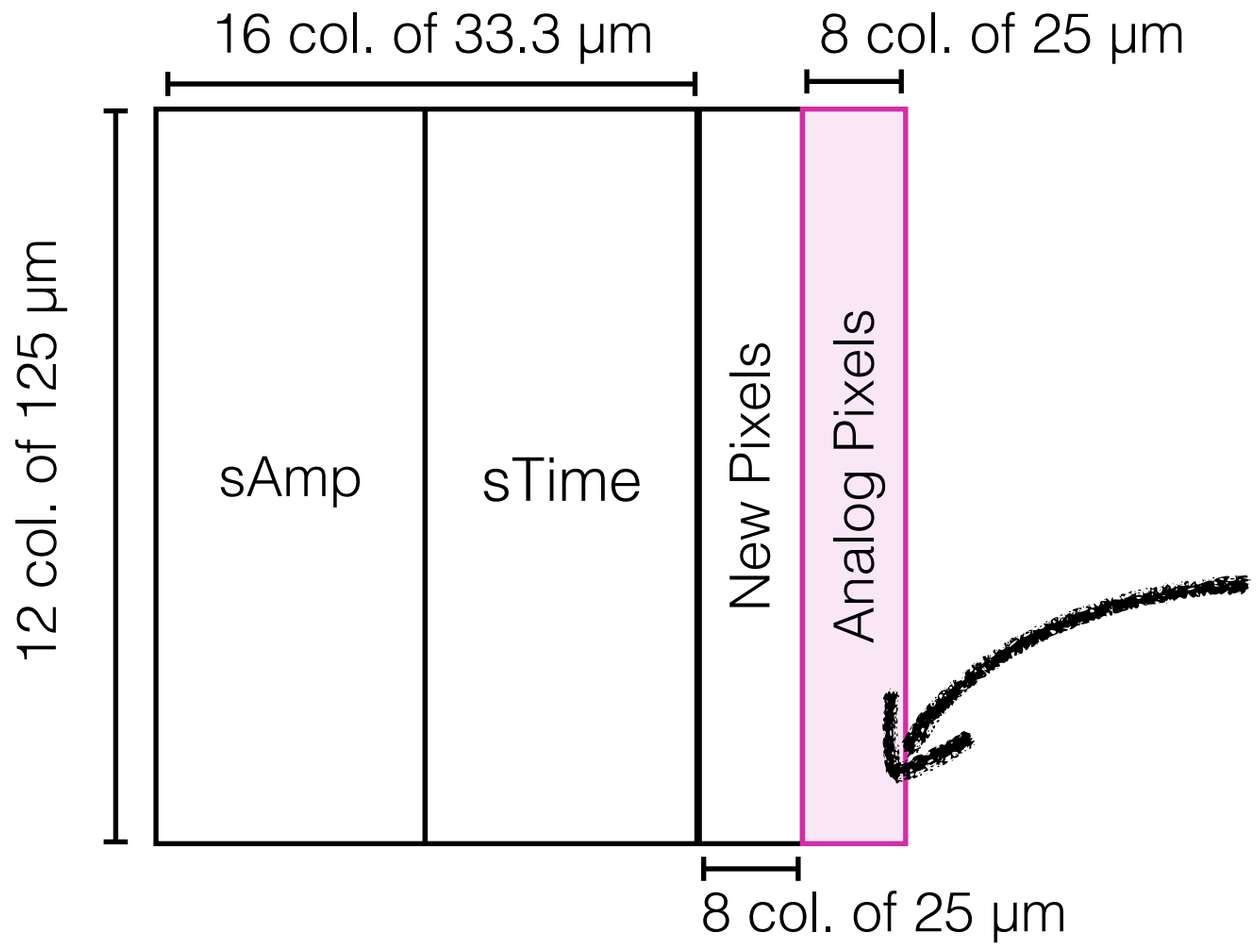


404, 10^{15} n_{eq}/cm^2
Bias 30 V, Th 0.84V
Run: 4074



v4 structure

- Several HVCMOS pixels flavours



Output amplitude
dependent on input signal

Analog pixel - ToT vs Lv1

402, unIrradiated
Bias 12 V, Th 0.84 V
Run: 3966 - 3967