Capacitively Coupled Hybrid Pixel Assemblies for the CLIC Vertex Detector

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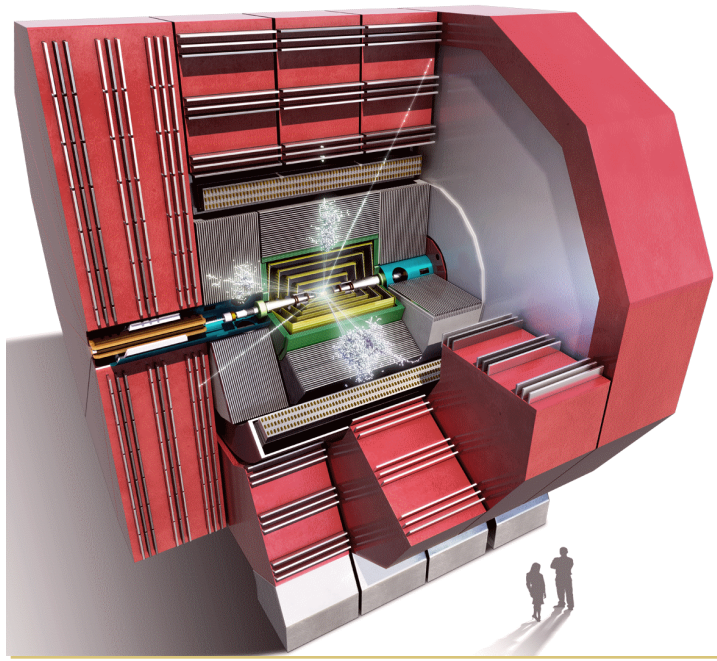
(on behalf of the CLICdp Collaboration)

The CLIC vertex detector

- CLICdp collaboration developing detector design for the proposed Compact LInear Collider at CERN
  - Software description, simulation, physics benchmarks, hardware R&D

- Beam timing structure, beam-induced background and precision required for physics drive the requirements
  - 312-bunch train lasting 156 ns, 0.5 ns between bunches, repeated at 50 Hz
  - Beam-beam interactions produce many background particles, such as $\gamma\gamma \Rightarrow hh$



- For the vertex detector, the requirements are
  - Low material - a budget of 0.2 % X_0 per layer (200 µm of silicon total)
  - Low power consumption - no active cooling (forced air flow, power pulsing)
  - Fast signal generation and timestamping (10 ns)
  - High spatial precision - 3 µm single hit resolution (for Impact Parameter resolution 5 + 15/p µm)

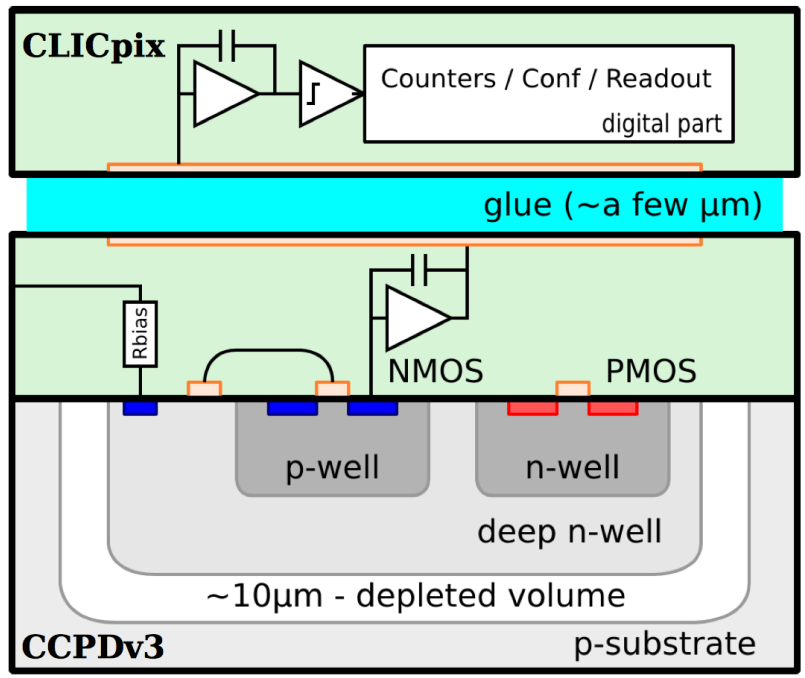
Capacitively coupled hybrid pixel detectors

- Baseline technology for CLIC vertex detector assumed to by hybrid pixel detectors. Requirements lead to a small pitch design with 50 µm sensor on 50 µm thinned ASIC. R&D has been diverse:
  - Bump-bonding tests with existing ASICs and thin sensors (currently achieved 100 µm on 100 µm)
  - Prototype ASIC with small (25 µm) pitch has been fabricated in 65 nm technology, featuring power-pulsing and the required timing granularity

- Emerging technology in particle physics: high voltage/high resistivity CMOS
  - Aim to replace passive diode sensors with "smart" sensors containing signal amplification
  - Use capacitive coupling instead of bump bonding

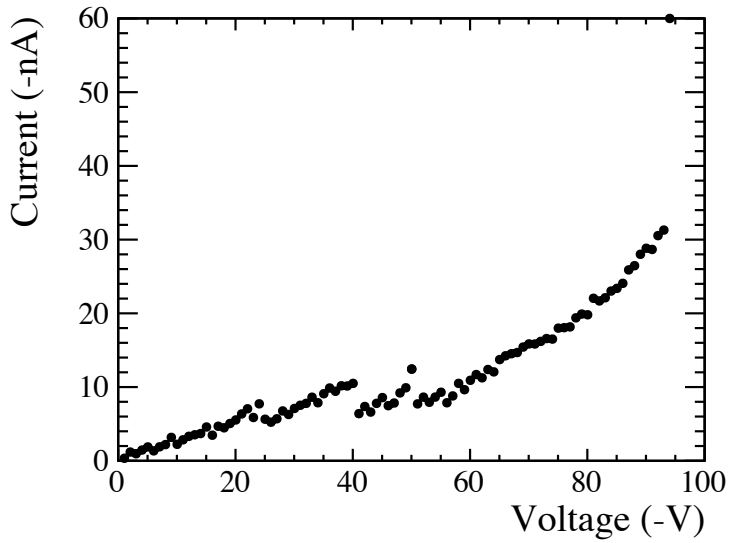
- Industry-standard process
  - Use deep n-well to shield electronics and allow application of a (mild) bias voltage to the substrate => fast drift signal from depleted region

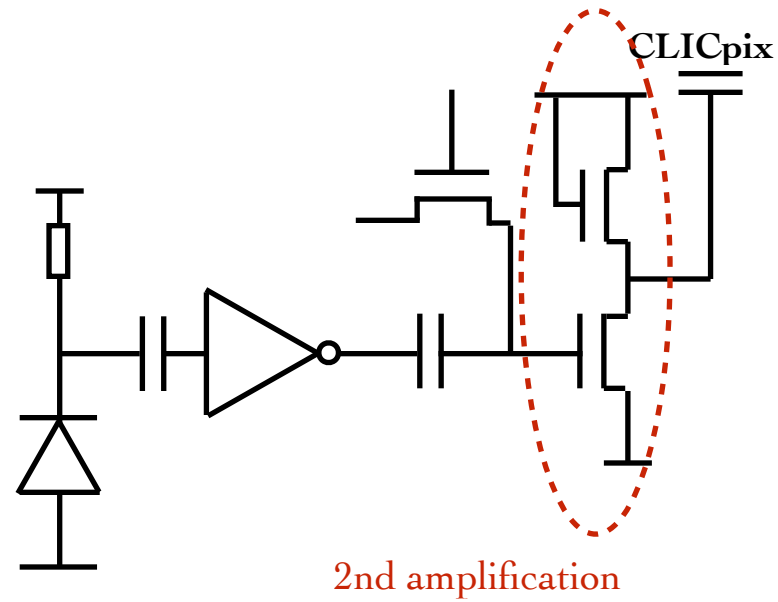
- Prototype assemblies under investigation for CLIC



HV-CMOS, the CCPDv3 chip

- CCPD (Capacitively Coupled Pixel Detector) version 3 designed by I. Perić
  - Fabrication in 180 nm AMS technology (deep n-well shielding, ~60 V rated, ~90 V tolerant)
  - 25 µm square pixels, 64 × 64 matrix designed to fit the CLICpix prototype readout ASIC
  - 4 columns contain a single amplification stage (positive signal), while 60 columns contain two-stage amplification (negative signal)
  - Relatively simple pixel architecture, limited standalone readout capabilities (analogue output possible from ~few pixels for debugging)

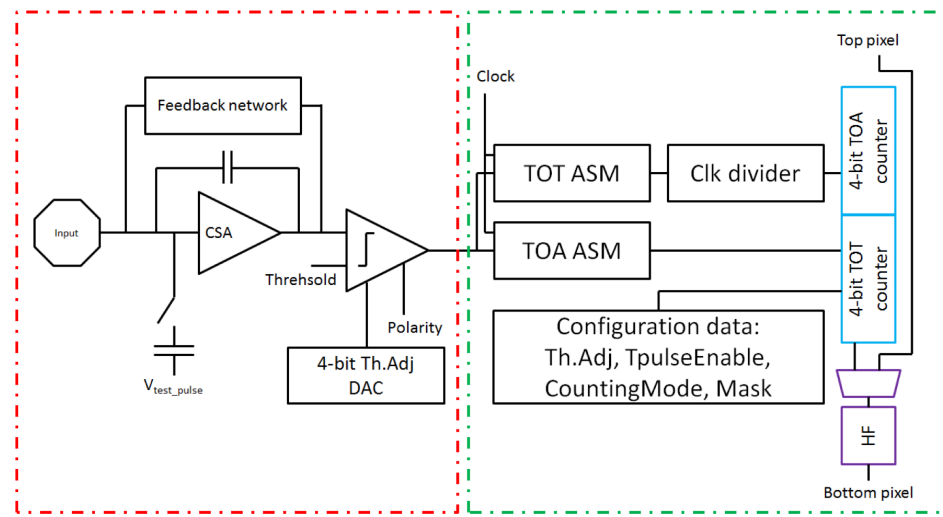




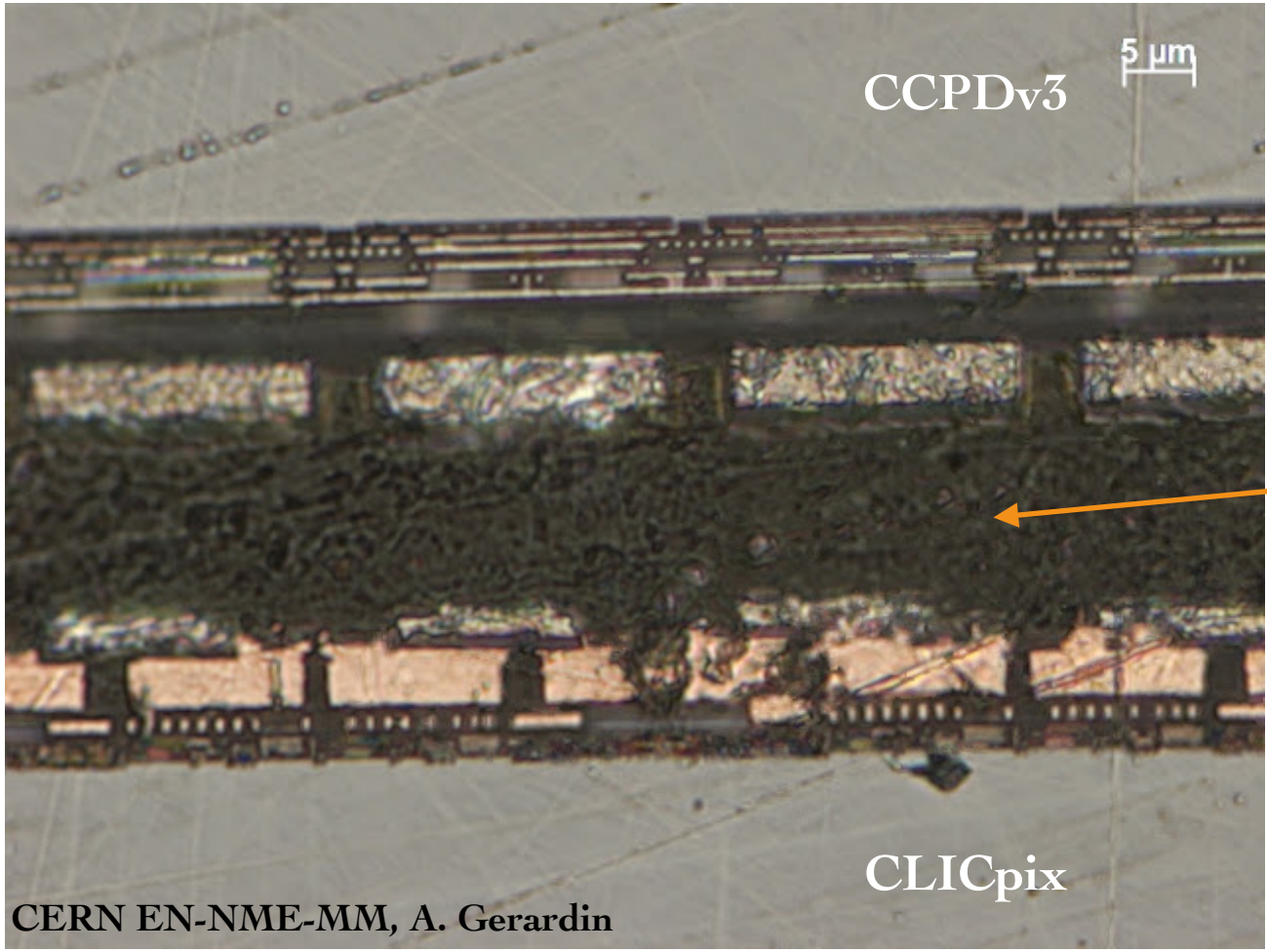
CLICpix

- CLICpix is the prototype readout ASIC designed to fit CLIC vertex detector specifications
  - Manufactured in 65 nm CMOS with small pixel size (25 µm × 25 µm) and containing a matrix of 64 × 64 pixels
  - Two 4-bit counters on each pixel for simultaneous ToT and ToA (or ToT and counting…)
  - Shutter-based data acquisition but with optional on-chip data compression
  - Power pulsing of the pixel matrix

- Known issues:
  - Small overlap of discriminator signal line with CSA input pad => negative pulse injected into the front end when the discriminator starts firing
  - Will add signal to negative pulses, subtract signal for positive pulses
  - Important effect when interpreting the results later…

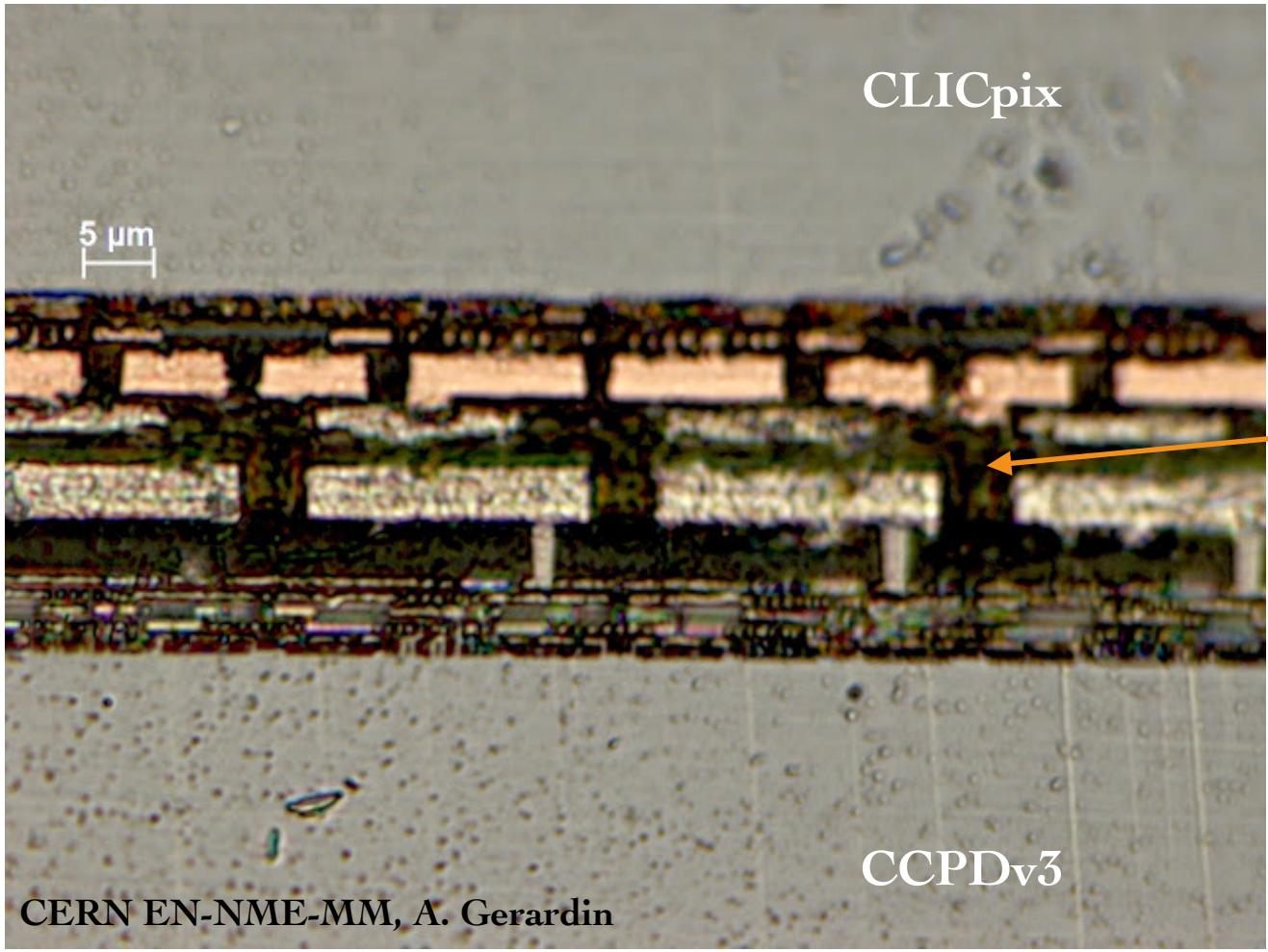


Assembly

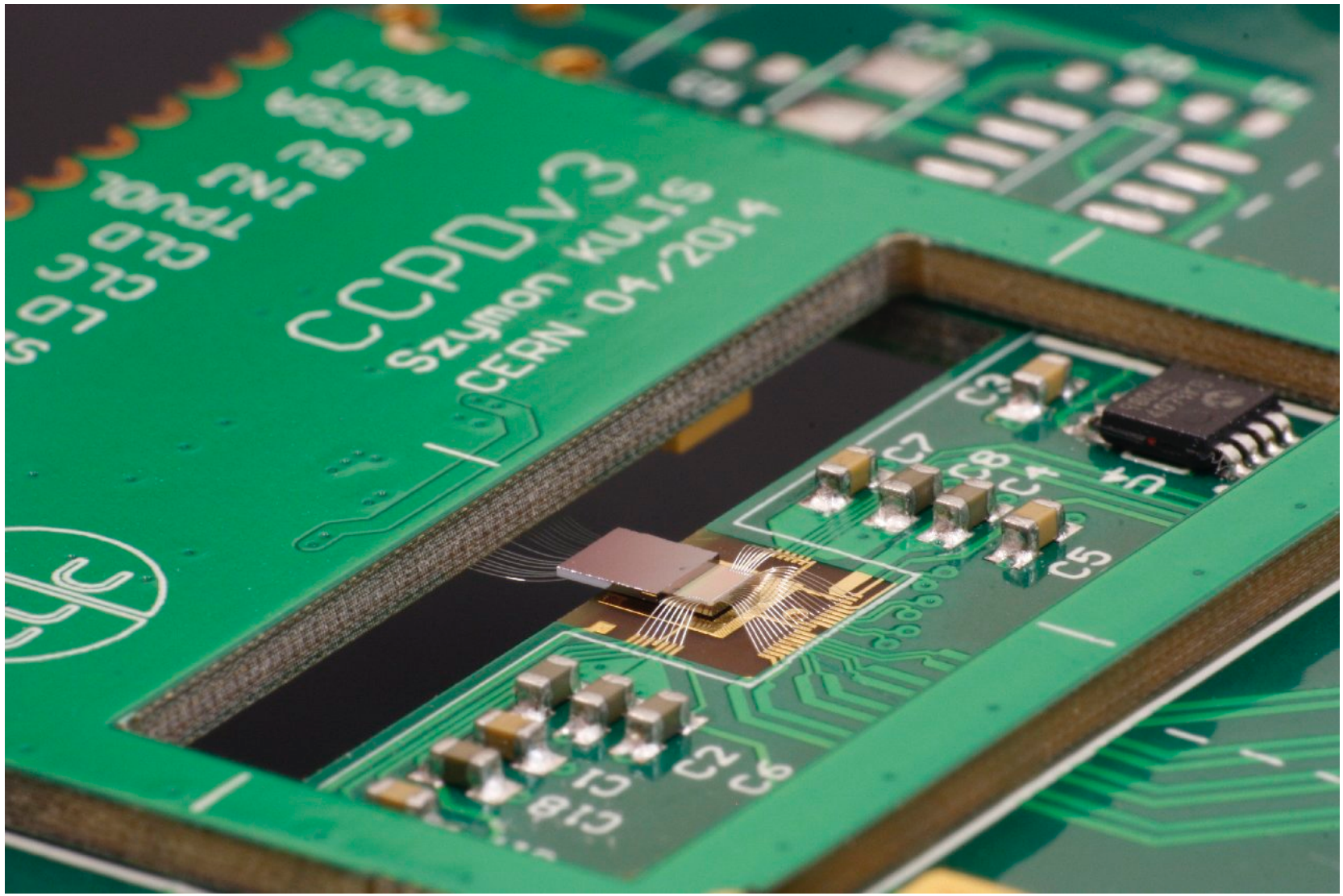


Epoxy glue

Assembly

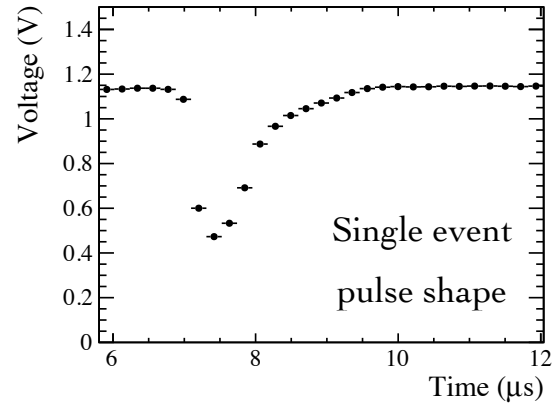


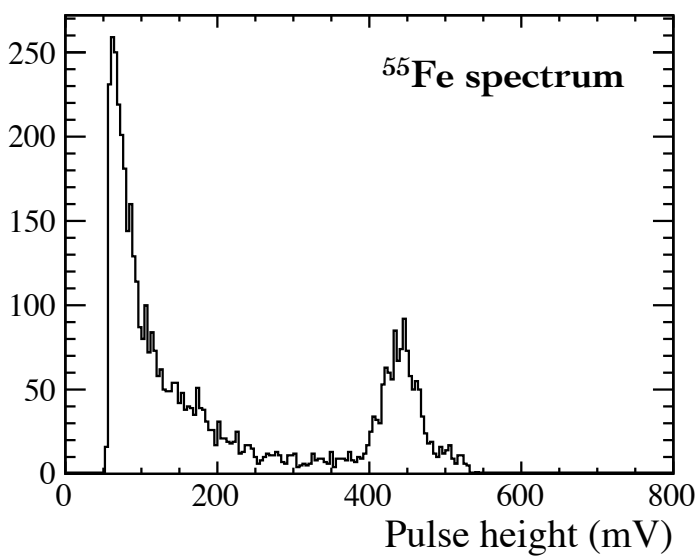
Lab measurements

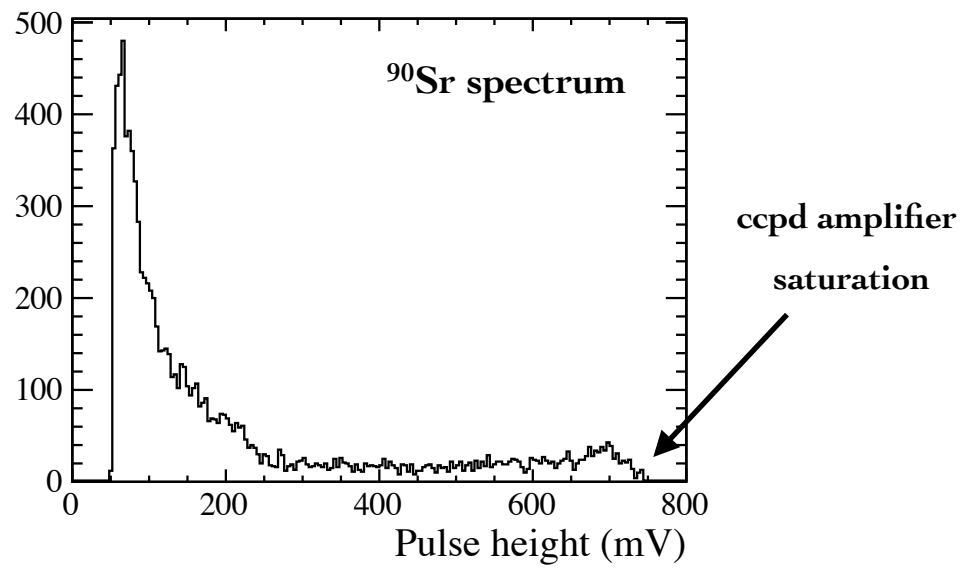


Charge spectra with HV-CMOS

- Lab tests performed on the HV-CMOS using single pixel analogue output to investigate signal shape and charge spectra with sources
  - Front-impinging ^{55}Fe on bare HV-CMOS assembly (~6 keV)
  - Back-impinging ^{90}Sr on full HV-CMOS + CLICpix assembly
  - (results shown for 2-stage amplifier design)



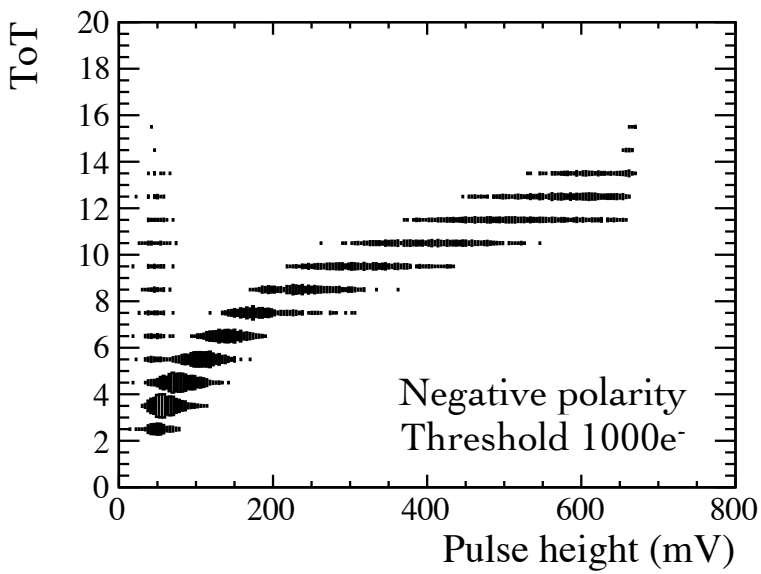


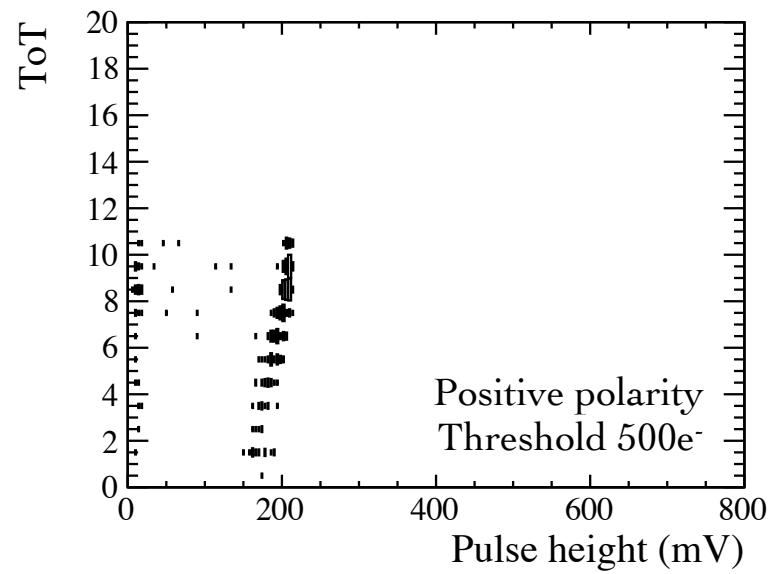


Induced signal in CLICpix

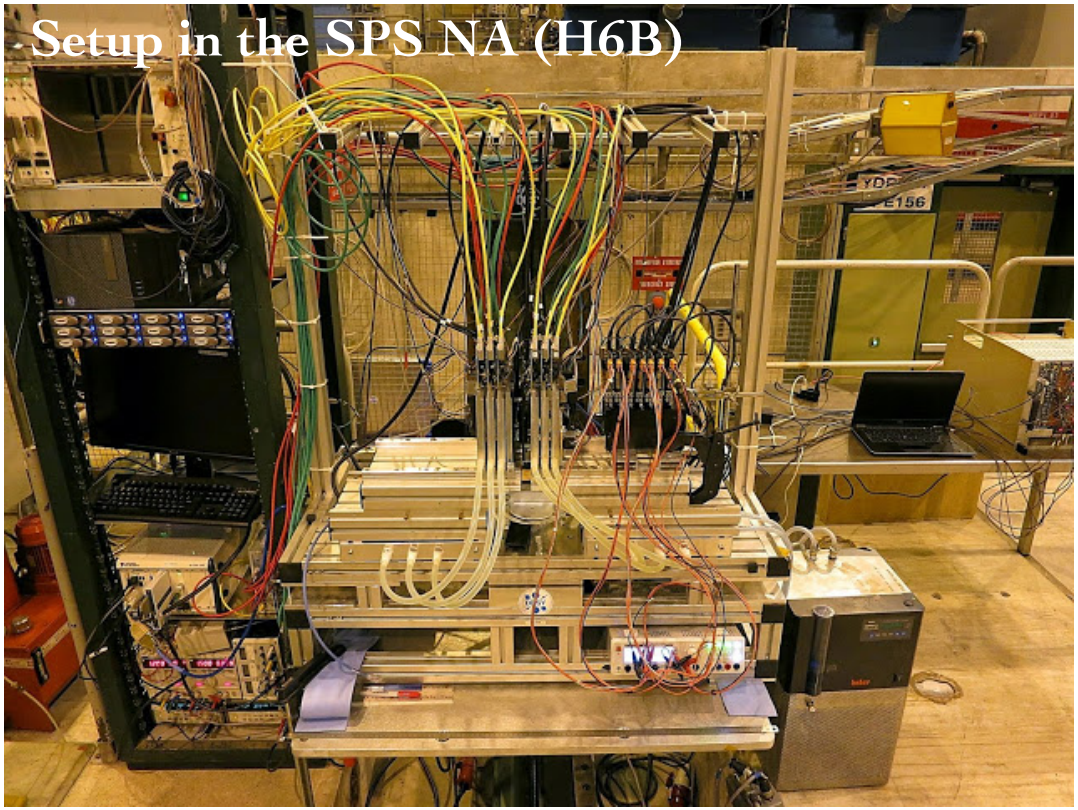
- Analogue output from several pixels on the HV-CMOS device can be monitored individually
  - Can take data in parallel with the CLICpix, correlate the pulse shape with the ToT
  - Open shutter, wait for signal on scope, close shutter and read out before subsequent hits

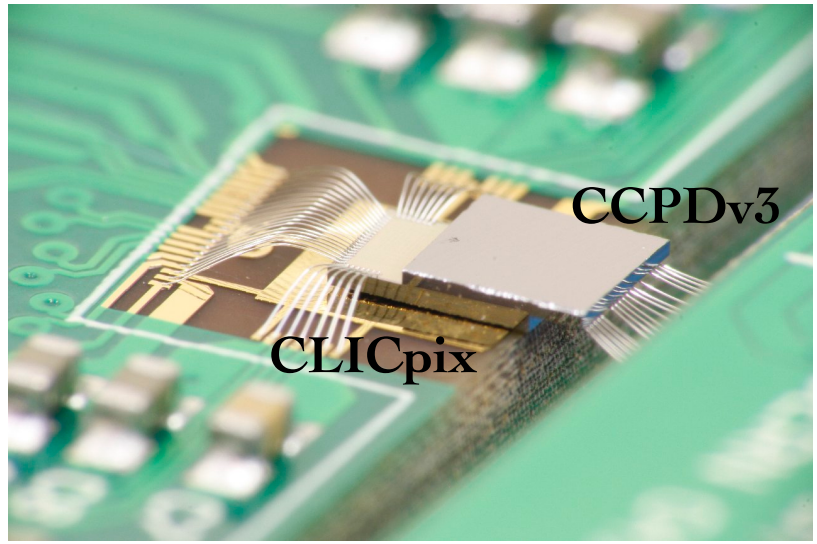
- Can see the difference between polarities
  - Injected negative charge gives a lower effective threshold when operating with negative polarity, higher effective threshold when operating with positive
  - Using nominal values of threshold this gives roughly 625 e^- injected charge

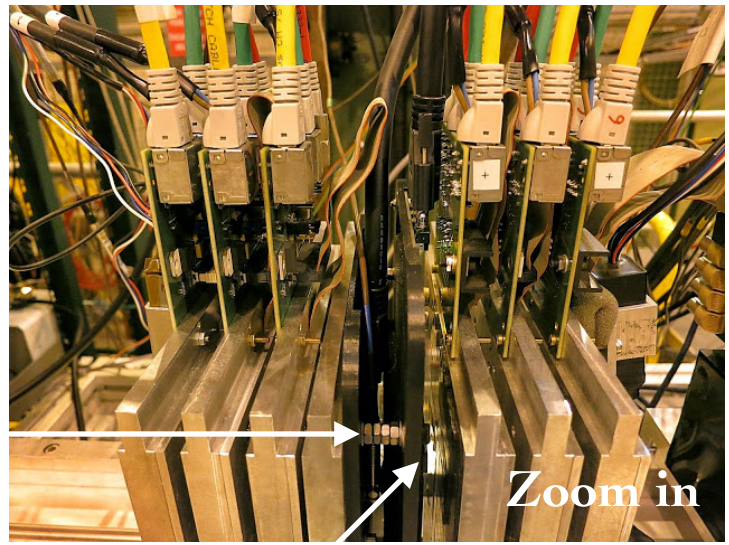




Beam data


Setup in the SPS NA (H6B)


CCPDv3
CLICpix

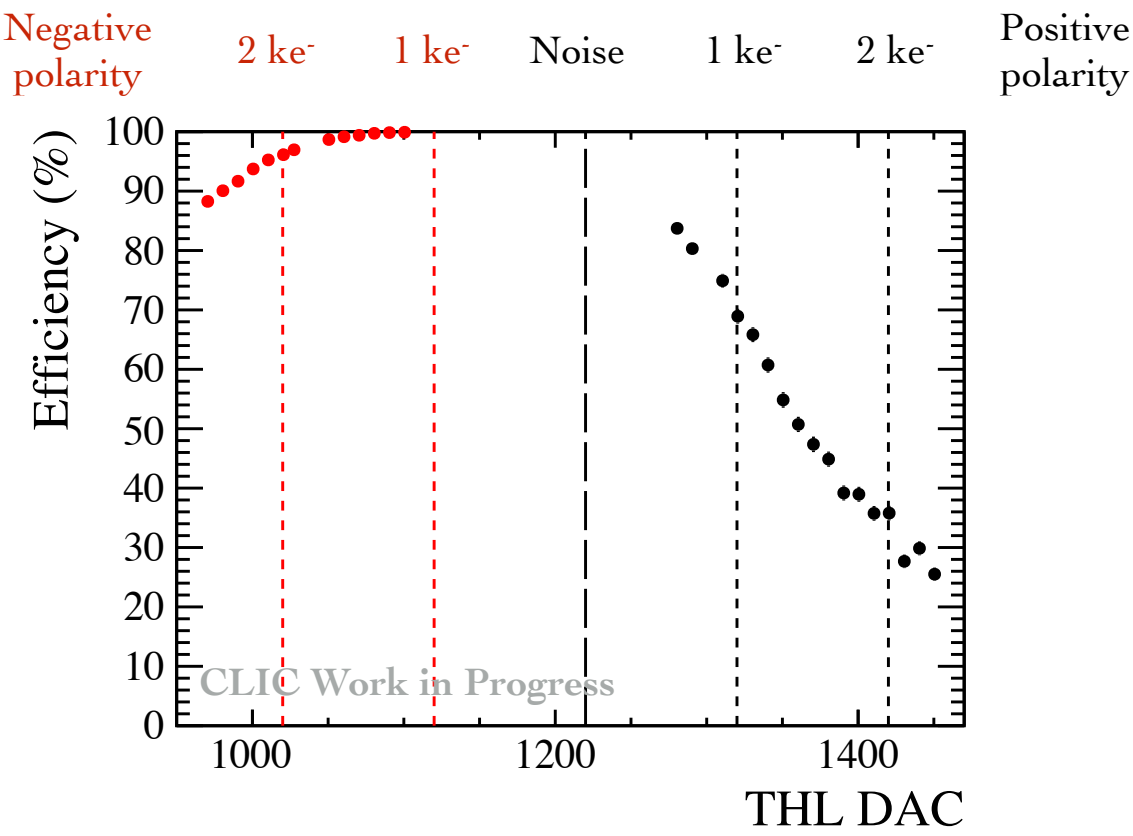

Timepix3
Zoom in
CLICpix

Threshold scan

- Data taken at the SPS North Area in November 2015, using the AIDA/EUDet telescope to provide tracking

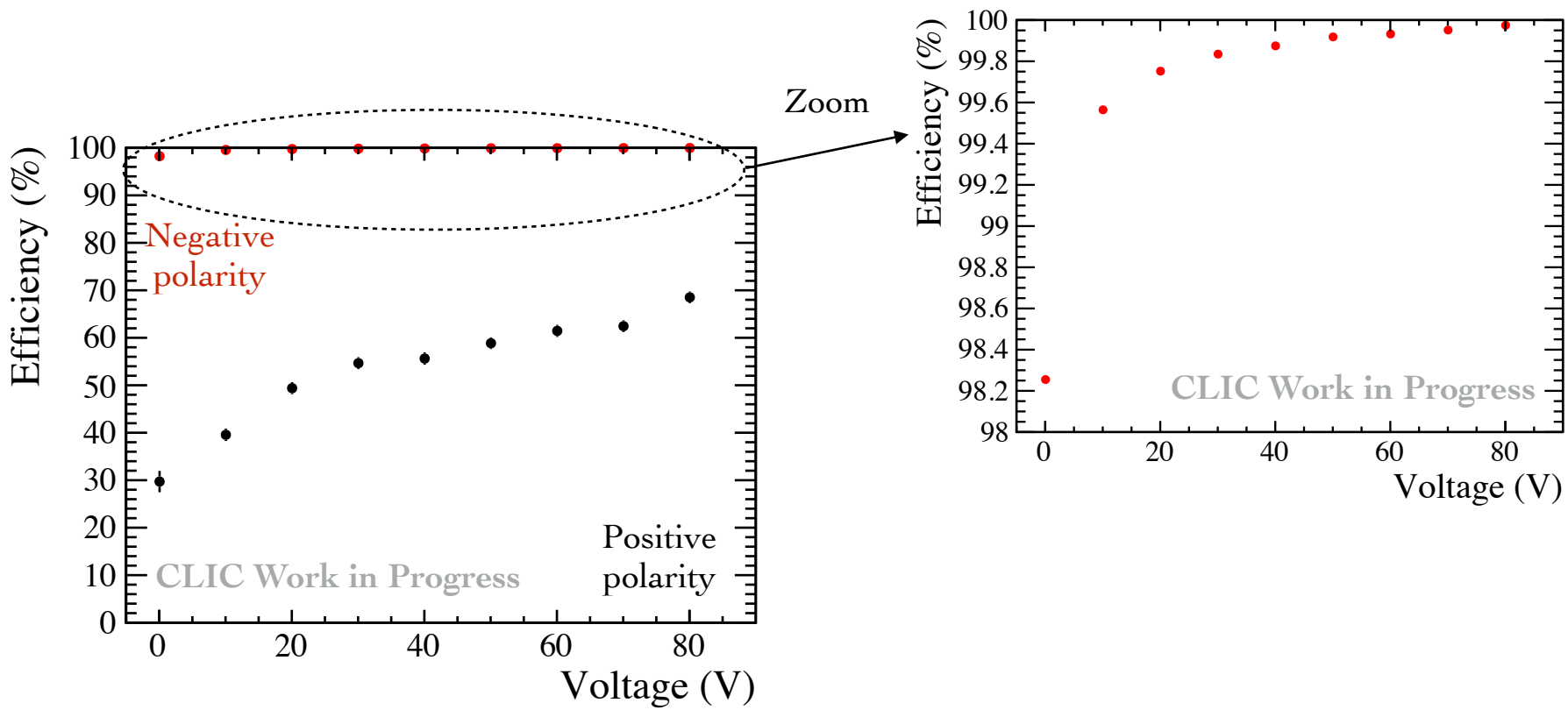
- Efficiency versus threshold for both polarities measured (60 V)
  - Pointing resolution from the telescope estimated < 2 µm

- Clear difference in performance
  - Able to reach high efficiency, 99.97 %, in negative polarity mode (2-stage amplification) with threshold ~ 1100 e^-
  - Single amplification stage pixels suffer from lower signal **and** subtraction of charge, but given fall off in 2-stage pixels it seems likely that with a new chip 500 e^- threshold will require 2nd stage



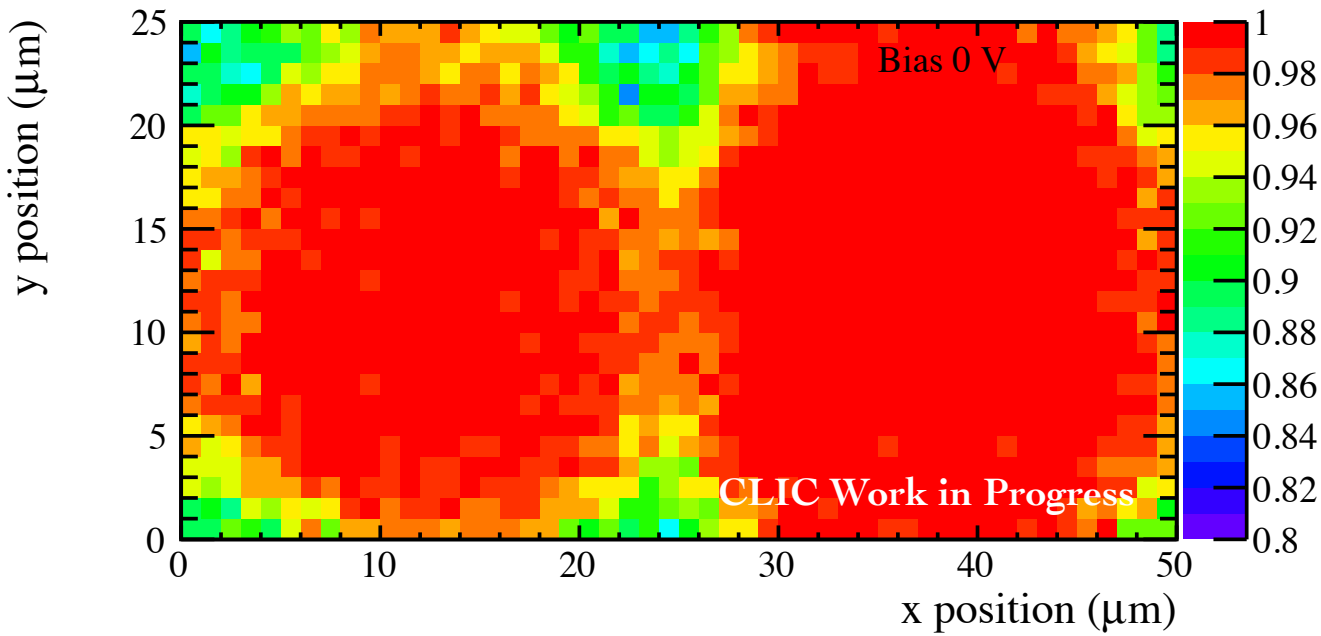
Bias scan

- High efficiency observed in negative polarity mode without bias on the HV-CMOS
  - Large component of collected charge from diffusion? Or large built-in depletion layer?
  - Estimates for depleted region vary, but typically ~10 µm at 60 V



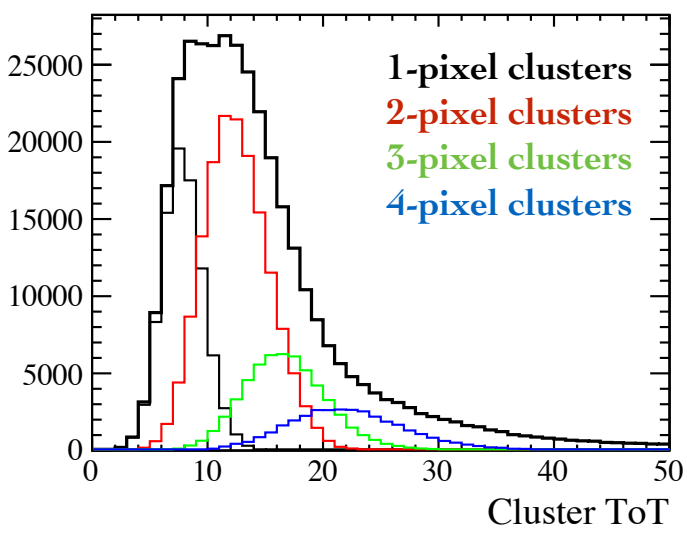
Bias scan - negative polarity

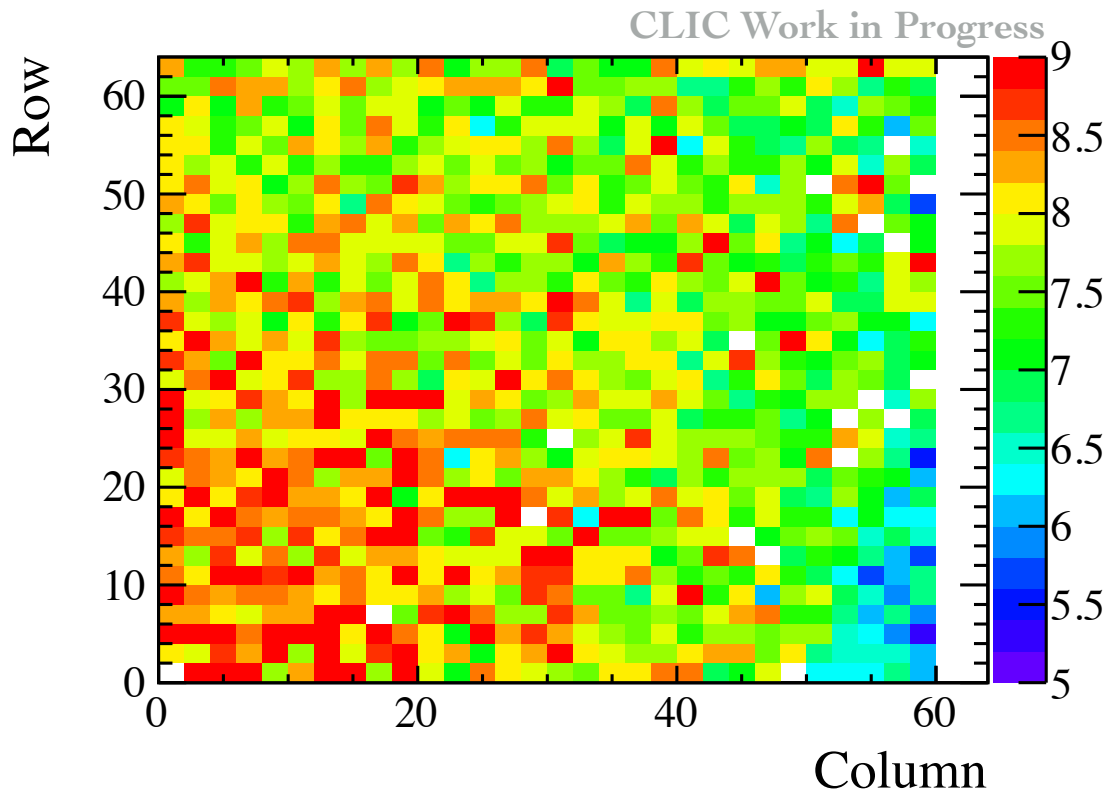
- Can map the variation in efficiency across the 2-pixel unit (charge injection differs between odd and even columns due to layout of signal routing)
  - Efficiency loss in the pixel corners for no applied bias (low threshold)
  - Clear difference between columns - more injected charge (left column) leads to higher observed efficiency



Artefacts of assembly

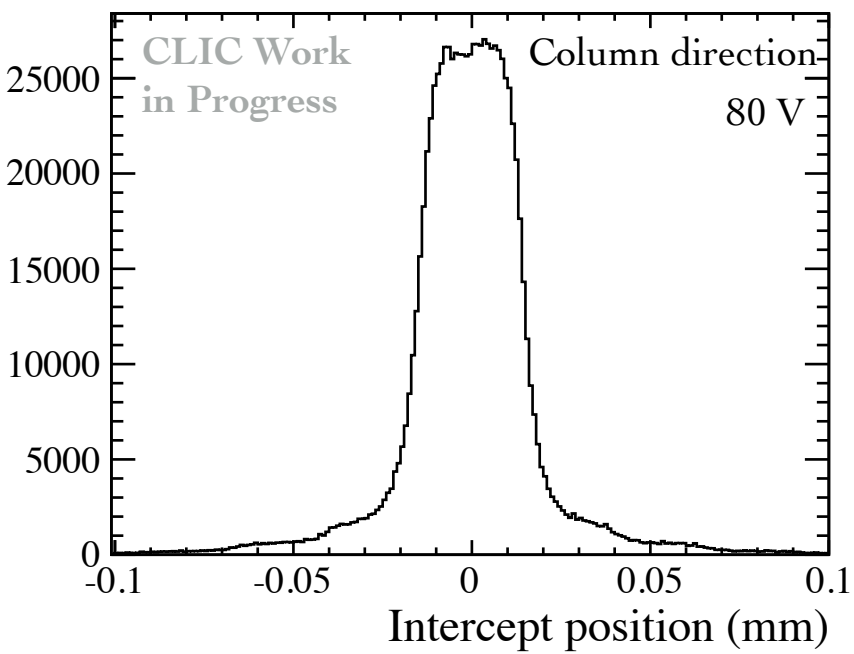
- Considering only single-pixel clusters, can compare the variation in coupling capacitance across the matrix by fitting the charge distribution as a function of track intercept
  - Appearance of a gradient across the assembly => non-uniform glue thickness
  - Smaller defect possibly due to dirt/contamination in the glue layer in one corner

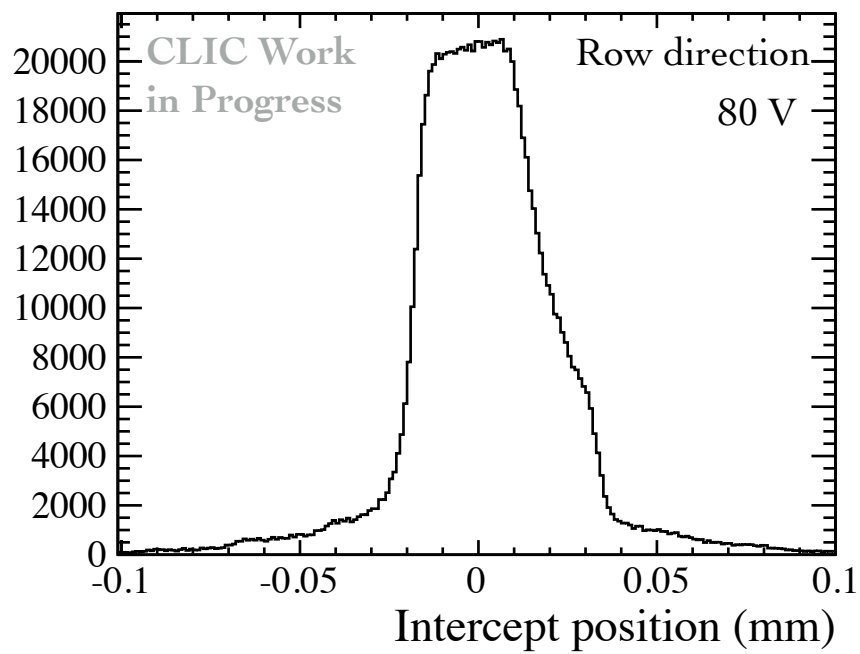




Pixel cross-coupling

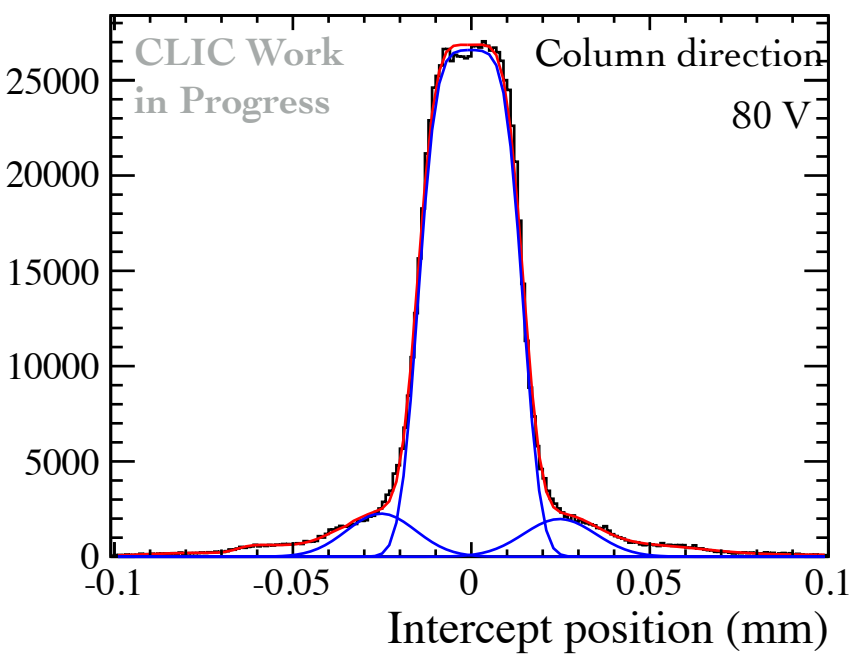
- Signal transfer between CCPDv3 and CLICpix via capacitive coupling - might be sensitive to cross-coupling/misalignment between pixels on the same/different device(s)?
  - Scan the beam across the matrix and observe the behaviour of all pixels
  - Look at when pixel starts responding, and when it stops
  - Ideal function should be top hat function with width described by the lateral charge diffusion

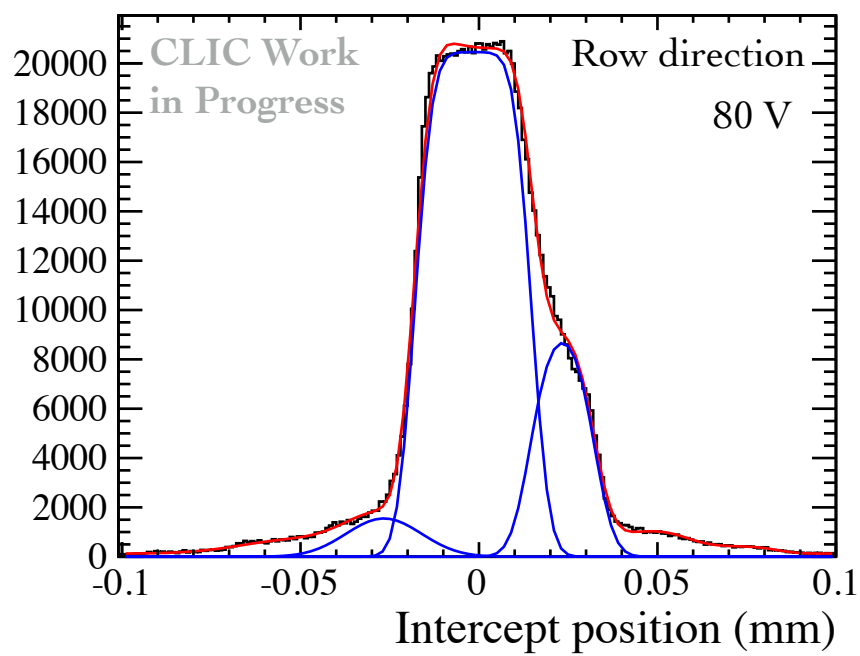




Pixel cross-coupling

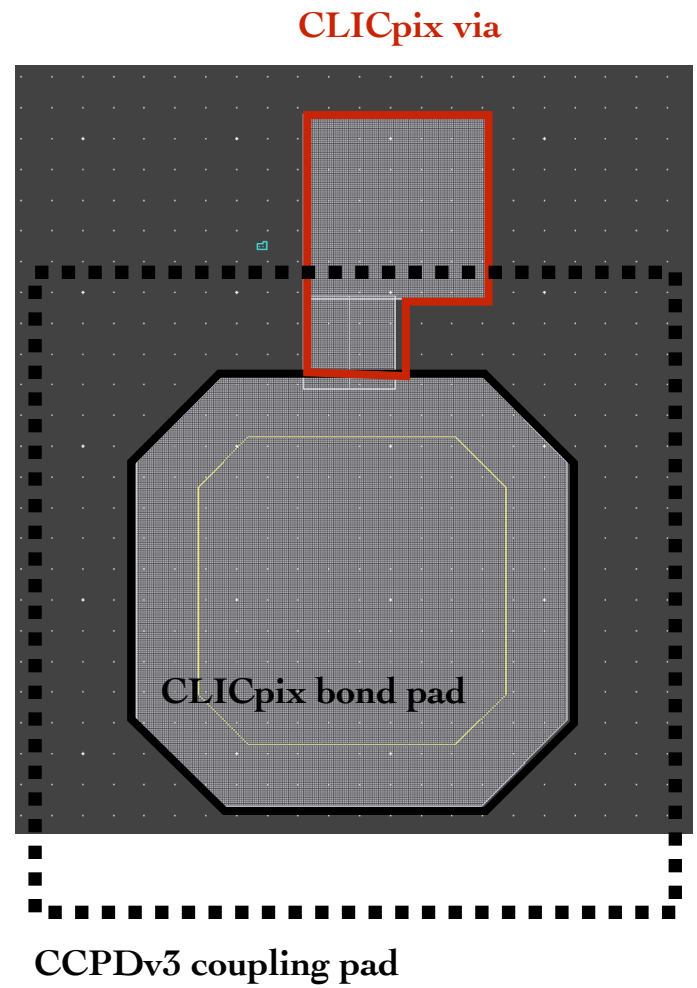
- Different response in row and column directions
  - In each case can fit for the contribution from each pixel - clear signal from coupling to neighbours
  - In the row direction there is a large contribution from the pixel immediately to the right => possible misalignment in the row direction?
  - Glueing studies planned to evaluate precision of the flip-chip machine





Pixel cross-coupling - design issues

- Misalignment appears to be related to signal routing on the CLICpix front-end
  - **Via** used to transfer input signal (from **bonding pad**) to lower metal layers also couples to CCPDv3 pad
  - Large pad (20 µm) on the CCPDv3 aligned with the CLICpix bonding pad - small overlap with neighbouring pads
  - Possible mitigation by optimised glueing - simulations ongoing
- Next generation design needs to take this into account
  - Smaller pad size on the HV-CMOS
  - Different layout of the CLICpix pad (limited space due to 25 µm pitch and foundry design rules)
  - Avoid significant decrease in total coupling capacitance



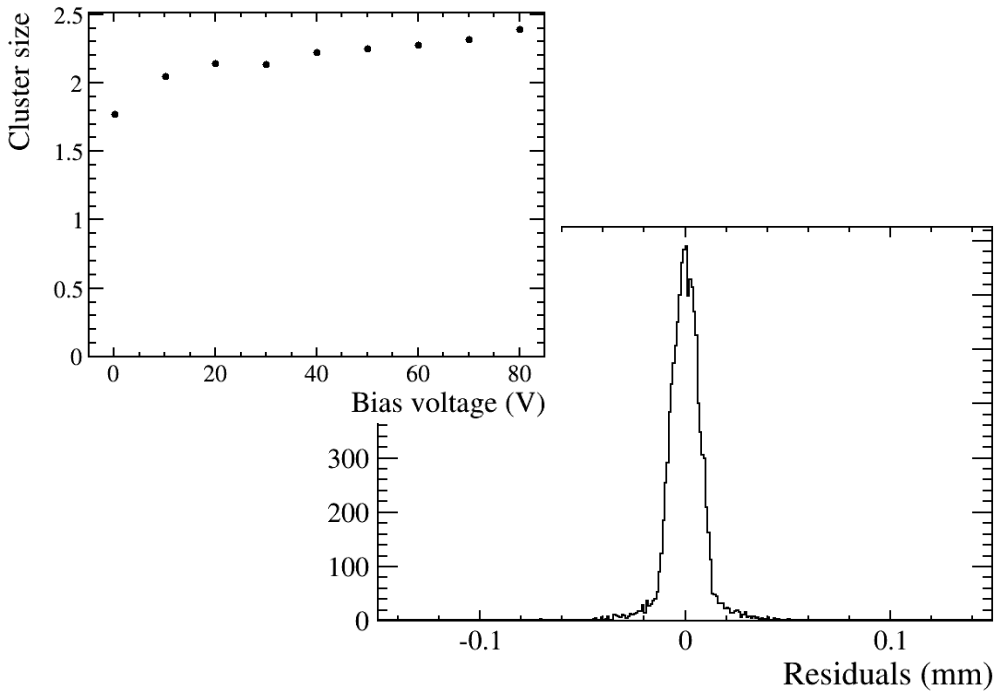
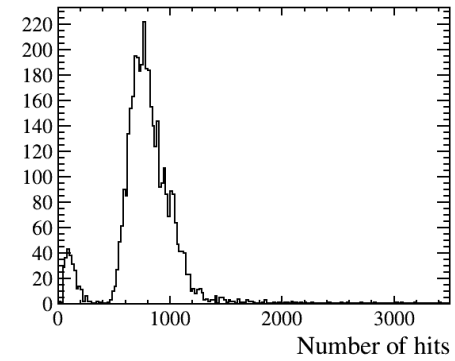
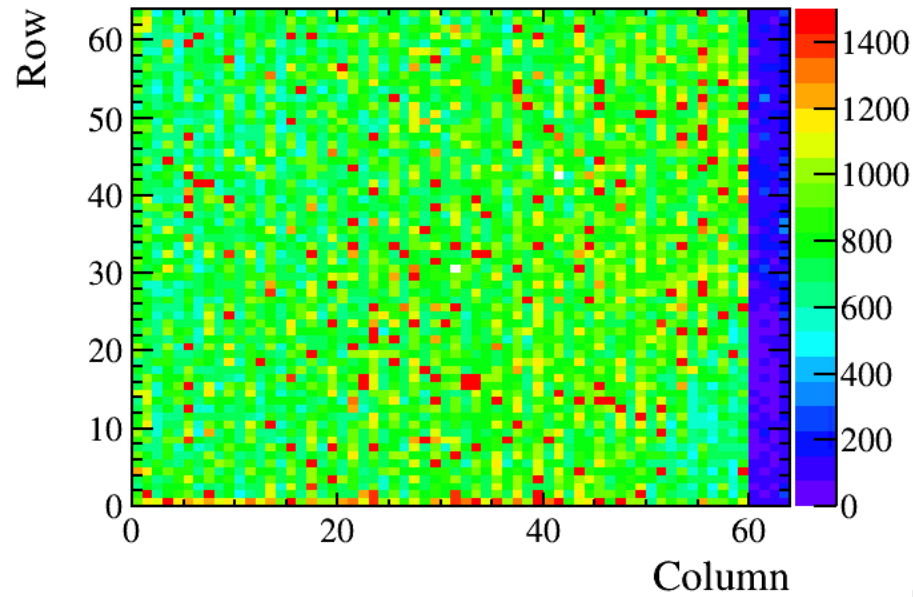
Summary and plans

- Promising early results from capacitively coupled assemblies
  - Simple pixel layout with 2-stage analogue amplification shows high (> 99 %) efficiency
  - High efficiency without applied bias voltage, ~40 V required to reduce inefficiencies between pixels

- Fabrication steps
  - Larger (and injection-free) version of CLICpix under development - submission ~mid 2015
  - New HV-CMOS devices planned
    - Higher resistivity substrate (increased drift region)
    - Faster amplifier
    - Possible digital version(s) in addition to straightforward 2-stage amplifier
    - Submission 2nd half 2015

- Future studies
  - Measurements of coupling capacitance variation (and cross-capacitance) due to gluing
  - Beam measurements to evaluate power-pulsing of the front end and timewalk of the assembly
  - Active depth measurements to determine drift region and contribution of diffusion

BACKUP

Beam data - overview

- Full matrix appears responsive (negative polarity)
  - Small number of hits observed on positive polarity pixels, due to undershoot of the signal pulse
  - Reconstruction performed and residuals good