Resistive anode studies

D. Attié, P. Colas, E. Delagnes, M. Dixit, A. Giganon, M. Riallot, F. Senée, S. Turnbull

Irfu cea saclay

RD51 Paris 2008

LC TPC

Micromegas Large Prototype panels

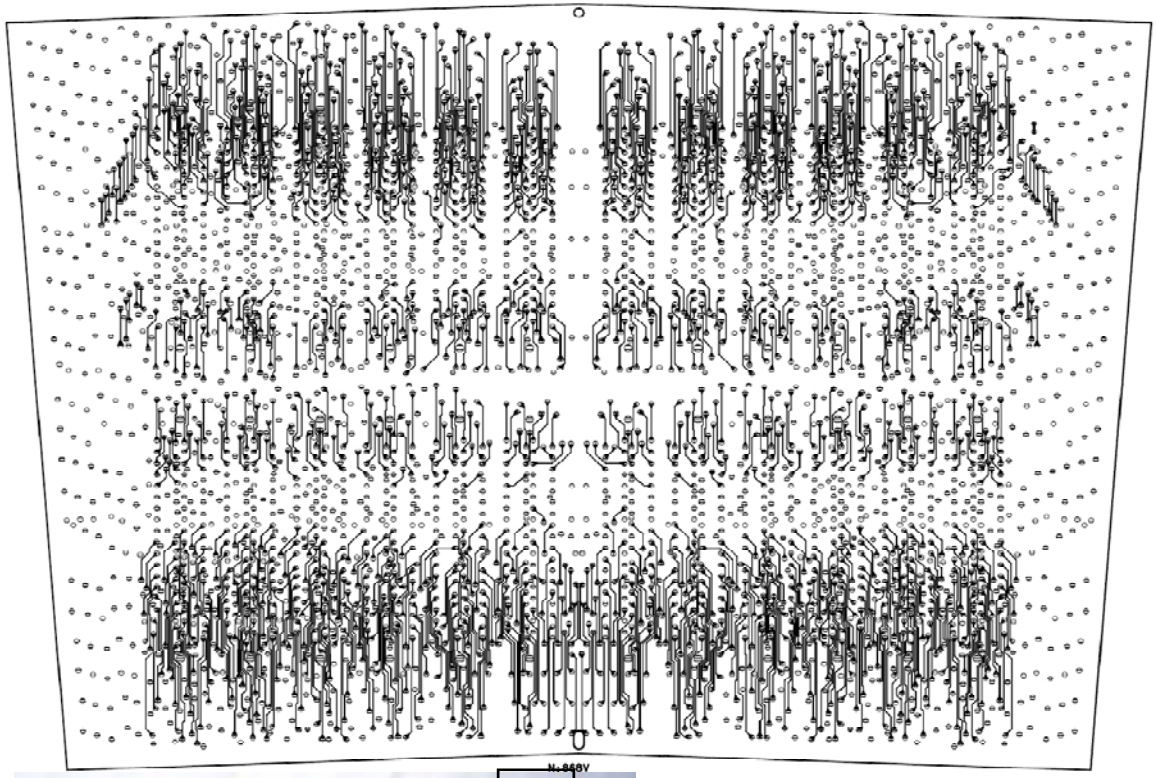
Studies on resistive coatings

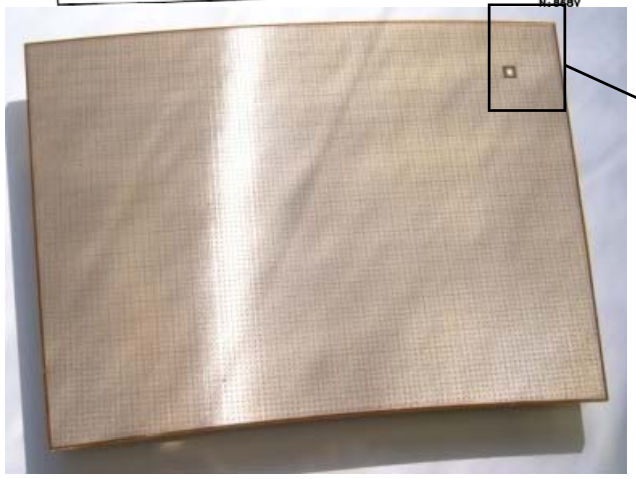
The panels

PCBs have been produced

4 with the Saclay routing in 6 layers (delivered early June)

4 with the CERN routing with 4 layers (August)

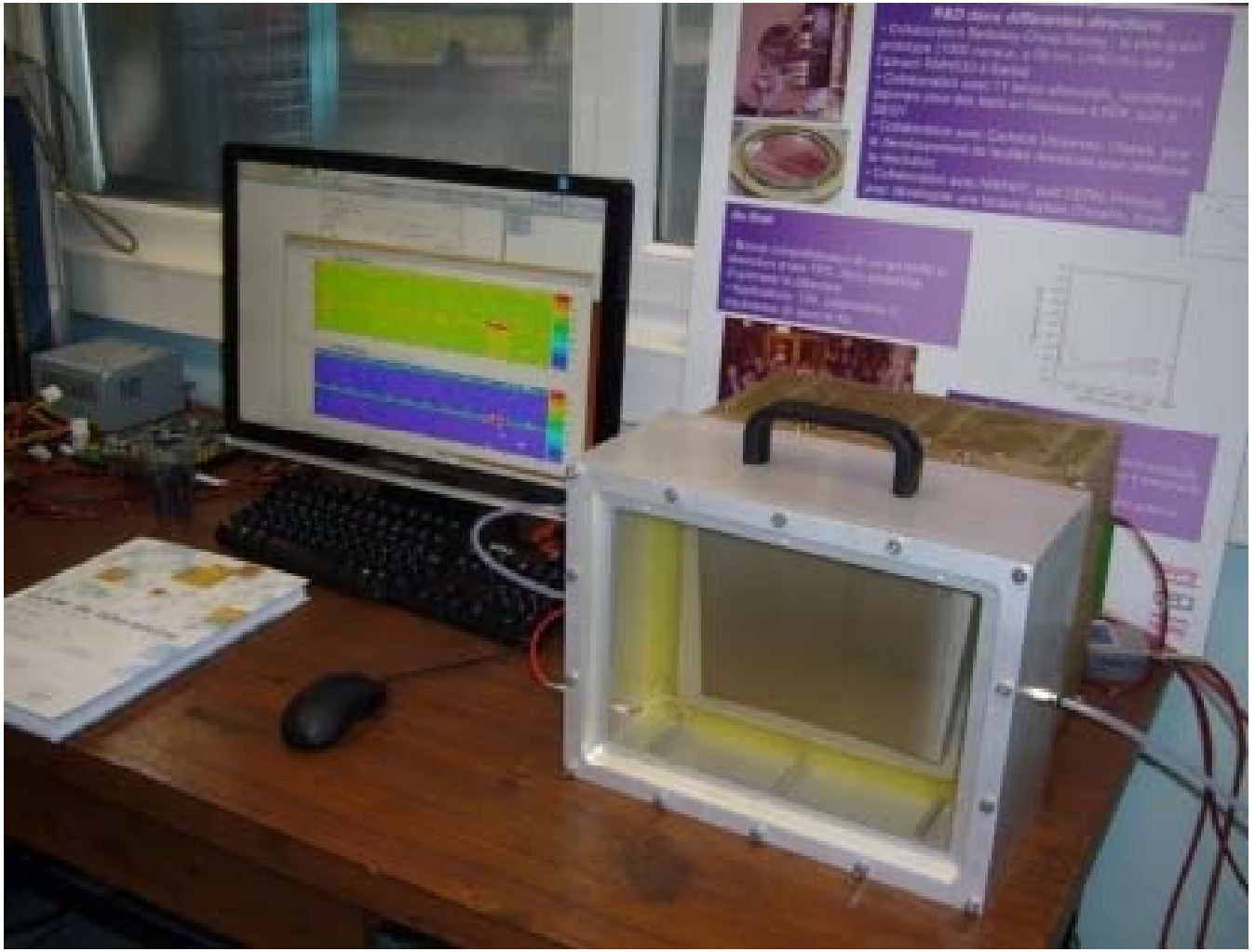


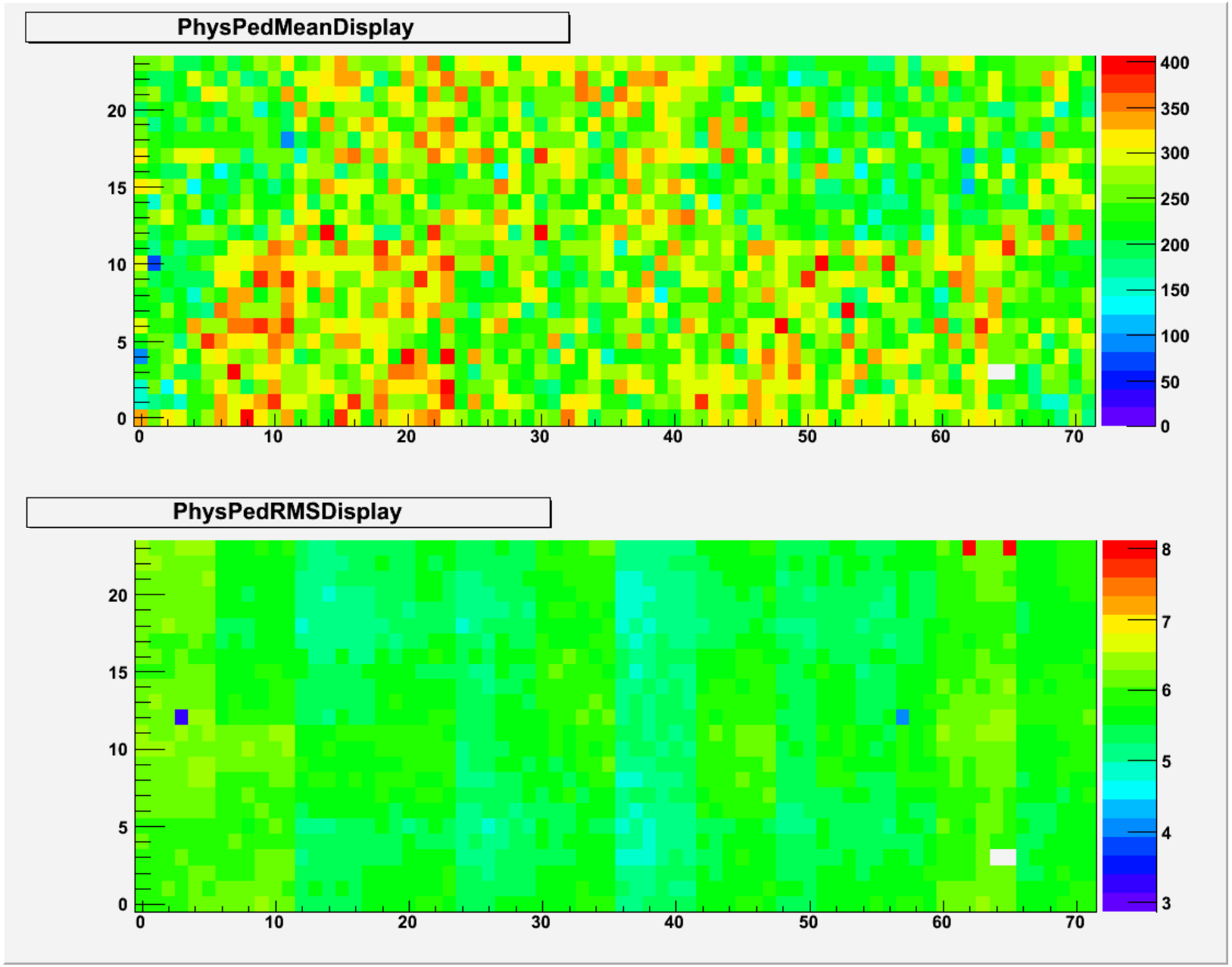


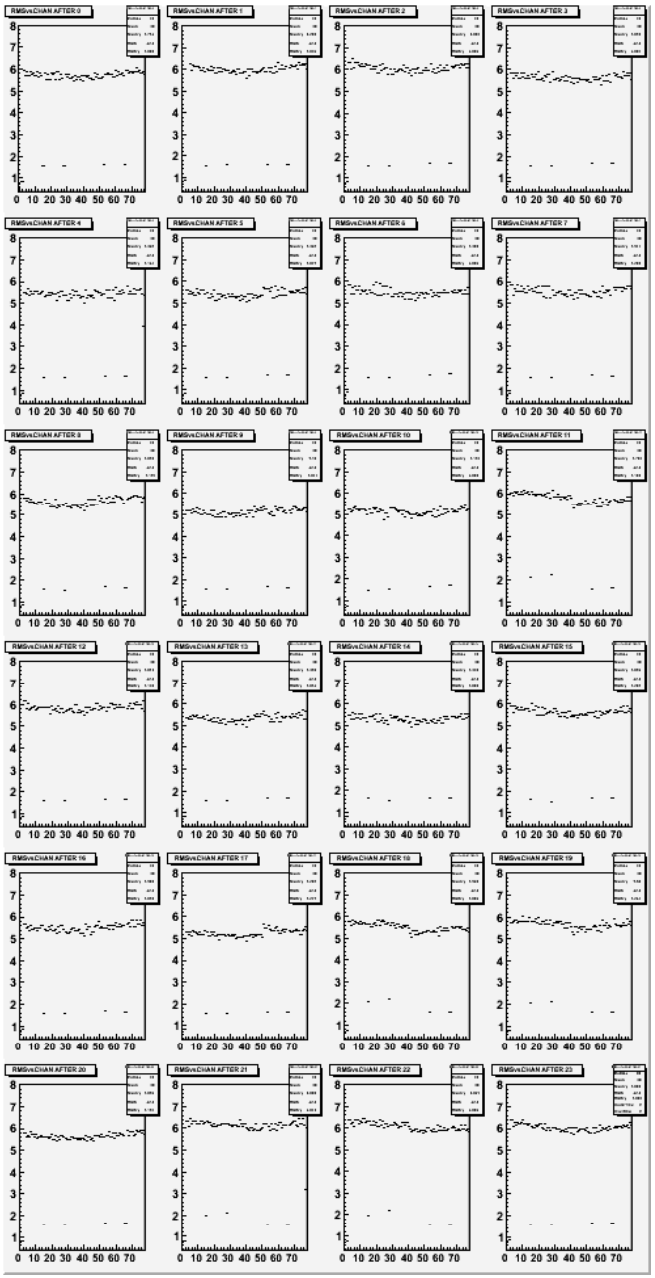
Test setup at Saclay

Tests in gas were performed in our lab

(one faulty pad had to be disconnected)

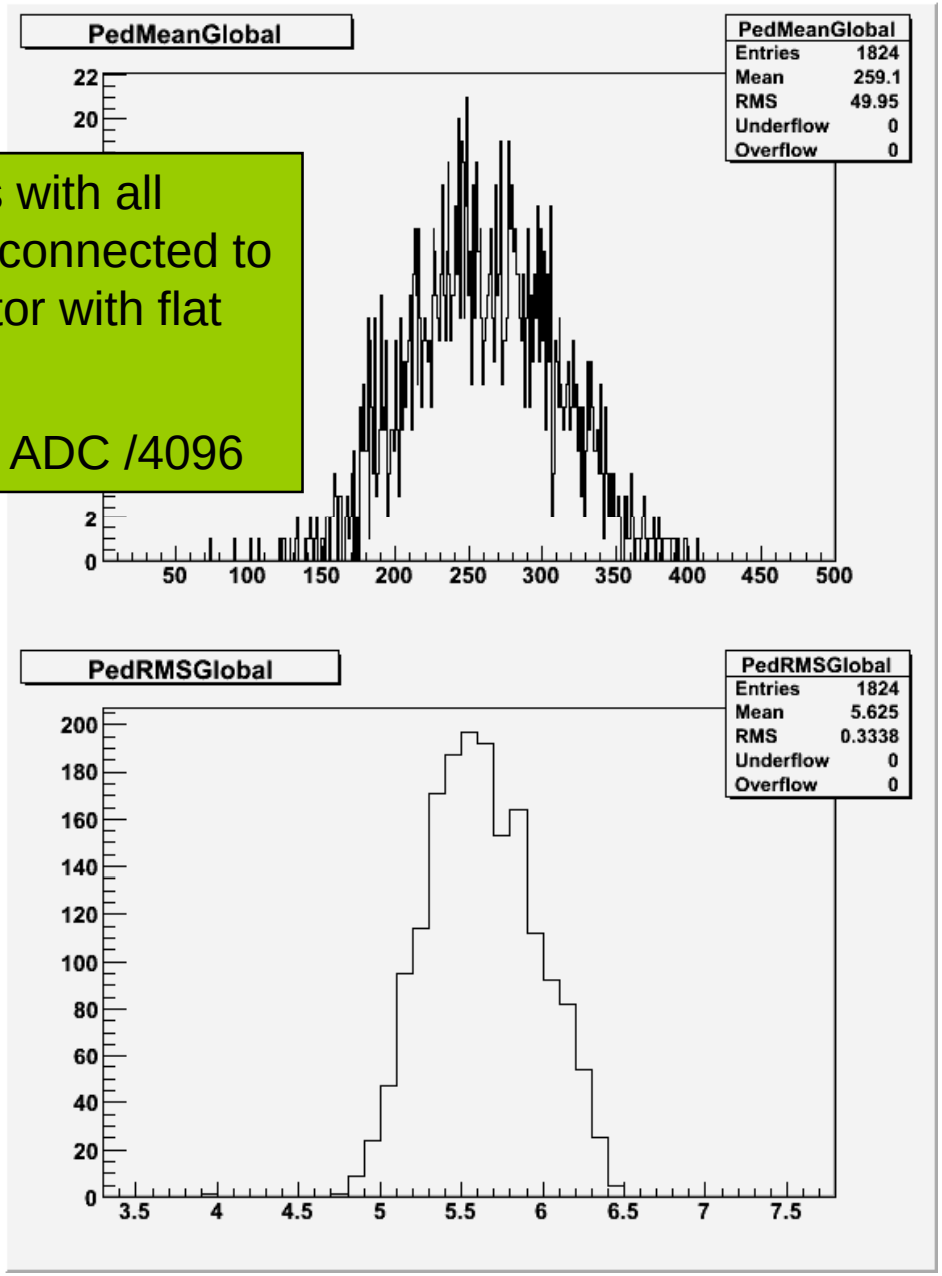



PhysPedMeanDisplay
0
5
10
15
20
0
10
20
30
40
50
60
70
400
350
300
250
200
150
100
50
0
PhysPedRMSDisplay
0
5
10
15
20
0
10
20
30
40
50
60
70
8
7
6
5
4
3

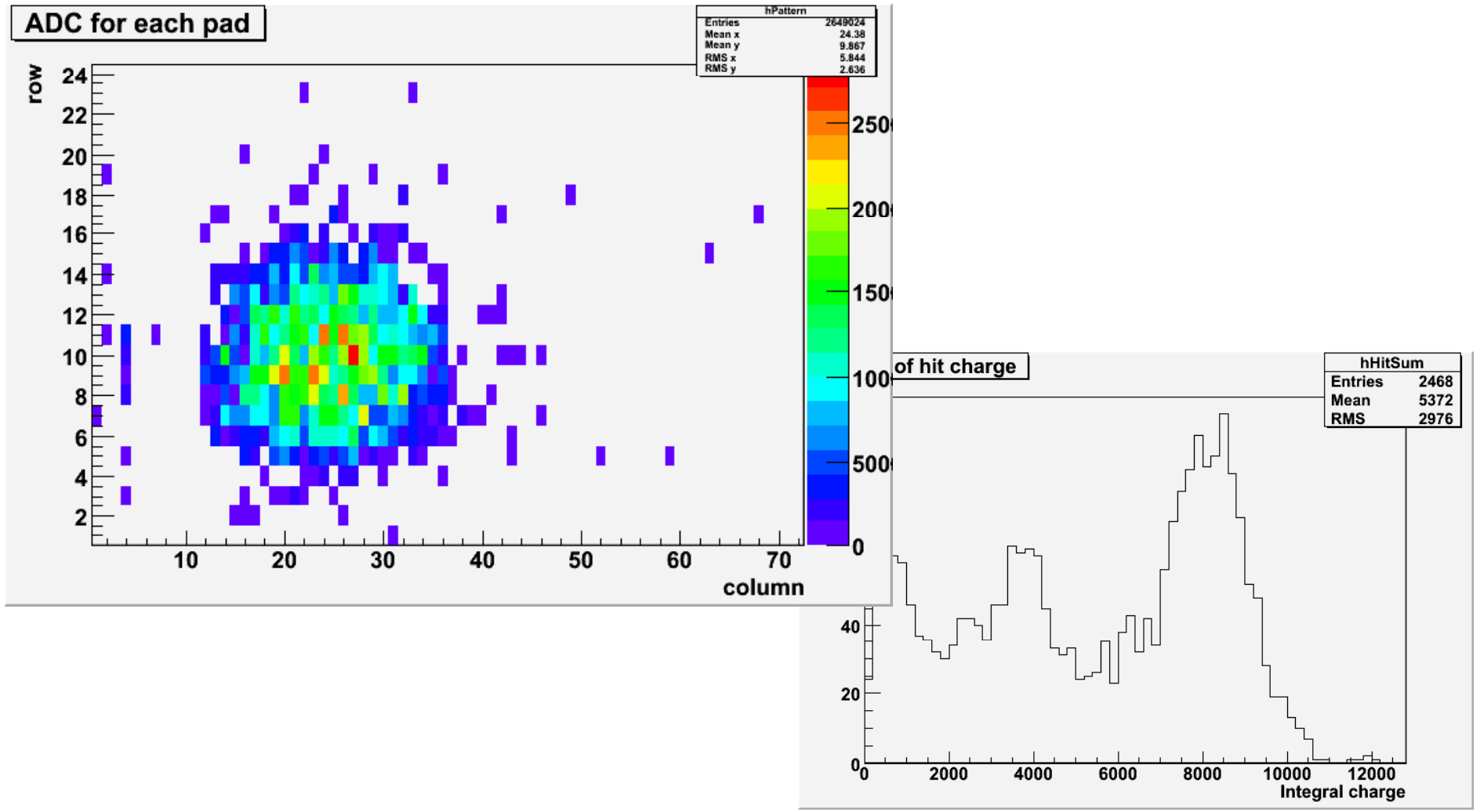


Pedestals with all channels connected to the detector with flat cables

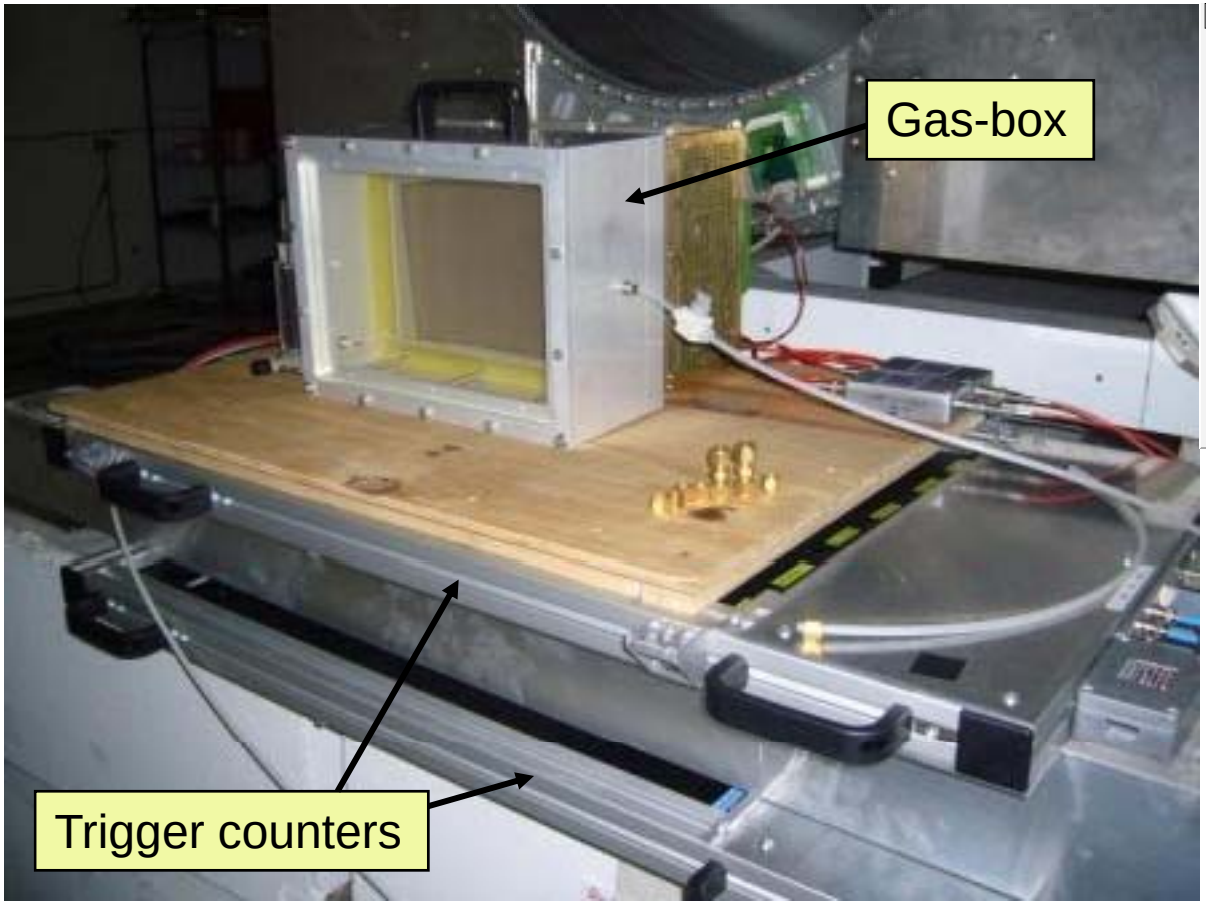
<σ> = 5.6 ADC /4096

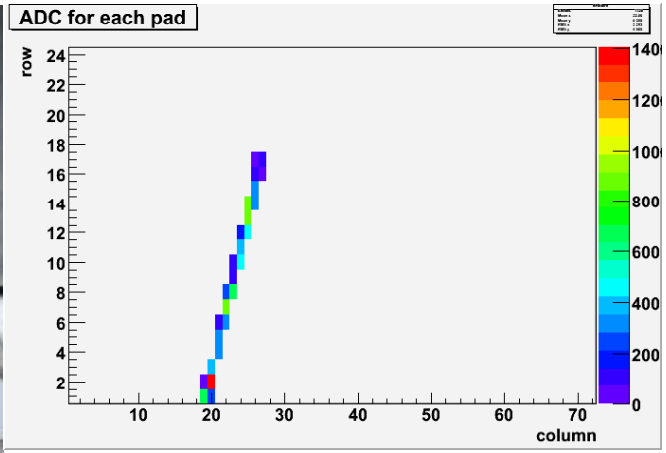


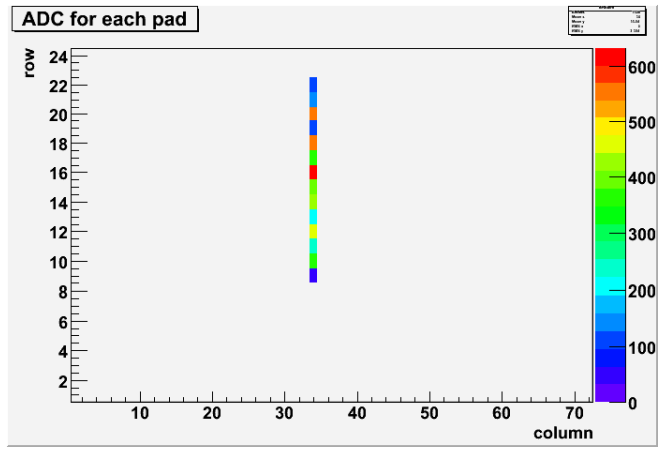
Tests at Saclay with a ^{55}Fe source

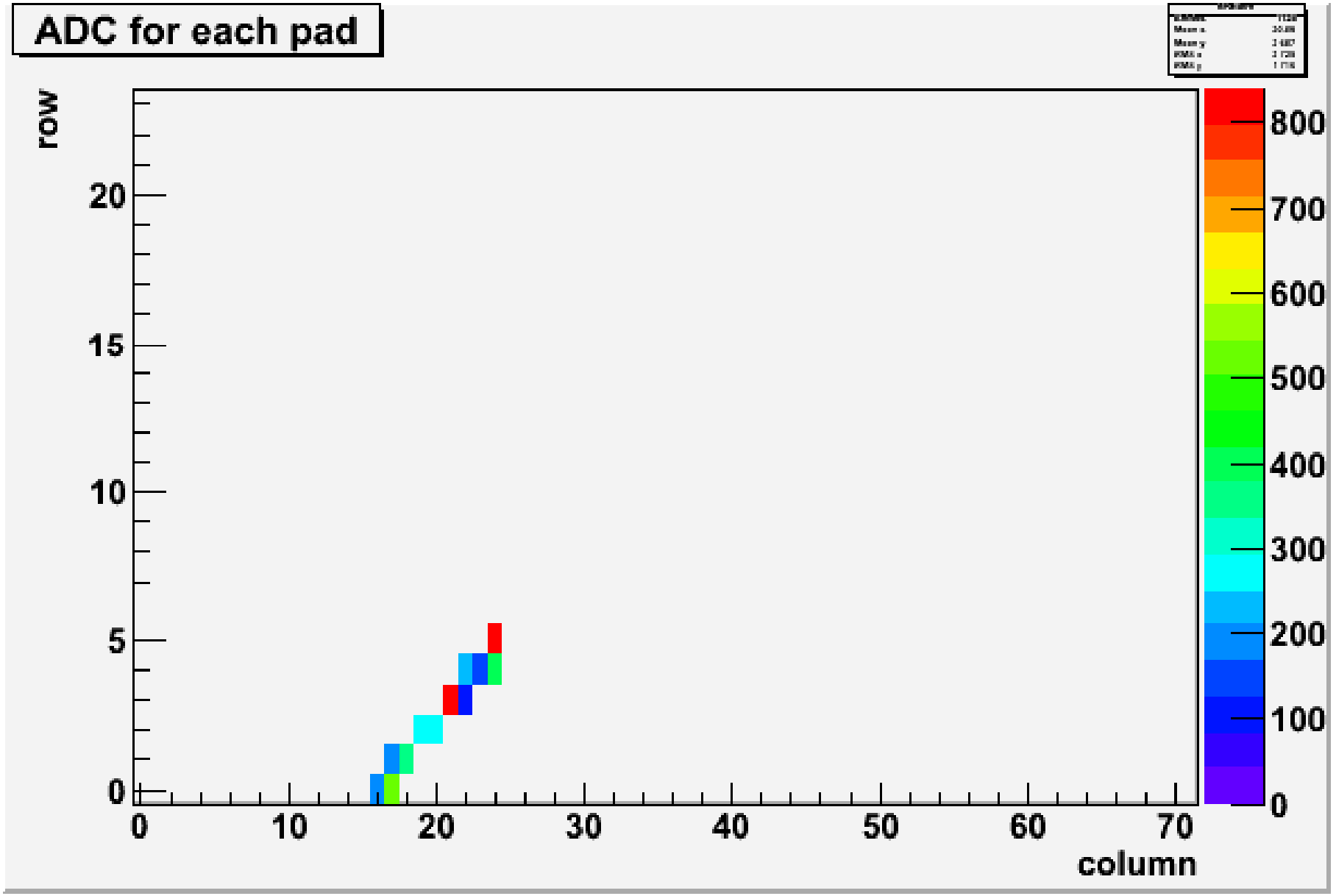


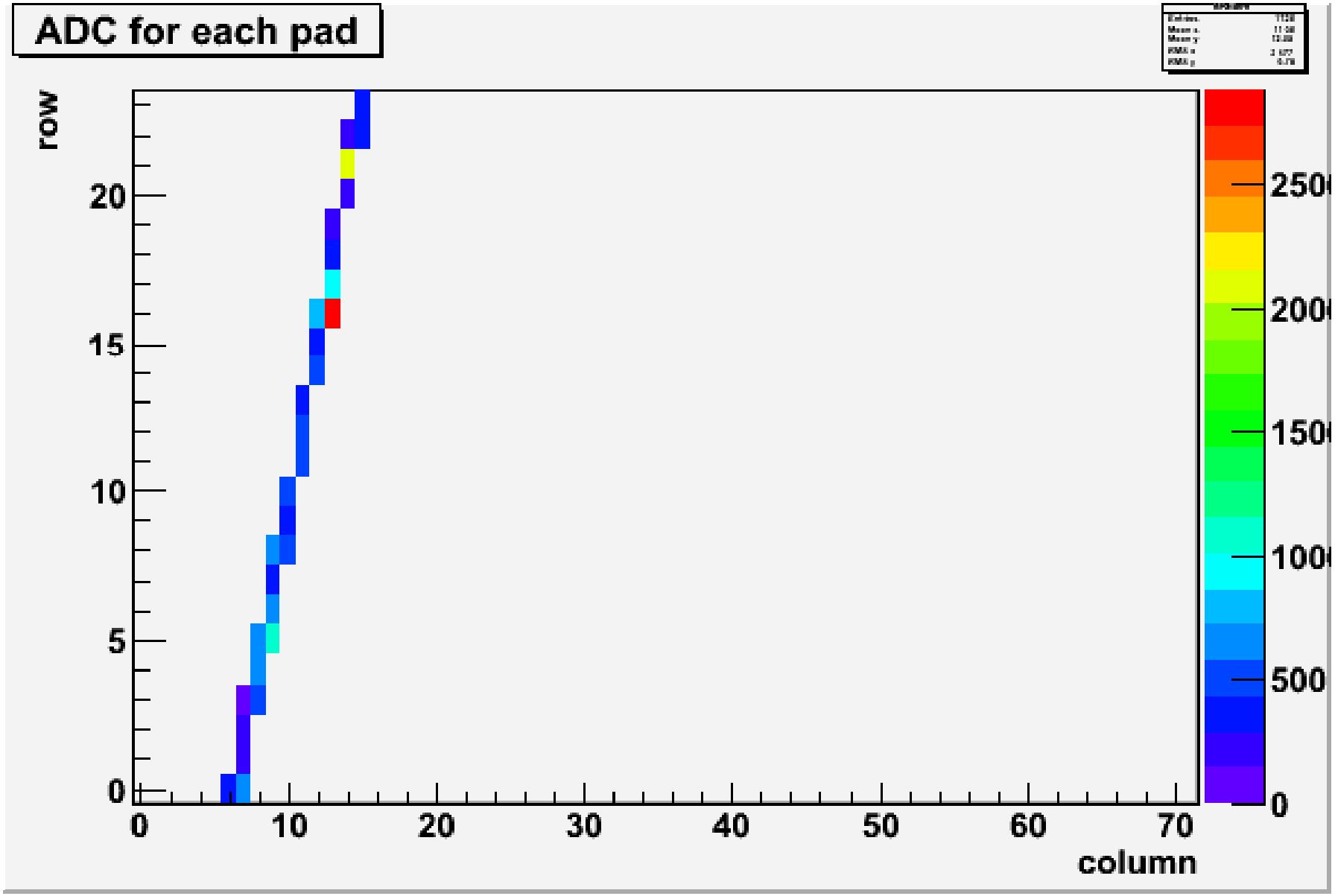
In-situ TEST at DESY

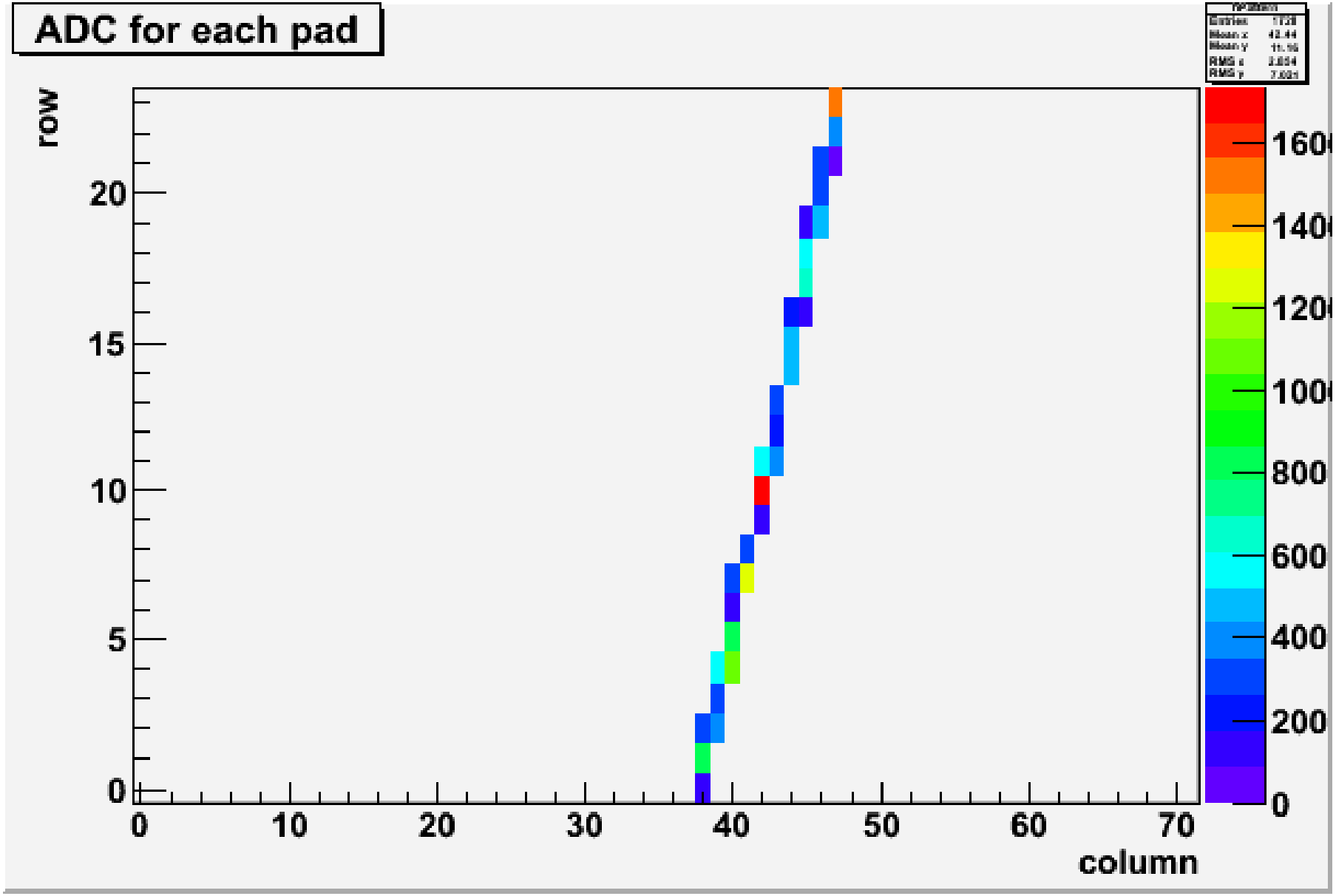







ADC for each pad
row
column
0
5
10
15
20
0
10
20
30
40
50
60
70
0
100
200
300
400
500
600
700
800


ADC for each pad
row
0
5
10
15
20
0
10
20
30
40
50
60
70
column
0
500
1000
1500
2000
2500


ADC for each pad
row
0
5
10
15
20
0
10
20
30
40
50
60
70
column
0
200
400
600
800
1000
1200
1400
1600

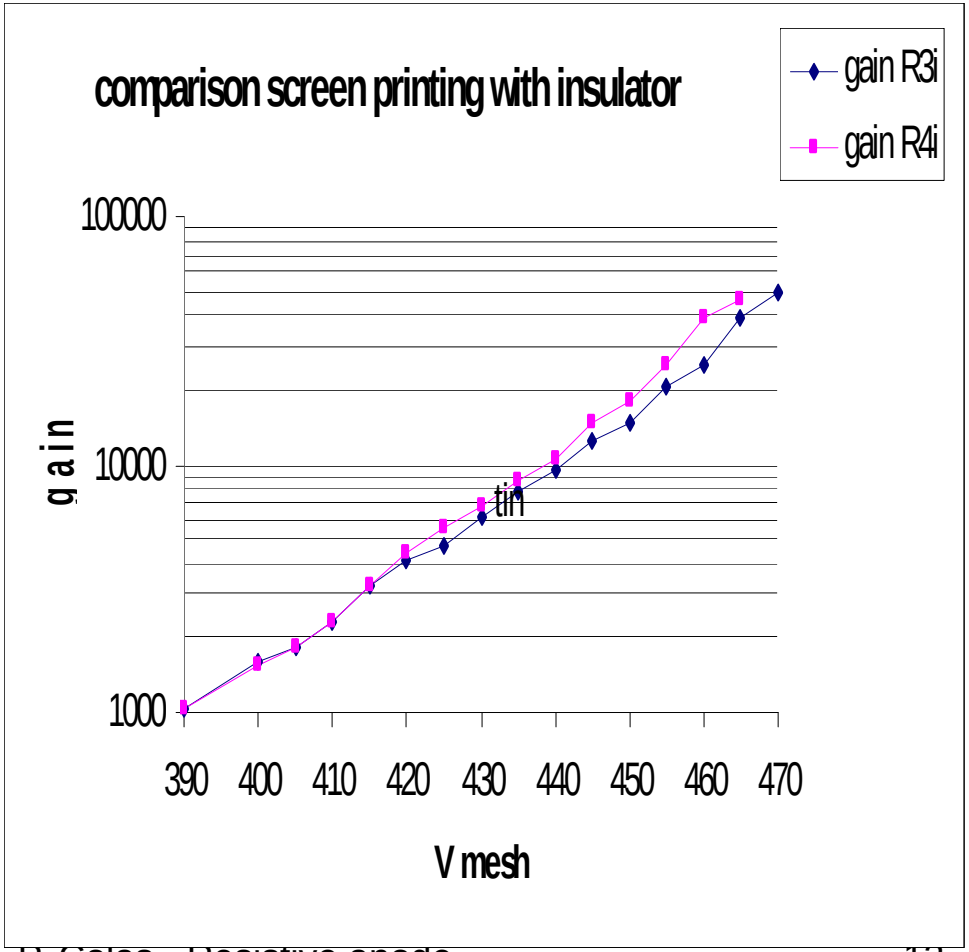
Several techniques are being tested for the resistive coating

1) Carbon-loaded kapton. An old technique first tested in Carleton, using a Dupont film 1 MOhm/sq. Improvements on application of the resistive foil and switch to bulk.

First results promising. One panel recently produced.

2) Prepreg+ screen printing

This has been tried at CERN. 2 prototypes of 10x10 cm (2 and 8 MOhm/sq) have been tried at Saclay. There is not clear evidence that they are spark protected. Even one of the detector has been damaged by the HV during the test. Still such a layer will be applied to a CERN panel.



Plasma deposition of thin layers (N. Wyrsch, Neuchatel, used for SiProt)

Preliminary tests going on. Next step: make a small bulk 12x14 cm^2 with 2 layers of different resistivity, and then cover a PCB with pads and make a bulk out of it

Future plans

Take beam data in the magnet in the period of weeks 44-45-46 (+1?) depending on the field cage status. Then other periods with various PCBs in 2009.

Start R&D for electronics on a mezzanine PCB. Should be ready for early 2010.

- R&D to optimize protection compactness

- Development to test AFTER chips at the wafer level

- new card design

Make 7 fully equipped modules (250 Watts)

Start cooling and integration studies