Summary of WG5
MPGD related Electronics

Wed. Oct. 15th , 2008

Prepared by W. Riegler, presented (and interpreted) by H. Van der Graaf

2nd RD51 Collaboration Meeting

Working Group 5 presentations

TASK 1

Definition of front-end electronics requirements for MPGDs

W. Riegler	how to proceed to arrive at a document	
A. Ranieri	the Gastone Chip	– Kloe GEM Tracker
J-P. Richer	the Mimac Chip	– Micromega TPC
R. Gaglione	the Dirac Chip	– MPGD Digital Hadron Calorimeter
A. White	the KPix Chip	– GEM Digital Hadron Calorimter

TASK 2

Development of general-purpose pixel chip for active anode readout

X. Llopard	Medipix3 chip
H. Van der Graaf	Timepix specifications

TASK 3

Development of large-area detectors with pixel readout

No presentation this time

TASK 4

Development of portable multichannel systems for detector studies

J. Toledo	proposing several options for a system.

Task1: Definition of front-end electronics requirements for MPGDs

The idea of this task is the development of common front-end requirements for MPGDs.

The necessary prerequisite for this task is a detailed understanding of MPGD signals as well as a common language for electronics parameters (e.g. ENC, Shaping time, Peaking Time etc.)

A survey of existing frontends and it's specifications and applicability should be carried out.

Questions of the following Nature should be discussed:

Do present ADCs have a power consumption that allows continuous digitization ?

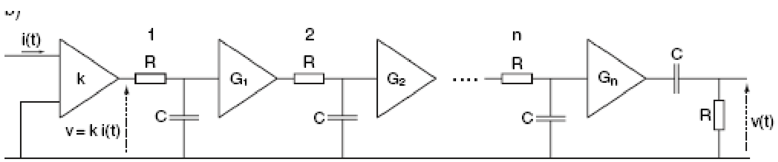
Are time over threshold measurements for charge measurement sufficient for MPGD tracking applications.

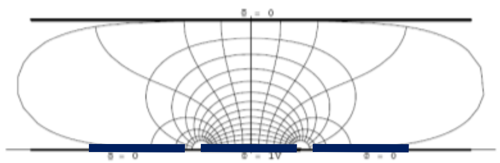
What kind of spark protection circuits have been implemented successfully ?

Many of the MPGD specification questions can be carried out by Simulations.

We want to write a document on this in the near future. we have to get organized and work on it …

An outline of the report will be circulated soon among the Persons/Institutes that indicated interest in this task (WG5: Task1) such that we can define who does studies what.





Task1: Definition of front-end electronics requirements for MPGDs

A Ranieri:

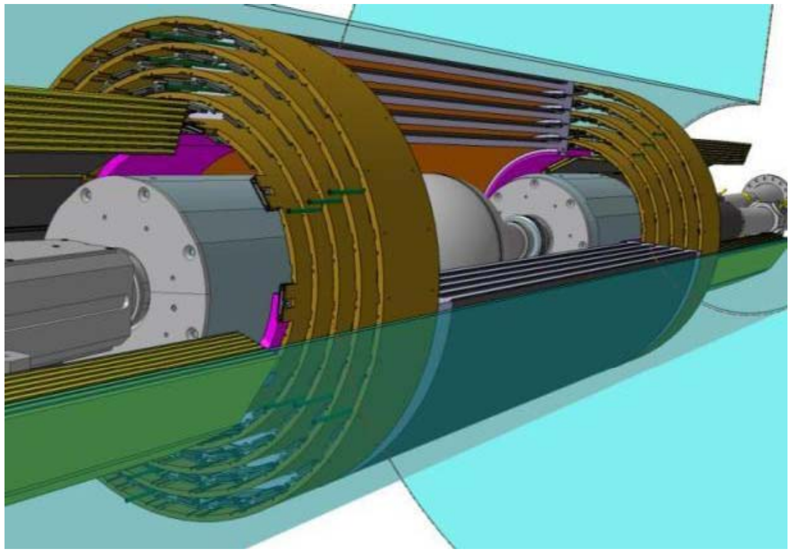
GASTONE (Gem Amplifier Shaper Tracking ON Events) A prototype Front-End chip for the KLOEInner Tracker Detector

Readout Chip for Cylindical GEM Tracker upgrade,

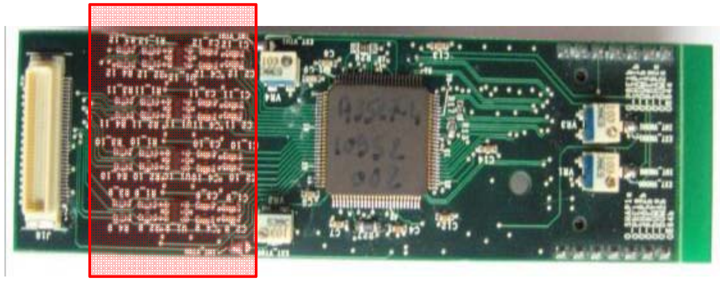
0.35um AMS CMOS: 16 channel prototype, Amplifier, RC-RC Shaper, Discriminator

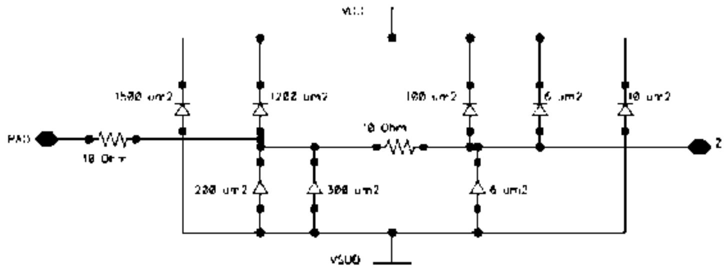
Aim for 64 channel prototype in early 2009

Input impedance	400 Ω
Total Gain sensitivity	25 mV/fC
Peaking time	90 ns÷200 ns (C_D=0 ÷50 pF)
ENC (rms) measured on detector	974 e^- + 59 e^-/pF
Power consumption	0.6 mA/Ch



Try to put space consuming Input protection circuit into the chip





Task1: Definition of front-end electronics requirements for MPGDs

J-P. Richer :

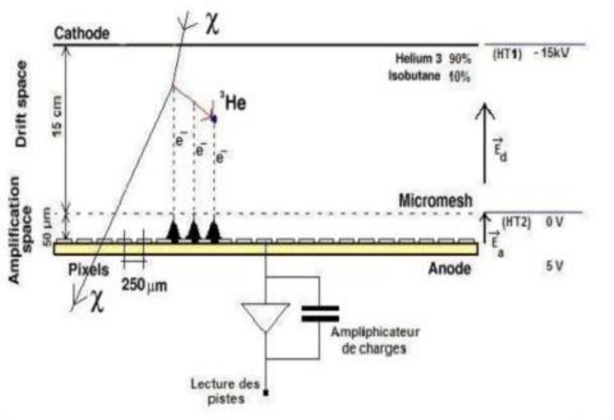
Chip MIMAC for the ^{3}He+^{19}F Micro-TPC Matrix of Chambers

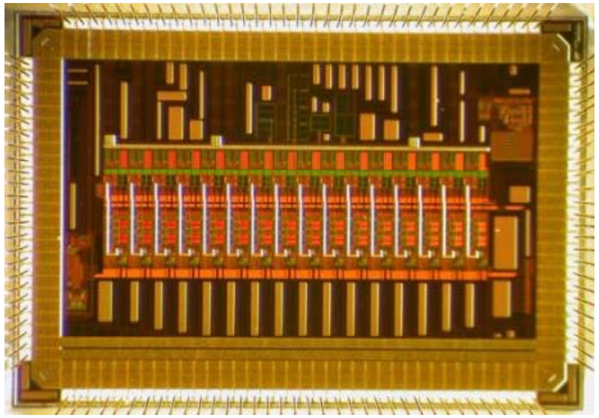
Readout Chip for Micromega TPC

0.35um AMS CMOS: 16 channel prototype, Amplifier, RC-RC^{3} Shaper (200ns), Discriminator, 40MHz Output

Offset Variations to be addressed

Probably go to 64 channels in next iterations





Task1: Definition of front-end electronics requirements for MPGDs

R. Gaglione:

DIRAC: Digital Readout ASIC for Hadronic Calorimeter

Readout Chip Digital MPGD based (GEM, MICROMEGA, RPC) Hadron Calorimeter at ILC

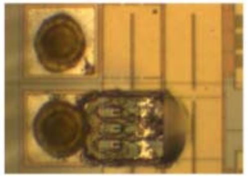
0.35um AMS CMOS: 64 channels, 2 gains 0.1mV/fC, 5mV/fC

<1mW/channel Power consumption → <10uW per channel in pulsed mode with 1% ILC duty cycle.

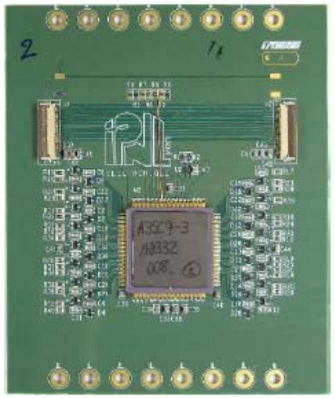
3 Thresholds – coarse energy measurement

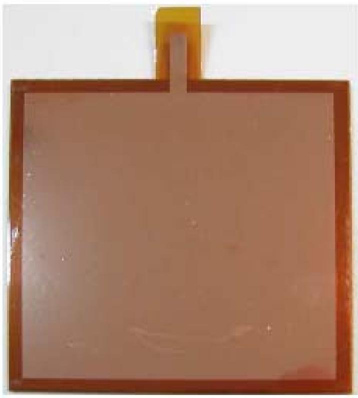
Offset Variations to be addressed

Input protection to be addressed



Readout PCM – MICROMEGA on one side, Chip on other side 'monolythic'.





Task1: Definition of front-end electronics requirements for MPGDs

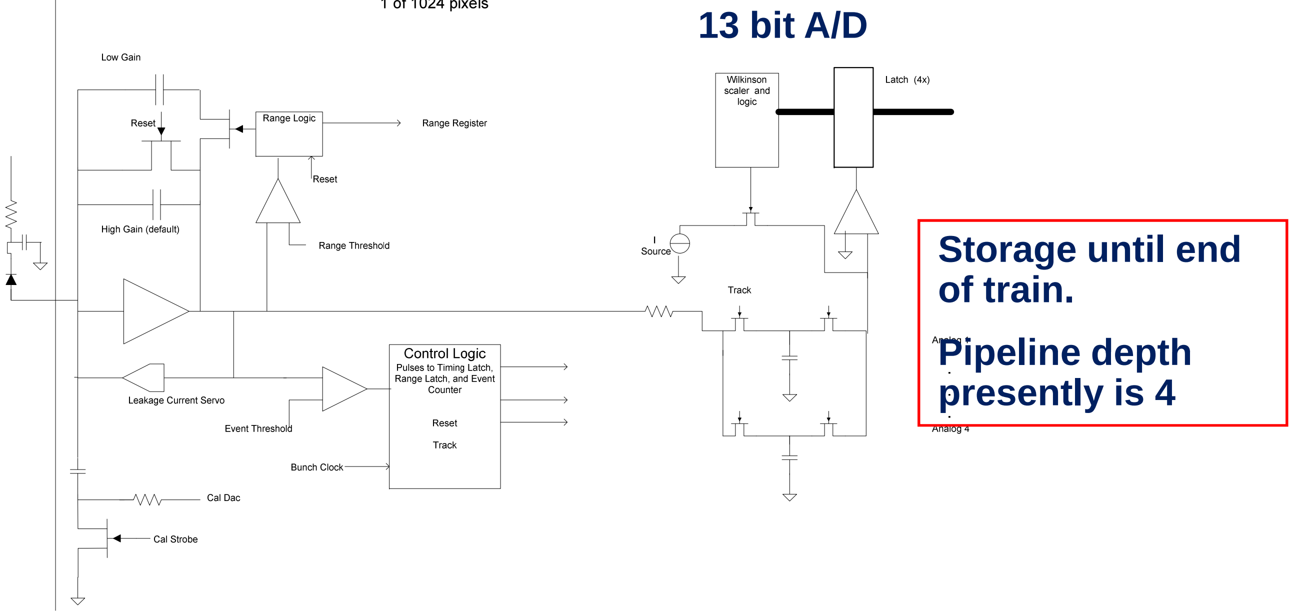
A . White:

The SLAC KPiX Chip for ILC GEM-Digital Hadron Calorimetry

Plan to have 1024 channels in the final Chip

Si-W Pixel Analog Section

1 of 1024 pixels



Simplified Timing:

There are ~ 3000 bunches separated by ~300 ns in a train, and trains are separated by ~200 ms.

Say a signal above event threshold happens at bunch n and time T0.
The Event discriminator triggers in ~100 ns and removes resets and strobes the Timing Latch (12 bit), range latch (1 bit) and Event Counter (5 bits).
The Range discriminator triggers in ~100 ns if the signal exceeds the Range Threshold.
When the glitch from the Range switch has had time to settle, Track connects the sample capacitor to the amplifier output. (~150 ns)
The Track signal opens the switch isolating the sample capacitor at T0 + 1 micro s. At this time, the amplitude of the signal at T0 is held on the Sample Capacitor .
Reset is asserted (synched to the bunch clock) . Note that the second capacitor is reset at startup and following an event, while the high gain (small) capacitor is reset each bunch crossing (except while processing an event)
The system is ready for another signal in ~1.2 microsec.
After the bunch train, the capacitor charge is measured by a Wilkinson converter.

Task1: Definition of front-end electronics requirements for MPGDs

Conclusion on the 4 presented Chip developments:

Specifications of the analog part are very similar (ASDs with 100-200ns peaking time)

Observed problems are very similar – Input protection – offset variations

The digital part of the chips is quite different and adapted to the specific experimental environment (Kloe, ILC …)

Whether there could be a common multipurpose chip that satisfies all requirements is difficult to tell. We should at least establish contacts between the developers and have discussions on common issues (inout protection, power consumption, offset variations …)

Task2: Development of general-purpose pixel chip for active anode readout

X. Llopard:

Experience with the design and submission of the Medipix3 pixel readout chip in 0.13 µm CMOS

The Medipix3 chip is the first 130 nm engineering run organized through the CERN HEP service.

The Medipix3 prototype demonstrated the principle of local communication between pixels to solve charge sharing effects.

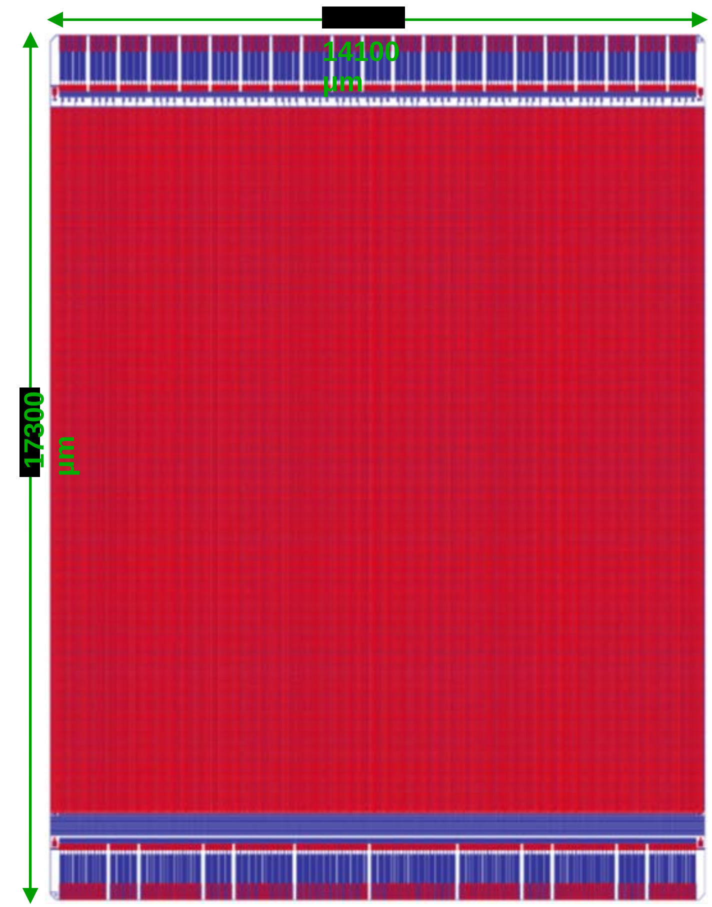
From there still took 4 man-years (3 people) for the completion of the design. Why?

- Change of BEOL technology from the prototype
- New programmable counter
- Many unavailable blocks (DACs, LVDS driver and receiver, e-fuse bits, …)
- Use new tools for the first time (MRE, CALIBRE LVS, …)

Experience gained should reduce design time for future projects

Chip was sent to IBM 24th September !!!

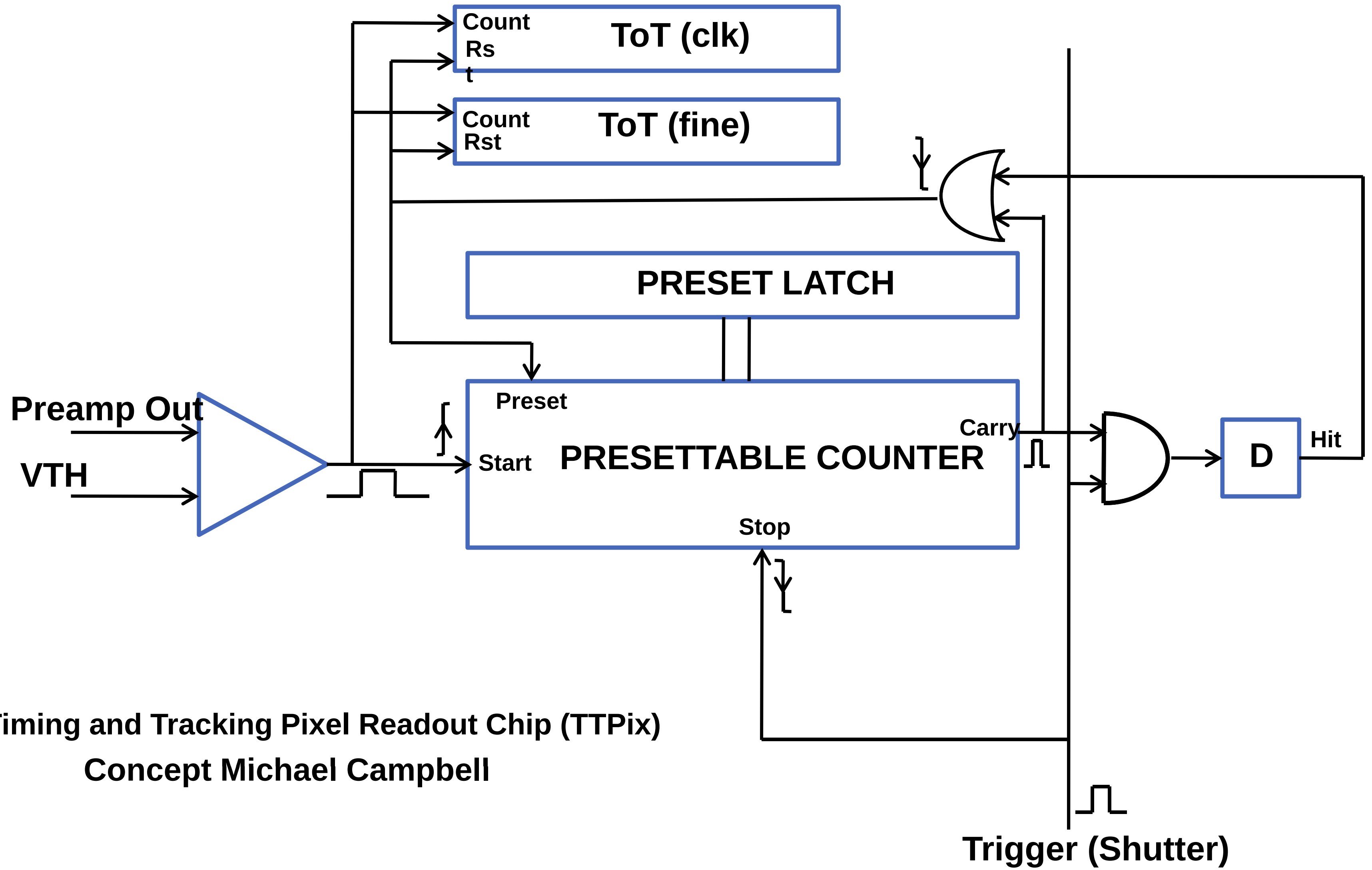
→ Hopefully back as 2009 Christmas present.



Task2: Development of general-purpose pixel chip for active anode readout

H. Van der Graaf:

TimePix-2 requirements



Timing and Tracking Pixel Readout Chip (TTPix)

Concept Michael Campbell

Task2: Development of general-purpose pixel chip for active anode readout

How to proceed:

Using the Experience and achievements from MPIX3 effort is essential.

Common Silicon, Gas Detector specs seem possible.

Medipix Consortium is interested. Probably want to wait for MPIX3 result.

Final definition of Specifications and technical design work can go ahead.

All interested parties should meet, possibly around MPIX3 workshop end of Nov. 2008 at CERN, in order to define financial and organizational aspects.

Task3: Development of large-area detectors with pixel readout

Need to organize presentations for next meeting …

Task4: Development of portable multichannel systems for detector studies

J. Toledo:

Discussion on portable multichannel systems for MPGDs

Digital Systems Design Group of Universidad Politecnica de Valencia has lots of experience in designing and building readout and DAQ systems.

They are interested in providing systems for RD51. → Excellent offer !

We will have close contact with them from now on in order to get a first definition of a system that uses available electronic (e.g. VFAT etc.

UNIVERSIDAD POLITECNICA DE VALENCIA

Conclusion

Jobs for the coming months:

Prepare the MPGD electronics Document

Kick off “Timepix 2, TTPix” Collaboration

Define Components of Portable Electronics System