DIRAC: DIgital Readout Asic for hadronic Calorimeter

2nd RD51 workshop, Paris

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Plan

Introduction

Architecture

ASIC Characterisation (in Micromegas mode)

Tests with detectors

What's next ?

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Requirements : detectors

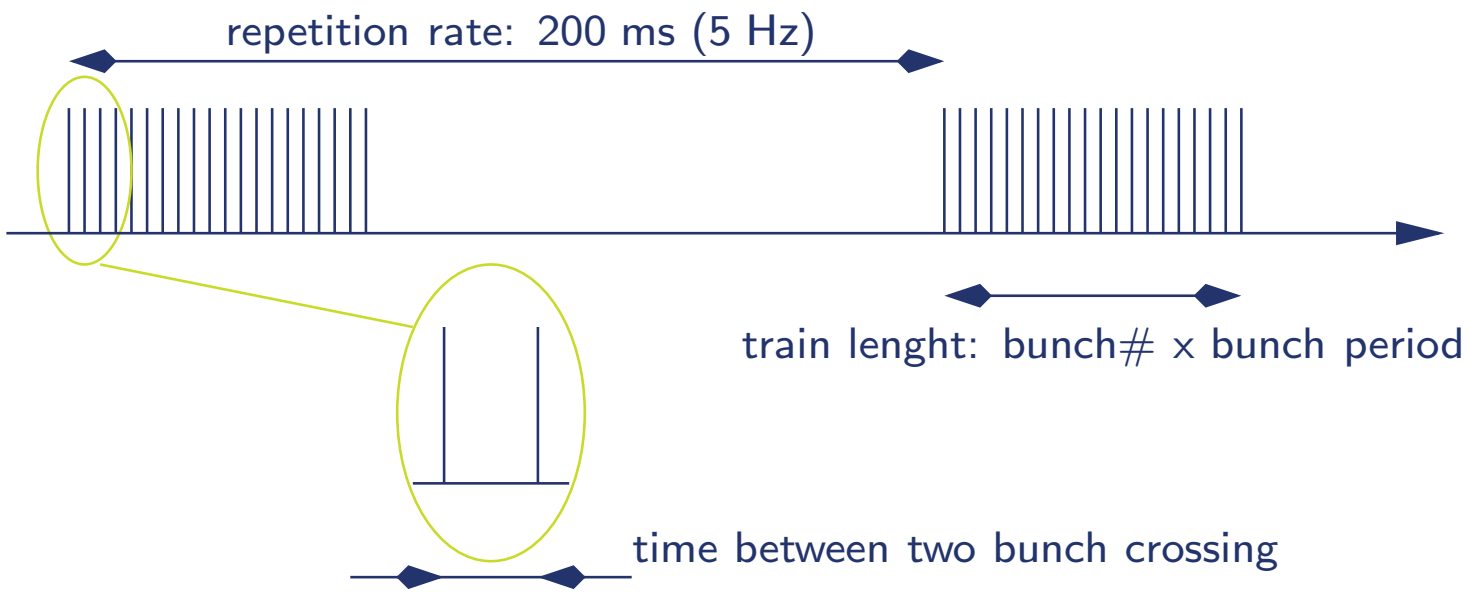
In order to build a Digital Hadronic CALorimeter with very high granularity at the ILC, frond end ASIC prototype must match different gaseous detectors to select which one is best:

	GRPC	MicroMegas	GEM
Charge	0.1∼10 pC	1∼100 fC	1∼100 fC
C_{det} (1 cm^2)	60 pF	60 pF	60 pF
t_r	2 ns	<2 ns	<2 ns
width	20 ns	complex form	20 ns

Requirements : beam structure

Front-end timing must respect beam clock characteritics:

	Minimum	Nominal	Maximum
Bunch#	1320	2625	5120
Period (ns)	189	369	480
Rate (Hz)		5	



Additionaly, the front end is shutted down during inter-train period to save power.

Aims of this development

The design is driven by he following constraints:

- Low cost ASIC (about 30 millions of channels !);
- Low power ASIC (*idem* !);
- Decrease PCB complexity (6 layers, easy routing, few external components);
- Try to suppress calibration needs (electronic channel disparity requirements not so strong for a DHCAL).

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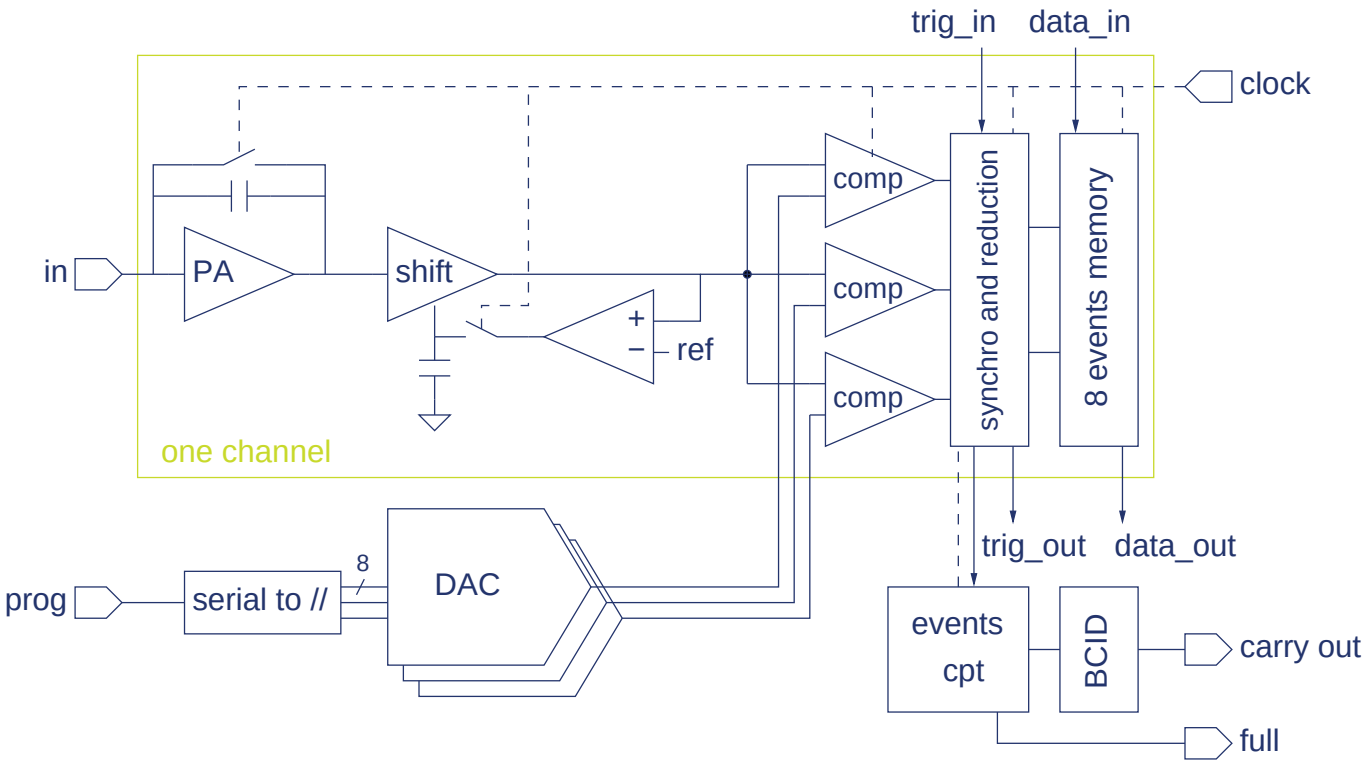
Synoptic

Compare input charge to 3 thresholds (set by 3 DACs) and store the 2 bits energy information.



Gated integrator : less sensitive to signal shape (different detectors) !

Operation

Synchronous architecture on beam clock (trains and bunchs):

During trains:

- Beam on: analog charge integration;
- Beam off: comparisons to thresholds, store results.

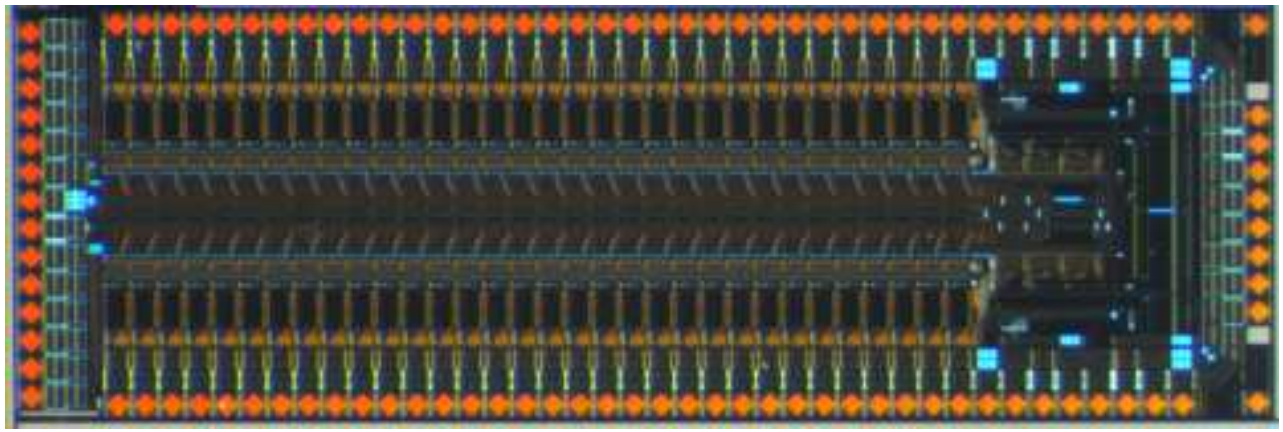
Outside trains:

- Standby analog front-end;
- Digital data readout;
- Slow control.

Main features summary

- 64 channels;
- Low-cost AMS CMOS 0.35 µm process technology;
- Power consumption <1 mW per channel + 1% power pulsing:
  → <10 µW per channel
- 2 gains: 100 mV/pC and 5 mV/fC;
- 3 thresholds, each on 8 bits for 1 V, *i.e.* 3.9 mV/DAC:
  → 40 fC/DAC (Micromegas, GEM)
  → 0.8 fC/DAC (RPC)
- 12 bits BCID counter;
- Internal memory of 8 events (2 bits per event);
- Analog input on each sides: easy PCB routing.

Photography



Only 1.5×4.7 mm^2

- Top and bottom: analog inputs;
- Right: analog power supply and bias;
- Left: digital I/O.

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Prototype characterisation

For each input charge:

- Measure trigger efficiency *vs* thresholds;
- *S-Curves*: fit with a Fermi-Dirac distribution:

$$S(x) = \frac{max}{1 + e^{\frac{x-\mu}{w}}}$$

max : maximum efficiency
μ : inflexion point abcisse
w : inflexion slope

Next:

- μ *vs* input charge for each channel;
- Linear fit:

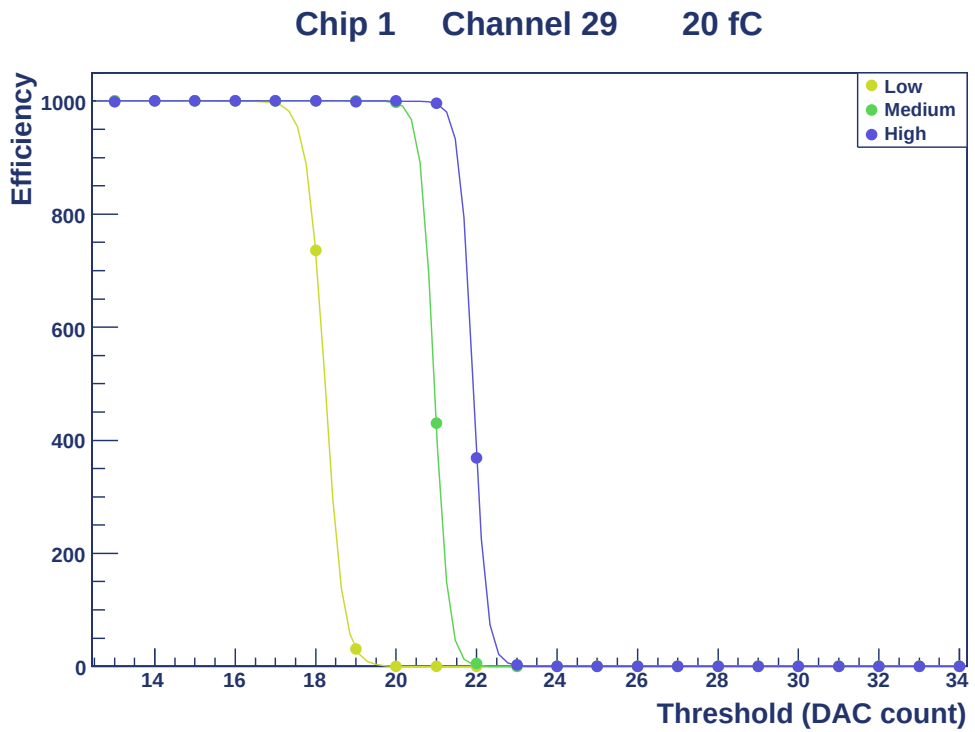
$$F(x) = 1/g \cdot x + b$$

g : gain
b : pedestal

- Non-linearity: difference between fit and measurements.

S-Curve

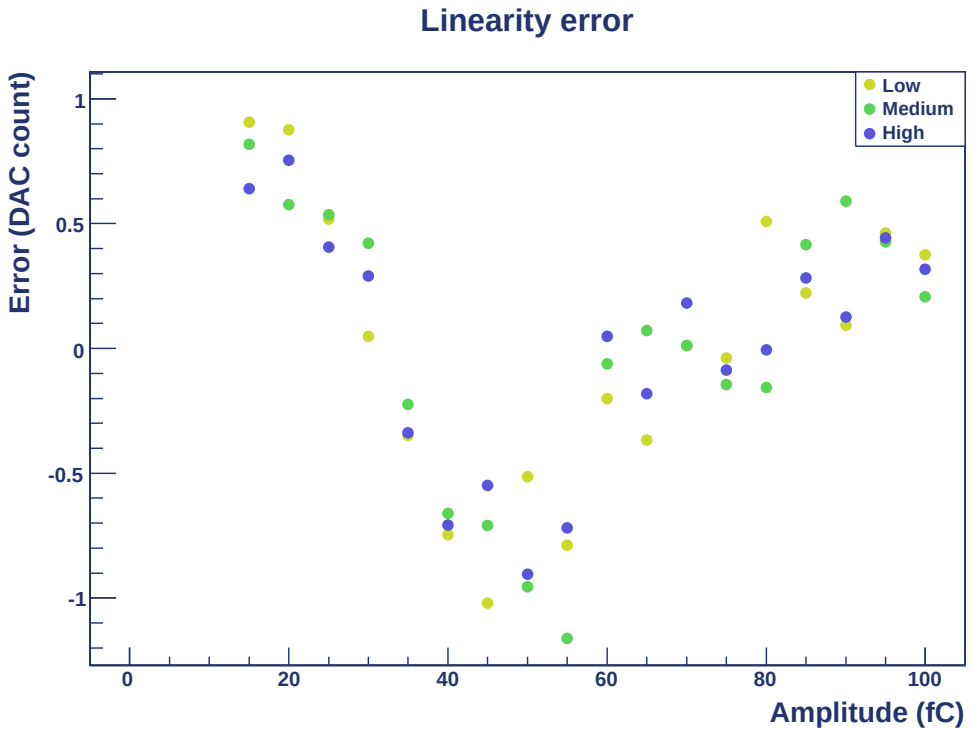
Example on 1 channel: 20 fC input charge: efficiency versus threshold for the 3 comparators.



Statistics on all channels: from 100% to 0% <2.4 fC
Worst dispersion between 3 comparators: 2.5 DAC code, *i.e.* 2 fC.

Integral non-linearity

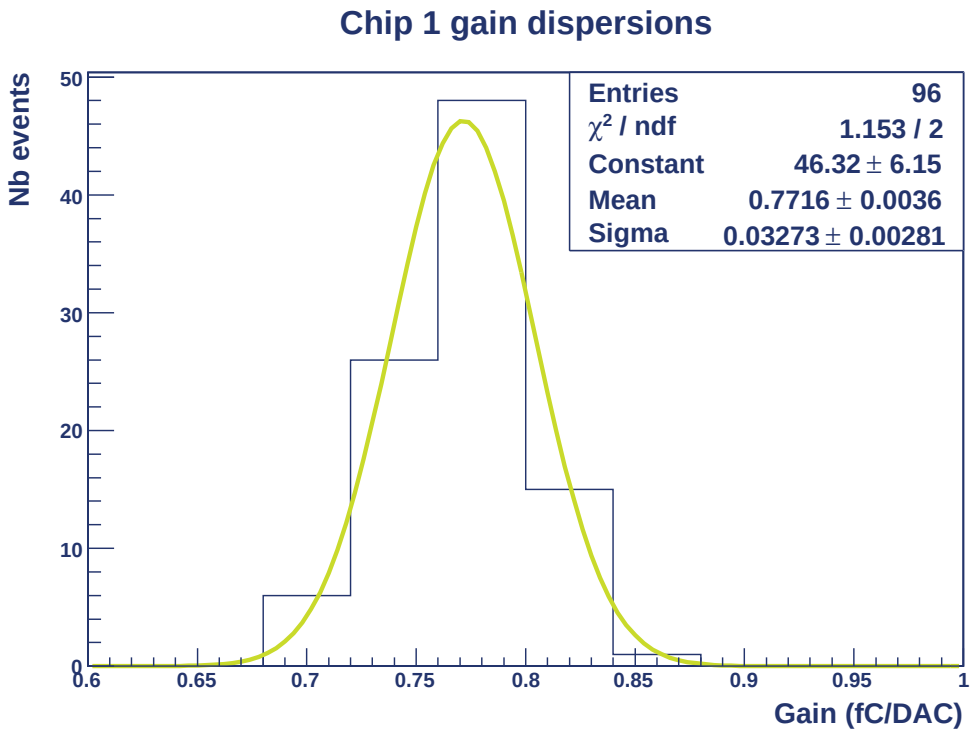
Difference between linear fit and measurements (1 channel):



The non-linearity is typically in ± 1 DAC code, *i.e.* ± 0.8 fC.

Gain dispersions

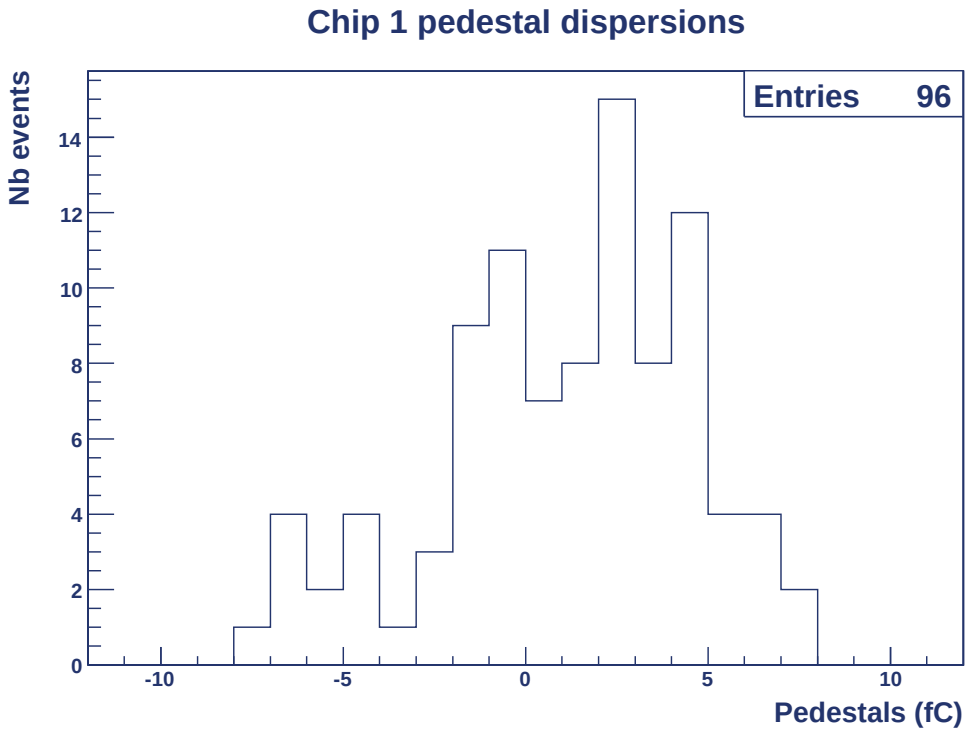
g distribution for all channels (1 ASIC):



Mean value of g: 0.77 fC/DAC code.

Pedestals dispersion

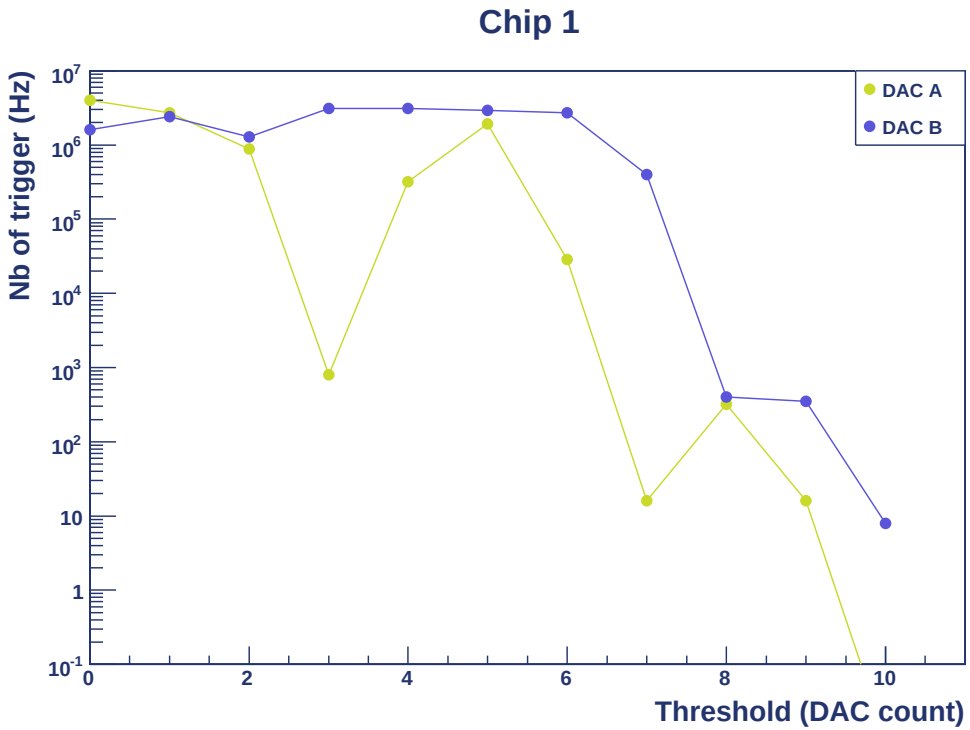
$b \cdot g$ distribution for all channels (1 ASIC):



Monte-Carlo Simulation: gaussian with σ=1 DAC code;
Measure: non-gaussian, total dispertion $\pm$ 10 DAC code:
comparators offset must be improved !

Auto-triggering

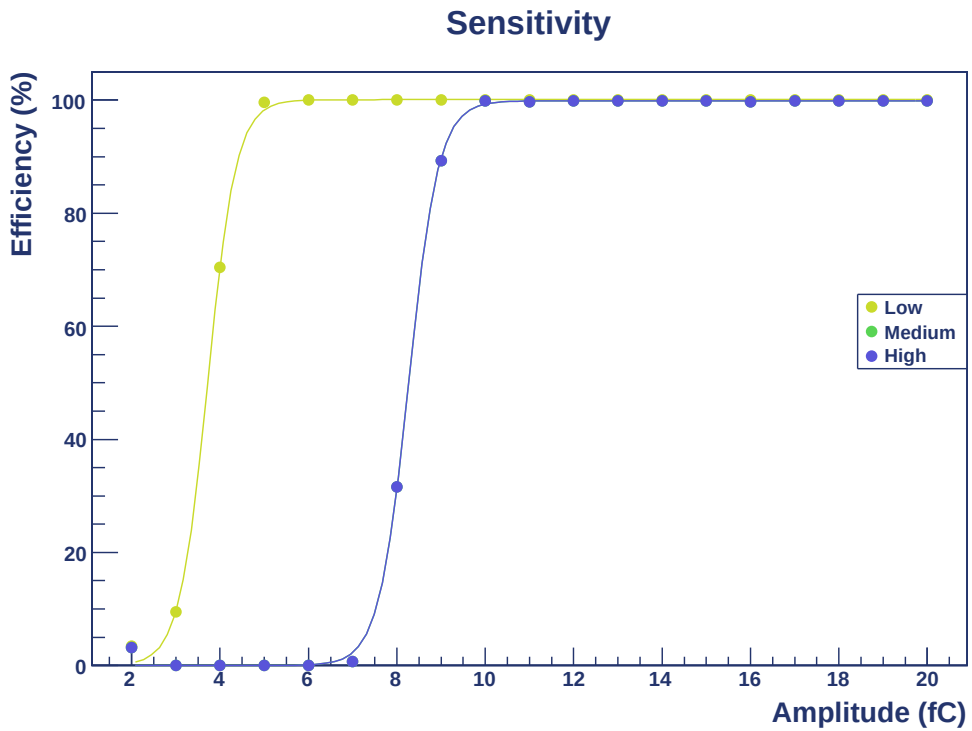
No input charge. False trigger rate versus threshold.



Channels with high pedestals stop to auto-trig @ threshold near DAC code=10 (8 fC).

Sensitivity

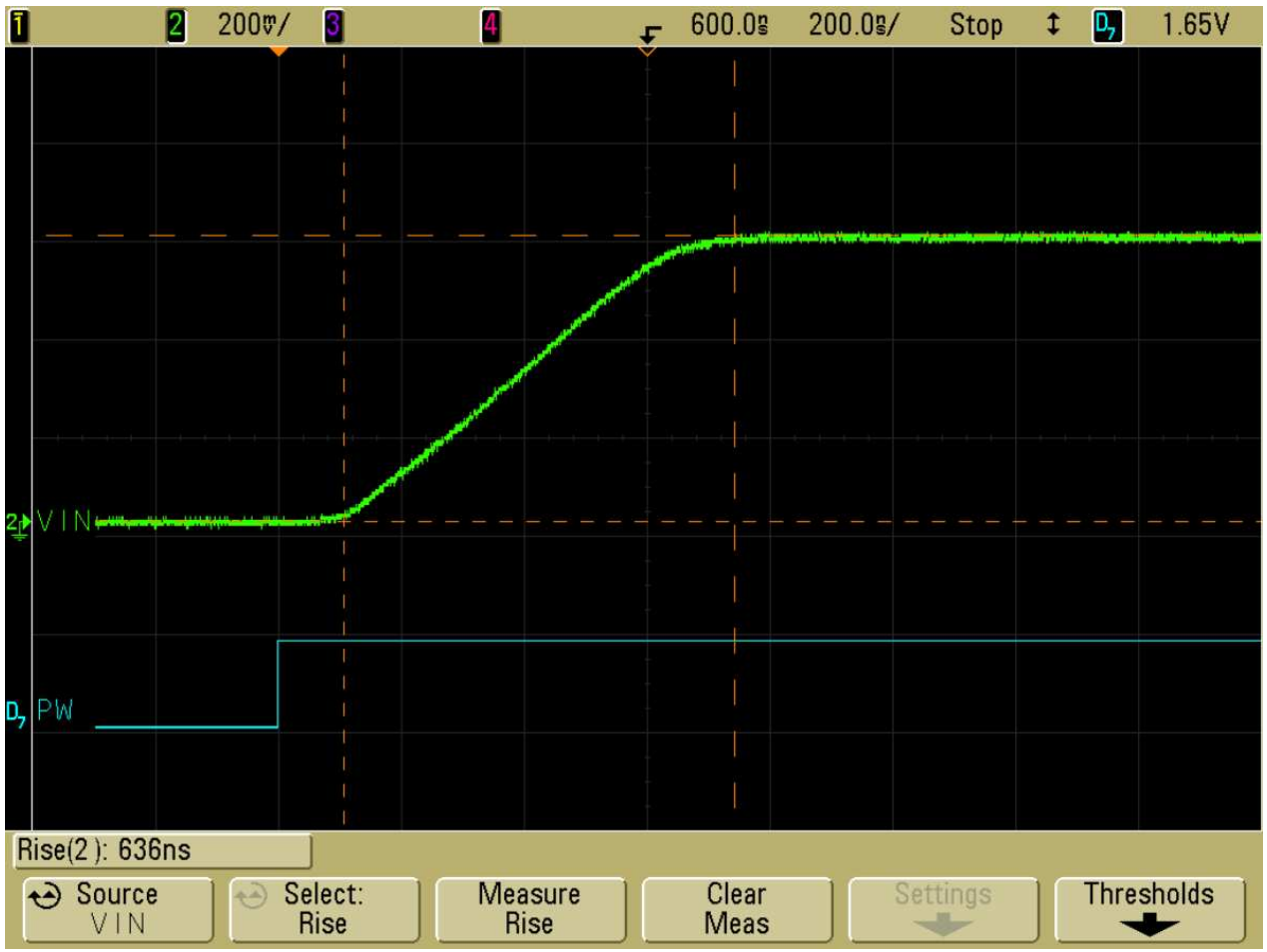
DAC code: 14 (above auto-triggering threshold).
Trigger efficiency *vs* input charge.



Best 50% efficiency: 3.5 fC.

Power pulsing

Power on time <800 ns (preamplifier input voltage *vs* time).



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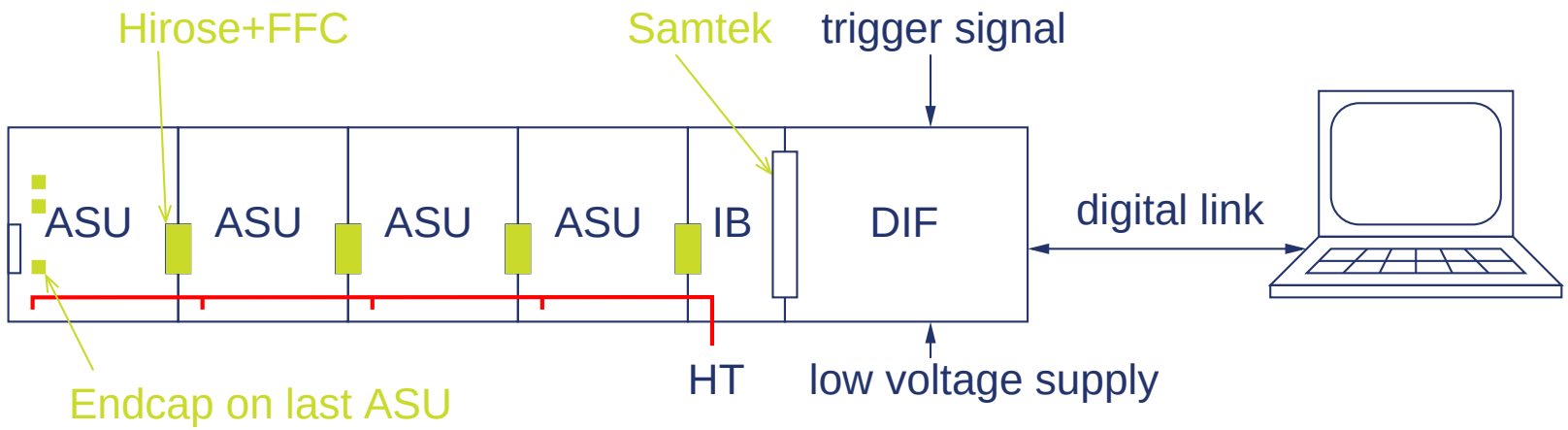
Assembly schematic overview

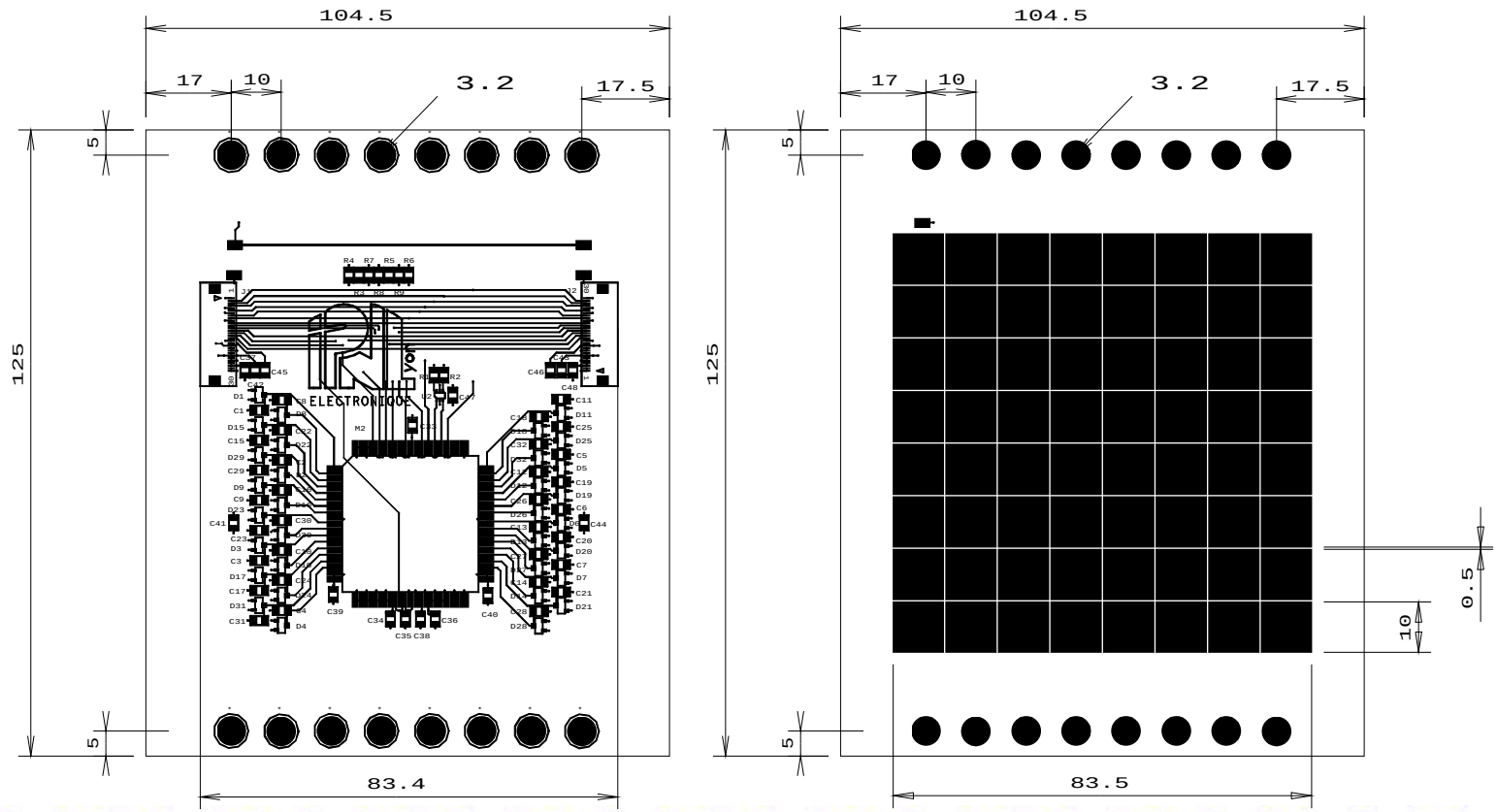
ASU: Active Sensor Unit
IB: Intermediate Board
DIF: Digital InterFace



Present: custom DAQ with ethernet for characterisation and august testbeam;
Futur: connection to the CALICE DIF and DAQ.

Active Sensor Unit boards

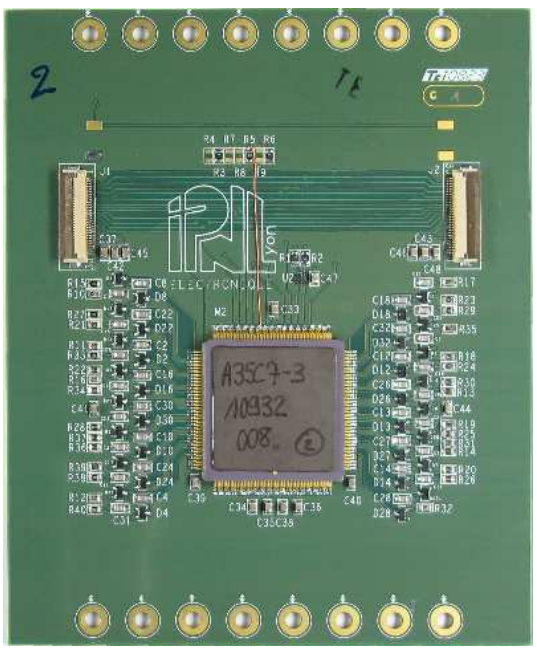
6 layers, 1.6 mm thick. Burried and blind vias for anode connection.
Digital daisy chain. 8×8 anodes of 1 cm^2 each.
MicroMegas sparks protections.
For Micromegas or RPC operation.

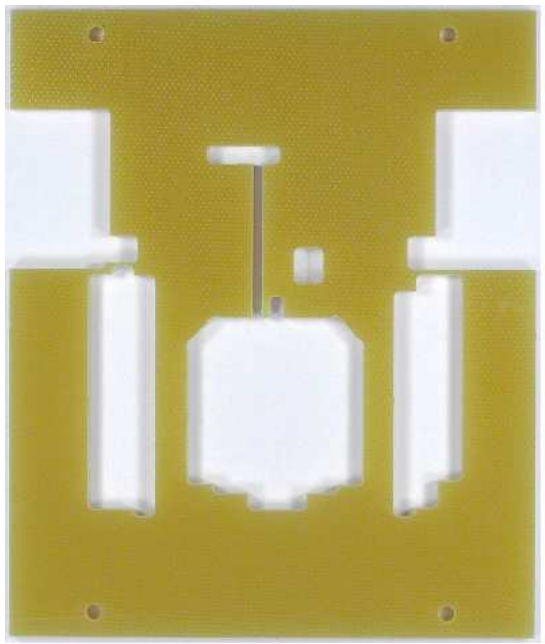


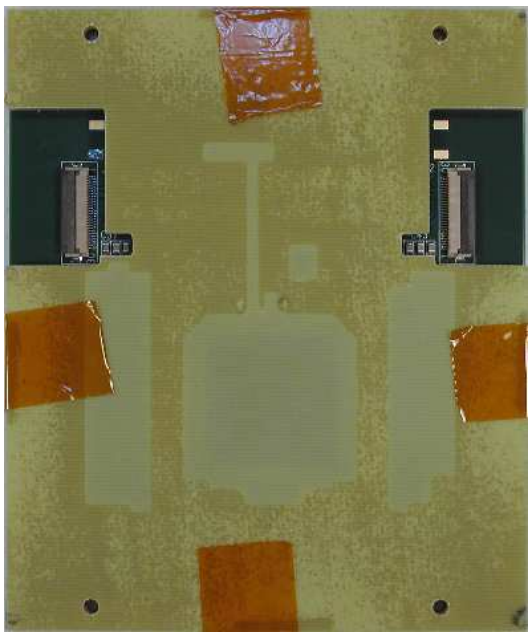
Micromegas Active Sensor Unit (1)

PCB and ASIC made by IPNL/IN2P3/CNRS
Bulk lamination by CERN (R. De Oliveira)
Detector assembly made by LAPP/IN2P3/CNRS (C. Adloff)

PCB + glued epoxy mask (flat top needed for lamination)

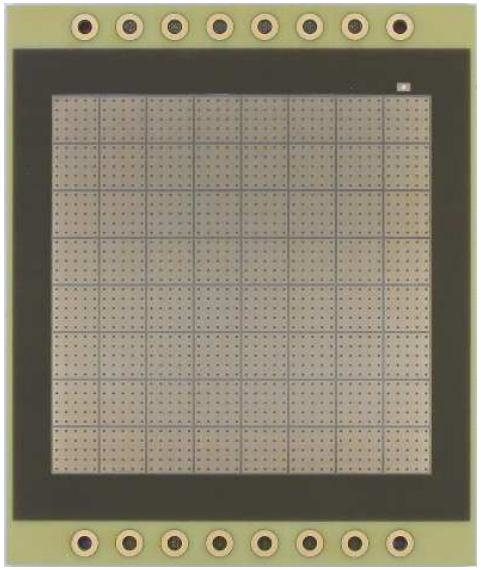


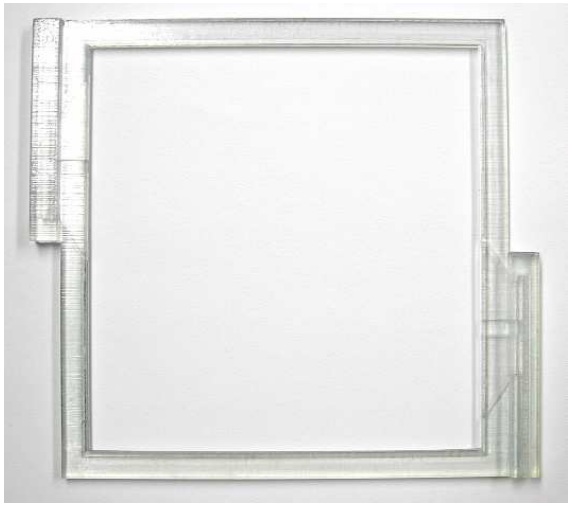


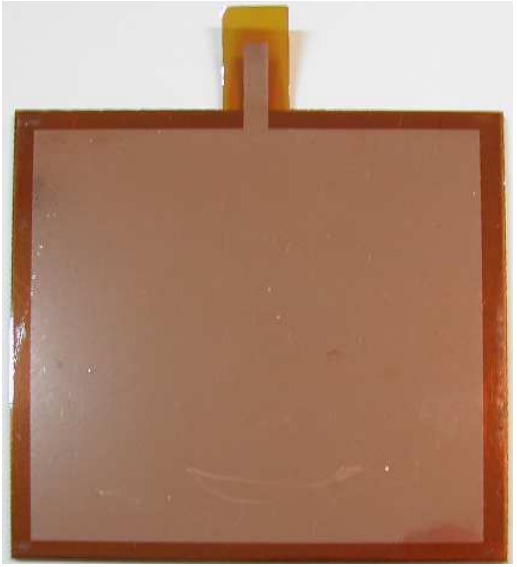


Micromegas Active Sensor Unit (2)

Laminated mesh on PCB + frame + drift cathode. . . .

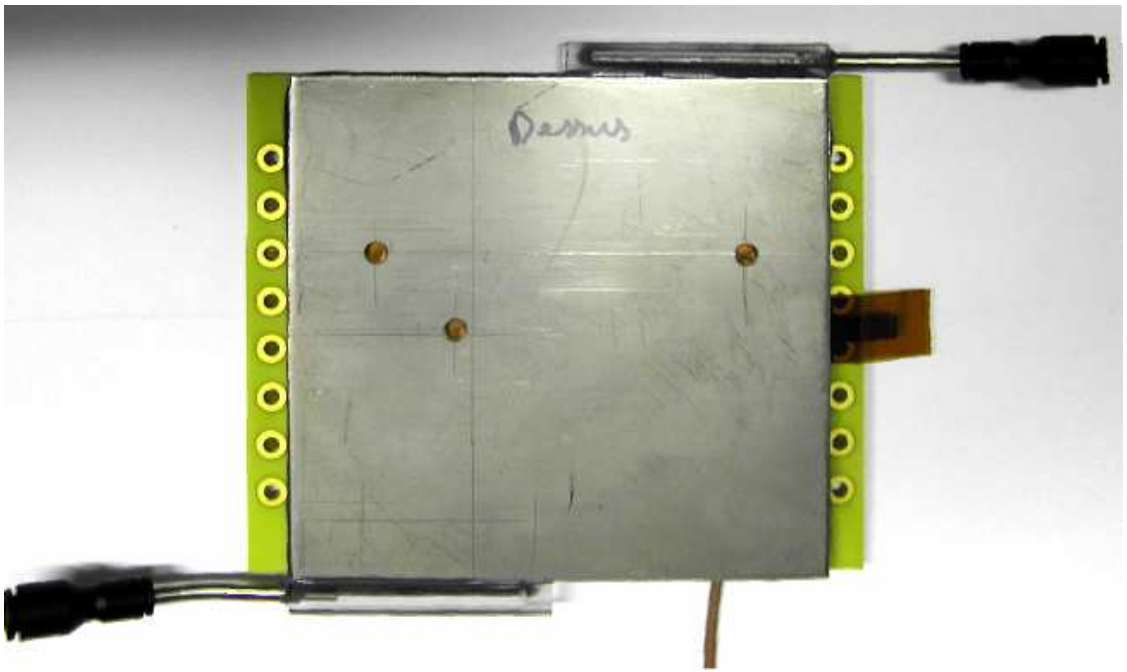






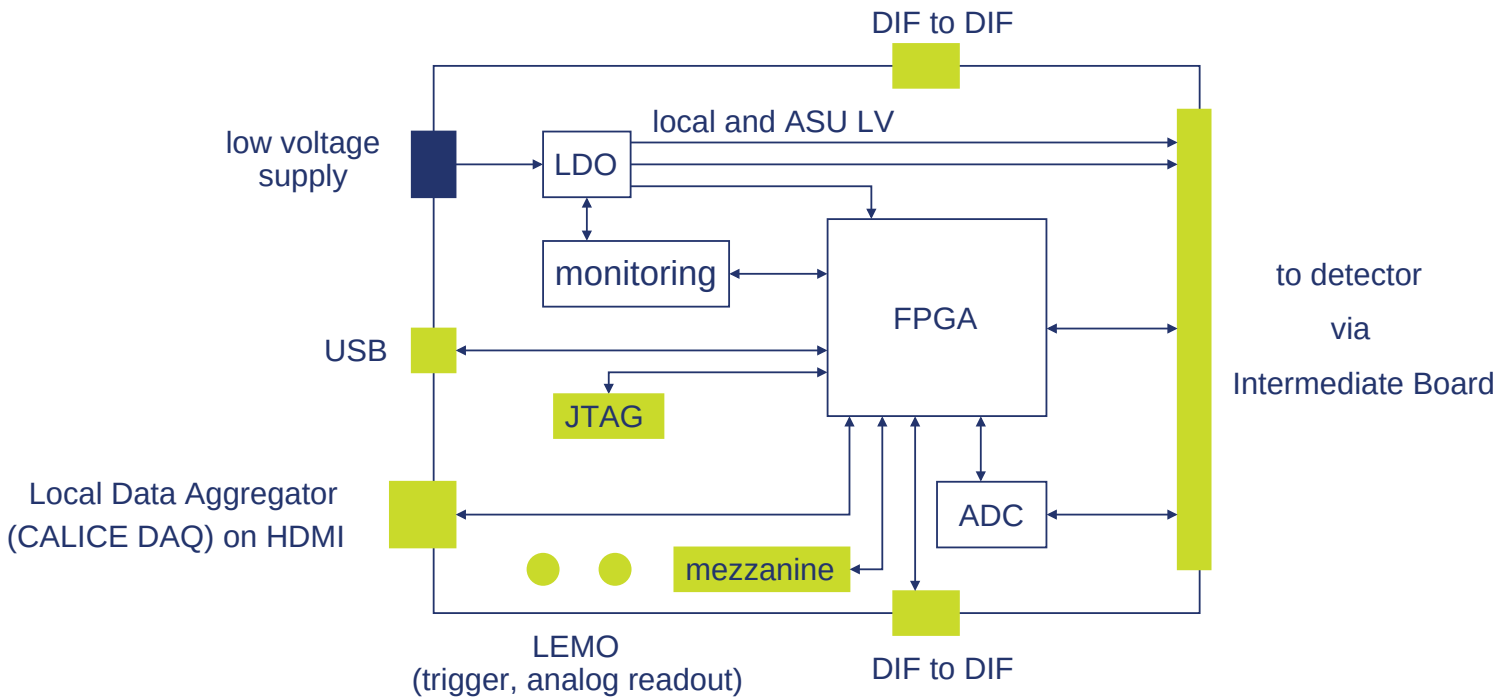
Micromegas Active Sensor Unit (3)

. . . add gaz inlets/outlets and HV connection: complete Micromegas chamber!



Digital InterFace boards

Hardware and firmware developed at LAPP/IN2P3/CNRS.
CALICE LDA DAQ connection for large area detector.



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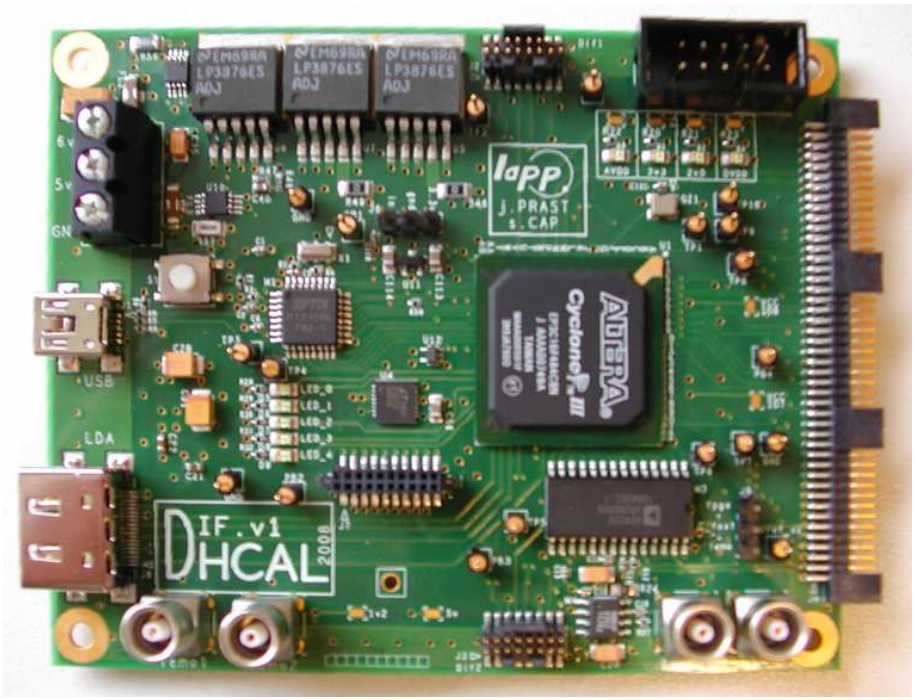
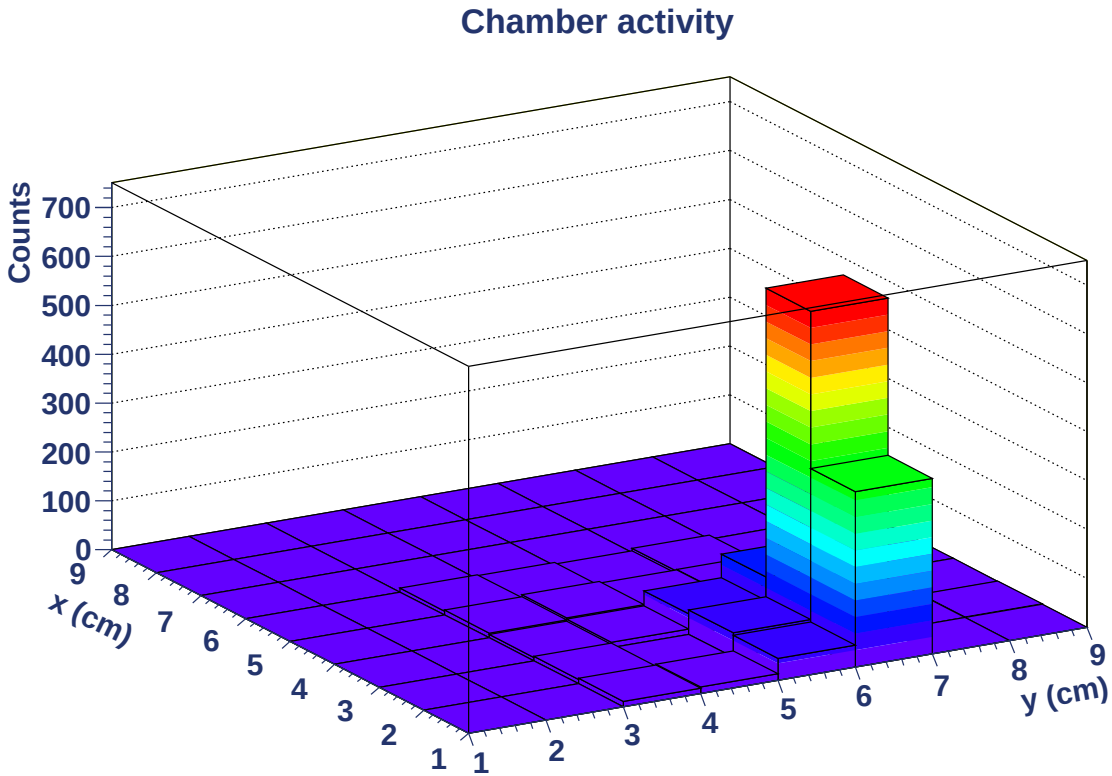


Test beam preliminary results

Detector fixed on a moving table with muon beam: we clearly see the table movement accros x axes and the y axis misalignment of the chamber!



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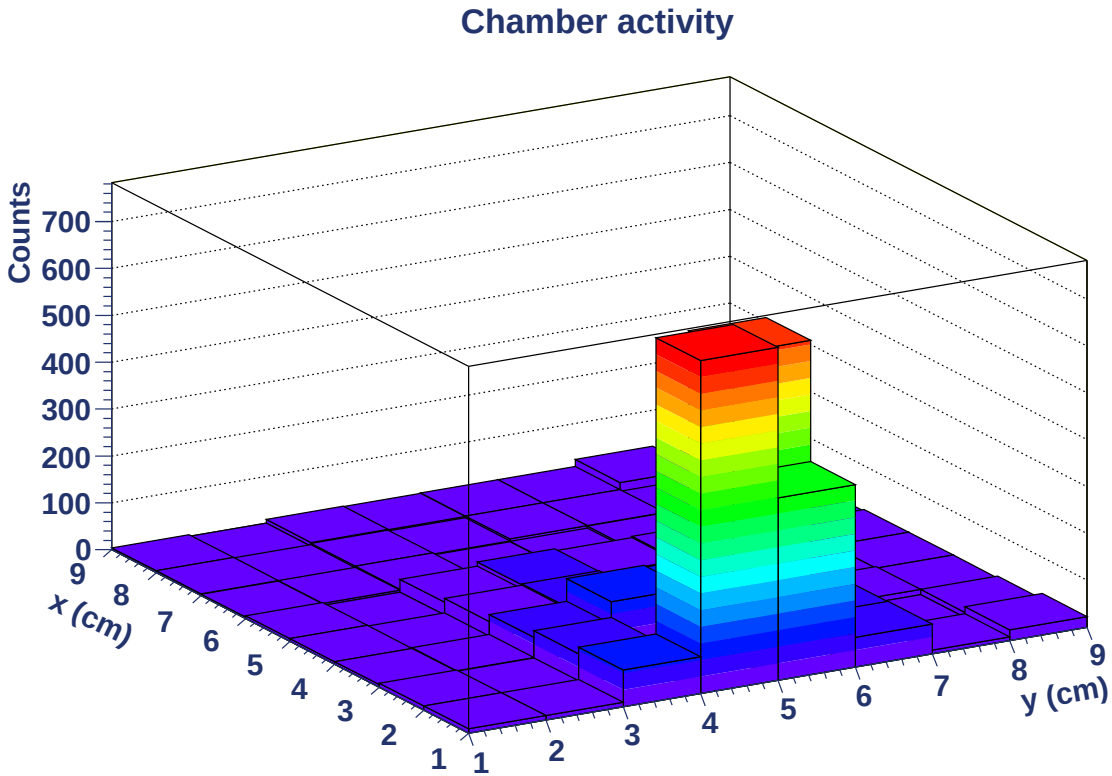

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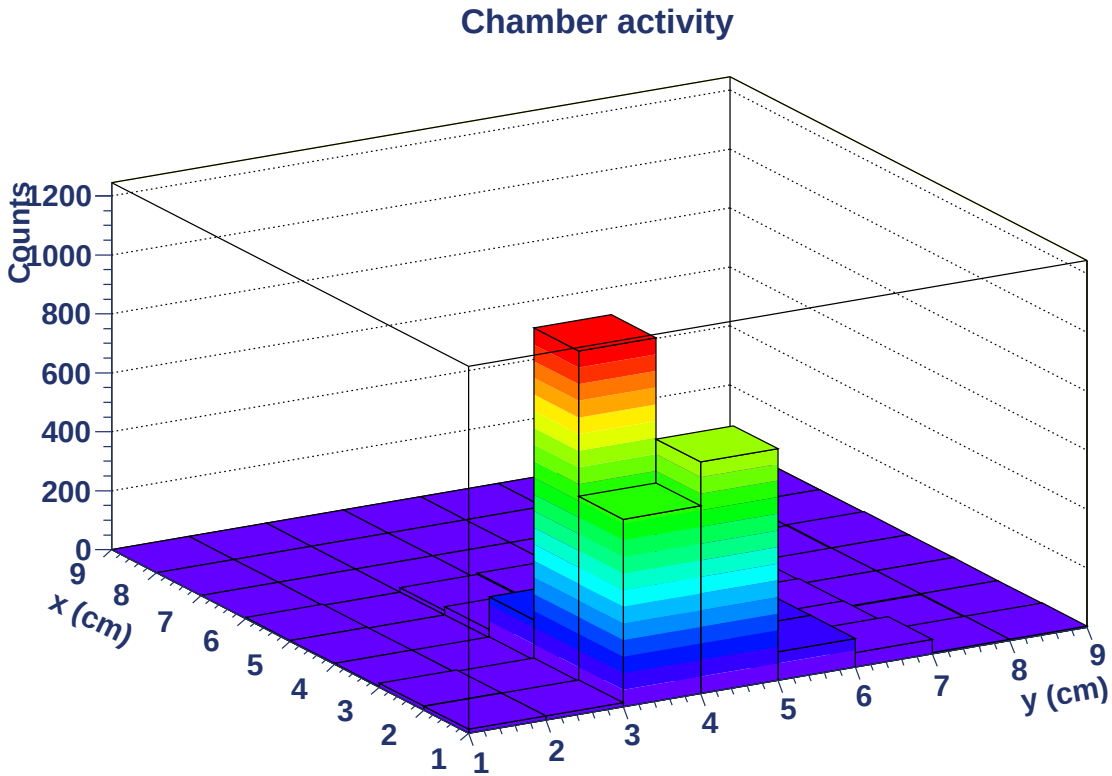
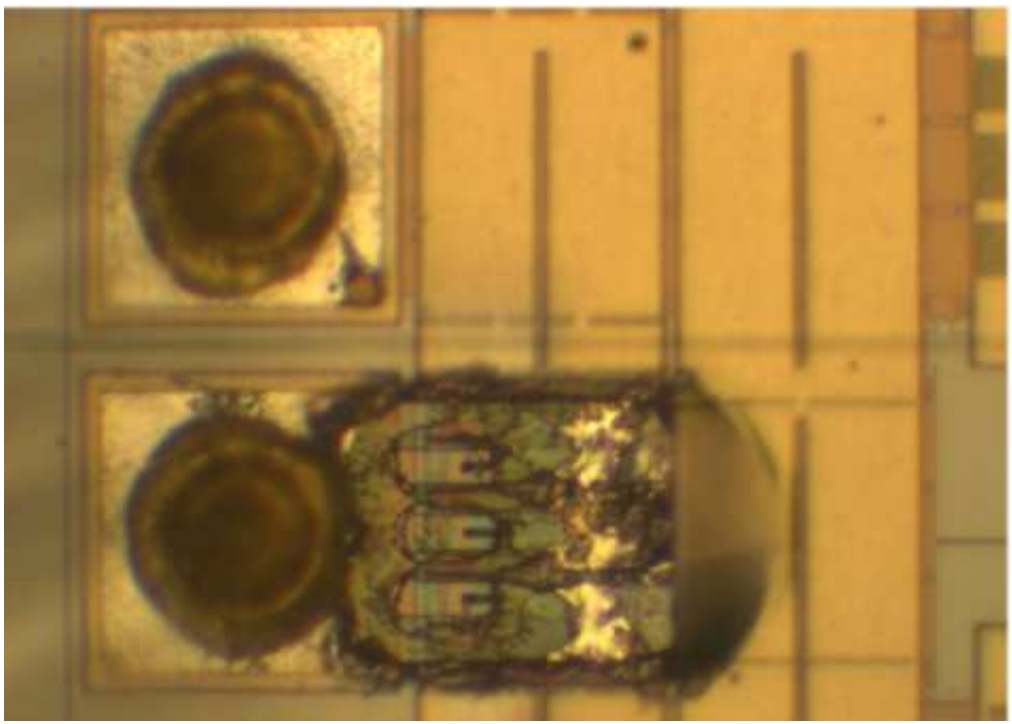


Spark protection

ESD pads without additional protection not sufficient!
Example @650 V):



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Further tests needed

Micromegas

- Response with a ^{55}Fe source;
- Efficiency with 3 detectors during futur testbeam.

RPC

4 boards are ready to equip a 8×32 cm^2 GRPC:

- Efficiency in cosmic bench with scintillator;
- Efficiency+multiplicity during november testbeam.

Improvements for DIRAC 2

- Internal trigger bug correction;
- Add trigger in/out capabilities;
- Add trigger masking feature (in slow control);
- Add internal test cicuitry;
- Add multiplexed analog readout (thanks to LPCC/IN2P3);
- Add 2 MicroMegas gain (in slow control);
- Minimum threshold reduction:
  - Lower offset discriminator;
  - Lower offset DC-servo loop;
- Add LVDS clock (thanks to LAL/IN2P3);
- Power supply pinout improvements and simplification;
- Decrease power consumption: preamplifier improved, but we'll be conservative for instance !

New foundry submission this autumn !

Thank you for your attention !