Muon Forward Tracker
a novel silicon detector for the ALICE upgrade

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for the ALICE MFT project

XIIth Quark Confinement and the Hadron Spectrum
September the 1st 2016
Thessaloniki, Greece
The ALICE experiment

The unique LHC experiment fully devoted to the study of QGP

Central region (ITS)

Muon Absorber

Muon Arm
The physics case

Complement to the present muon spectrometer with vertex capability

- In medium charmonium dynamics, dissociation/regeneration mechanism
  - Separation between prompt and decay $J/\psi$
  - Measurement of the $\psi(2S)$
  - Production yields and nuclear modification factors $R_{AA}$ down to $p_T = 0$
The physics case

Complement to the present muon spectrometer with vertex capability

• In medium charmonium dynamics, dissociation/regeneration mechanism
• Medium density and mass dependence of in-medium parton energy loss
  – Charm and beauty $p_T$-differential production yields
  – Charm in the single muon channel down to $p_T = 1$ GeV/c
The physics case

Complement to the present muon spectrometer with vertex capability

- In medium charmonium dynamics, dissociation/regeneration mechanism
- Medium density and mass dependence of in-medium parton energy loss
- QCD phase transition and its chiral nature
  - Measurement of QGP thermal radiation and spectral shape of low mass vector mesons

![Graphs showing dN/dM distributions for different mass ranges and production mechanisms.](image)
MFT design goals

• Vertexing for the Muon Spectrometer at forward rapidity
  – 5 detection disks of silicon pixel sensors $O(25 \, \mu m \times 25 \, \mu m)$
  – 0.6% of $X_0$ per disk
  – $-3.6 < \eta < -2.45$
  – Disk#0 at $z = -460 \, mm$, $R_{in} = 25 \, mm$ (limited by the beam-pipe radius)

• Good matching efficiency between MFT and MS
  – Disk#4 at $z = -768 \, mm$ (limited by FIT and the frontal absorber).

• Fast electronics read-out
  – Pb-Pb interaction rate $\sim 50 \, kHz$, pp interactions $\sim 200 \, kHz$. 
MFT Layout

920 silicon pixel sensors (0.4 m²) in 280 ladders of 2 to 5 sensors each.

- 10 half-disks
- 2 detection planes each

Radiation doses
< 400 krad
< 6x10¹² 1 MeV n_{eq}/cm²
10-fold security factor

-3.6 < \eta < -2.45

5% of the ITS surface
Twice the ITS inner barrel

\( z = -76.8 \text{ cm} \)
\( z = -46.0 \text{ cm} \)

IP region
MFT environment

Central region
MFT environment

MFT & FIT region
Joint ITS-MFT strategy

• Technical specifications of ITS inner-barrel and MFT are almost identical

• ITS-MFT common sensor:
  – same chip (participation to chip in-lab and in-beam tests)
  – similar flex printed circuit (same industrial process)
  – same interconnection technique (wire bonding)
  – same read-out architecture (common RU)
  – same cooling strategy (water cooling)
Brief history of the project

- 03/2011: Expression of Interest (EoI)
- 2011-2013: preliminary design studies
- 12/2013: Letter of Intent (LoI)
- 09/2015: Technical Design Report (TDR)
- 05/2015: funding finalized and approved
- 01/2016: Coordination Board composition updated
- 02/2016: Memorandum of Understanding (MoU)
- 06/2016: new Organization Breakdown Structure
- 08/2016: finalization of the ladder R&D
ITS-MFT sensor: ALPIDE

Pixel Sensor using TowerJazz 0.18µm CMOS Imaging Process

- High-resistivity (> 1 kΩ cm) p-type epitaxial layer (25 µm) on p-type substrate
- Very small n-well diode (2 µm diameter), low capacitance
- Application of reverse bias voltage to substrate to increase depletion zone
- Deep p-well shields n-well to allow full circuitry within active area
- Total chip thickness: 50 µm
ITS-MFT sensor: ALPIDE

Chip performances: pALPIDE3

- Proto pALPIDE3 (8 sectors with different pixel characteristics)
- **Efficiency and fake rate within specifications**
- Degradation due to irradiation fully compensated by applying back bias
- Positive EDR end of 2015; ALPIDE pre-production in progress
MFT ladder

From ALPIDE chip to Hybrid Integrated Circuit (HIC)

- Chips are interconnected to a Aluminum Flexible Printed Circuit (FPC)

- FPC design almost final (optimization according to the interconnection technique)
MFT ladder

From ALPIDE chip to Hybrid Integrated Circuit (HIC)

- Main baseline (ITS-TDR): laser soldering
- Abandoned on February 2016: yield < 95%
- Alternative solutions:
  - **New baseline**: wire bonding
  - Alternative: conductive glue
MFT ladder

From ALPIDE chip to Hybrid Integrated Circuit (HIC)

- Several tests realized with conductive glue
- Test with wire bonding ongoing
- Automatic positioning of chips on FPC: Module Assembly Machine (MAM)
MFT ladder

From HIC to ladder: the encapsulation

• Main goals
  – Allow ladder removal without dispersing Si pieces
  – Allow ladder gluing on disk
  – Provide electrical insulation between ladders and disk

• Encapsulation technique
  – Gluing adhesive Kapton (K104 Saint Gobin) on the sensor side of the HIC
  – Total encapsulation thickness (Kapton+glue): 37µm
  – Kapton thermal conduction: 0.16 W/mK

• Process definition almost finalized

• Creation of grey room at CEA Antenna

Ladder EDR: end of September
MFT disk

From ladder to disks: half disks overview

Half-Disk #0-#1
24 ladders
66 sensors

Half-Disk #3
32 ladders
114 sensors

Half-Disk #2
26 ladders
82 sensors

Half-Disk #4
34 ladders
132 sensors
**MFT disk**

**Half disk structure**

- Two detection planes
  - Coverage around the beam pipe
  - Water cooled plate in between
  - Redundancy (50%)

- PCB: signal/voltage routing
  - DC-DC converters (disk 3 and 4)

- Heat Exchanger
  - Rohacell + cold plates
  - Cold plate: assembly of carbon papers with embedded polymide water pipes (Ø 1 mm)
  - Manifold

- Disk support (Peek material)
MFT disk

Disk Exchanger R&D

- Study and optimization of C-fiber stacking
  - Comparison between 5-layer carbon fibers
  - Optimization of ply orientation
- Ladder thermal tests
  - Validation of mockup thermal behavior
  - Validation of the simulation parameters

- Cold plate prototypes
  - K13D2U material (high conductivity) made at CERN
  - MJ55 material (lower conductivity) made at Subatech (Nantes)
  - Feasibility of production in India
MFT disk

Disk assembly

• Ladders are glued on heat exchanger
  – Dedicated positioning tool

• Choice of the glue
  – Silicon (SE4445) for easier removal and longer working time
  – Used in ATLAS experiment (radiation hard)

• Ongoing R&D on automatic glue deposition
  – Automatic machine (IPN Lyon)
  – Deposition pattern: curved spiral

• Survey of chips position on 3D machine
MFT cone

Global layout of half MFT

- 5 half disks
- Power Supply Unit
- Mother Boards
- Cone structure
MFT Barrel

Integration scheme

TPC

Gutter

Gutter Insertion rails

Final position

Gutters slide in as the MFT is inserted

Gutters out position

Readout bundles

MFT cage
MFT readout

On-Detector

- Between 132-264 high speed data signals (1.2 Gb/s) per disk
- Between 96-136 clock and slow control signals per disk
- Total of 1480 twinax cables for read-out
- 80 concentrator boards (RU) ~ 4 m away, where TID about ~ 1 krad

Off-Detector

Barrel Patch Panel

• Between 132-264 high speed data signals (1.2 Gb/s) per disk
• Between 96-136 clock and slow control signals per disk
• Total of 1480 twinax cables for read-out
• 80 concentrator boards (RU) ~ 4 m away, where TID about ~ 1 krad
## Milestones

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- **Sensor (common with ITS)**
- **Ladder**
- **Disk**
- **Cone**
- **Barrel**

- **Commissioning and final installation**
Conclusions

- MFT: an innovative silicon tracker for the ALICE upgrade
- Precision tracking in the muon spectrometer acceptance
  - Vertexing capabilities
  - Muon matching
- Major improvement on several physics cases:
  - Open heavy flavours
  - Charmonia
  - Low mass mesons
- MFT collaboration: 16 groups for 8 countries.
- Project in its final R&D phase
- Chip production starting soon, the rest will follow
- Installation in ALICE cavern foreseen during first semester of 2020
Backup material
MFT design goals

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![Graph showing $\sigma_X$ vs. $p_T$](image1.png)

![Graph showing Efficiency vs. $p_T$](image2.png)
MFT design goals

- Vertexing for the Muon Spectrometer at forward rapidity
- Good matching efficiency between MFT and MS
  - Disk#4 at z = -768 mm (limited by FIT and the frontal absorber)
ITS-MFT sensor: ALPIDE

Chip architecture

- Matrix of pixels (29.24 µm x 26.88 µm) + peripheral bias/readout/control/interface
- Matrix zero-suppressed readout via Priority Encoders sent to 11b ADC
- Differential signal transmitted at 1.2 Gb/s
- Power consumption density: 35 mW/cm²
MFT Barrel

Global layout of half barrel

- Barrel function: MFT insertion and positioning
- Full scale mock-up built for integration studies
MFT Services

- LV architecture: provide analog, digital and back bias power
- Cooling plant: water cooling of disks and RU
- DCS architecture: standard setup and monitoring of operation conditions