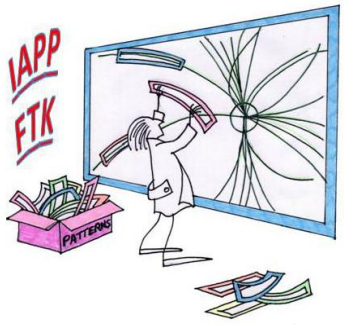
FTK: the hardware Fast TracKer of the ATLAS experiment at CERN

Yannis Maznas (A.U.Th.)

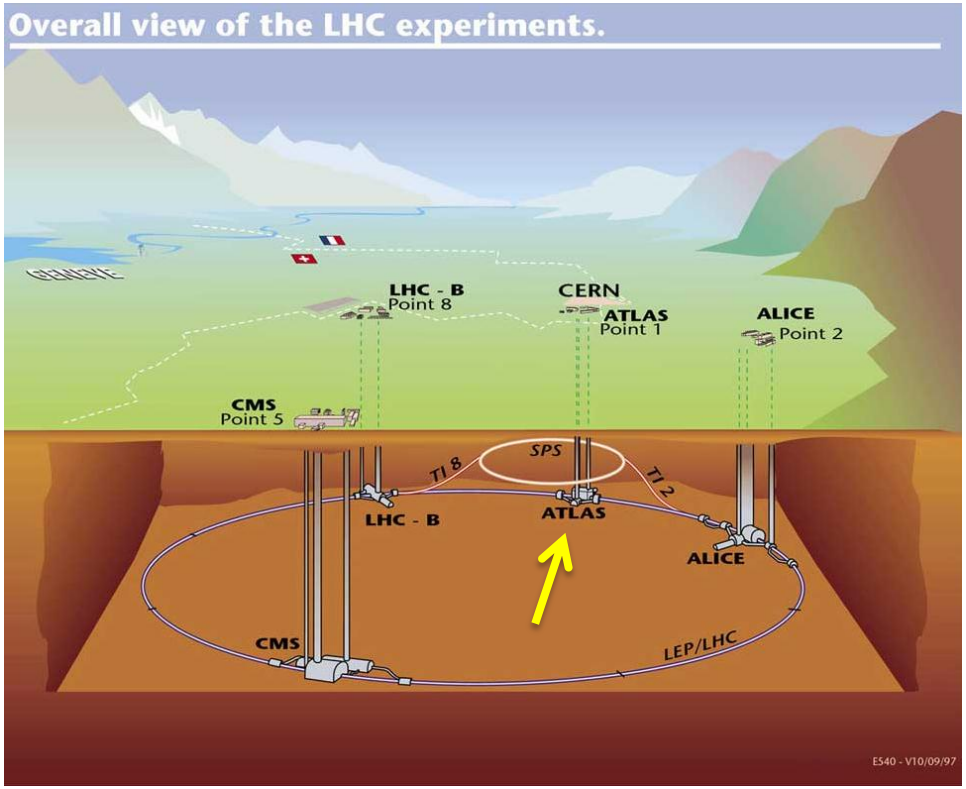
on behalf of the ATLAS Collaboration



FP7-PEOPLE-2012-IAPP
Grant No: 324318

ATLAS at CERN

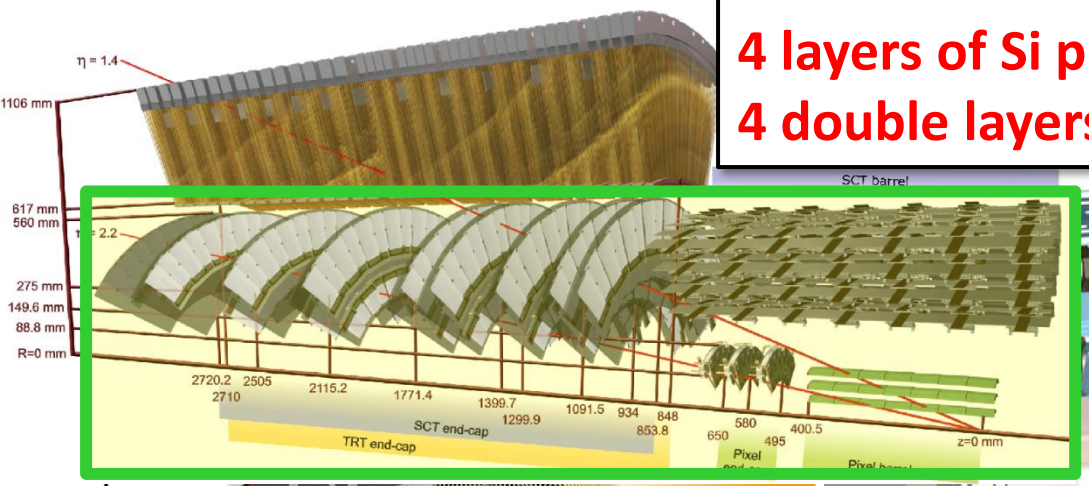
- Peak delivered luminosity for pp collisions in 2016 to ATLAS up to now is $11.6 \cdot 10^{-6}\, fb^{-1}s^{-1}$ and in total $22.7 fb^{-1}$ recorded data.
  - Peak delivered luminosity in 2016 is already above the instantaneous luminosity that ATLAS and CMS designed their trigger systems to cope with
- Integrated luminosity goal for Run 2 (2015-2018) is $100 fb^{-1}$ of good data for ATLAS and CMS

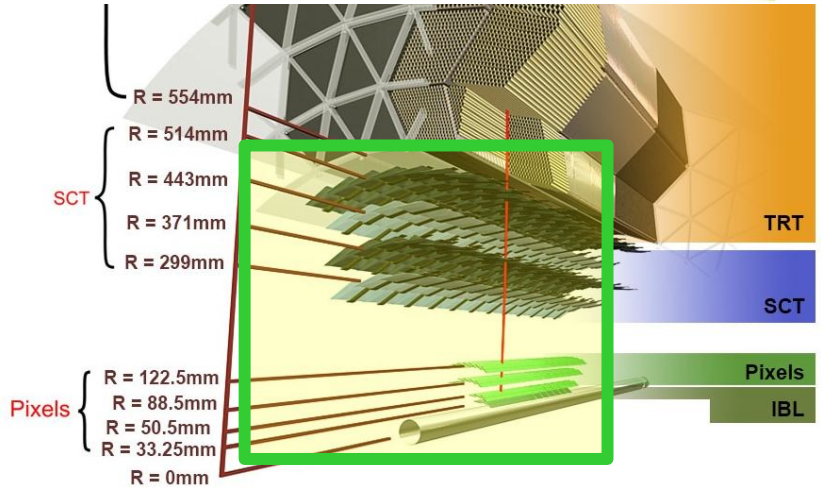


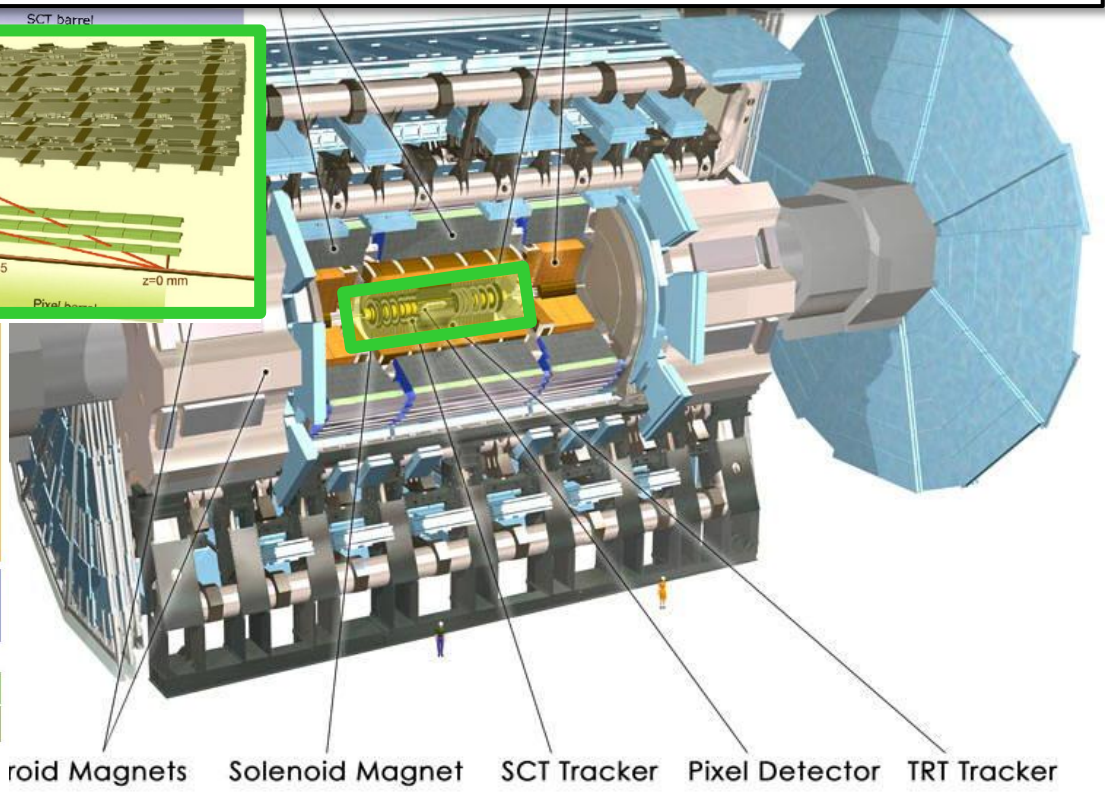
Too much load for the detector front ends to handle without serious sacrifices.

ATLAS Inner Detector

FTK uses 12 layers of the ATLAS Inner detector:
4 layers of Si pixel and
4 double layers of Si strips (2x4)

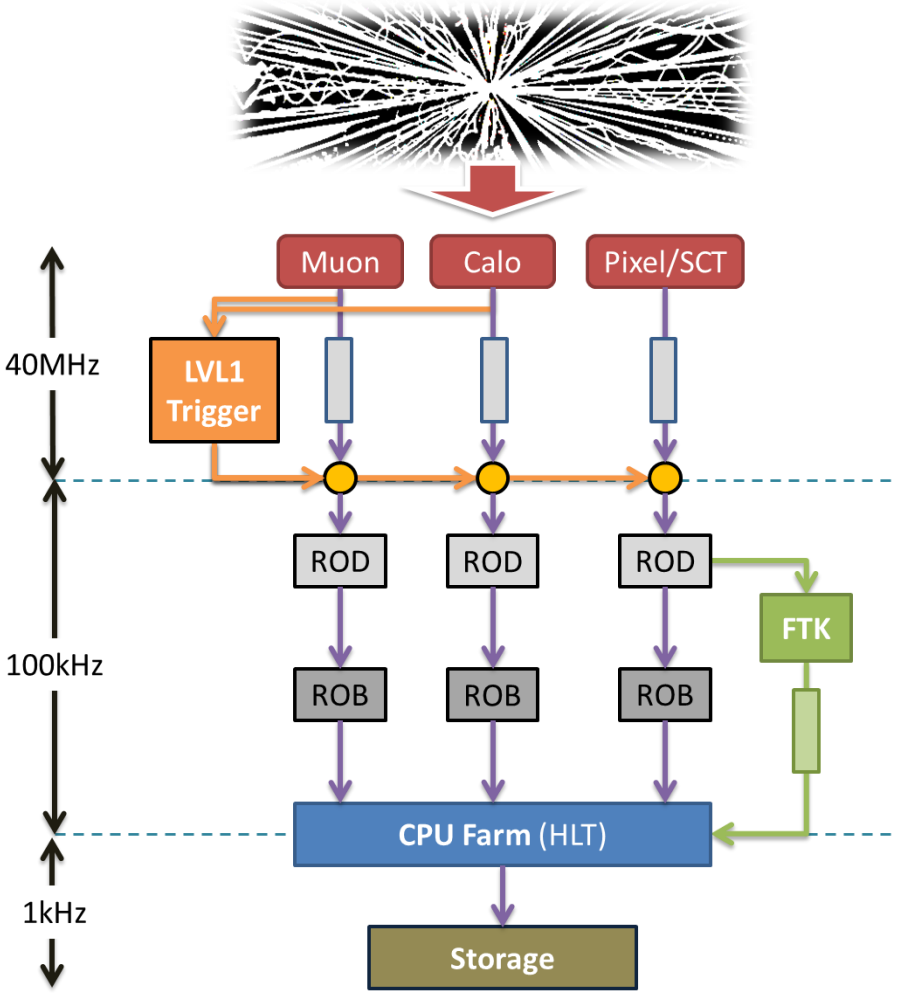




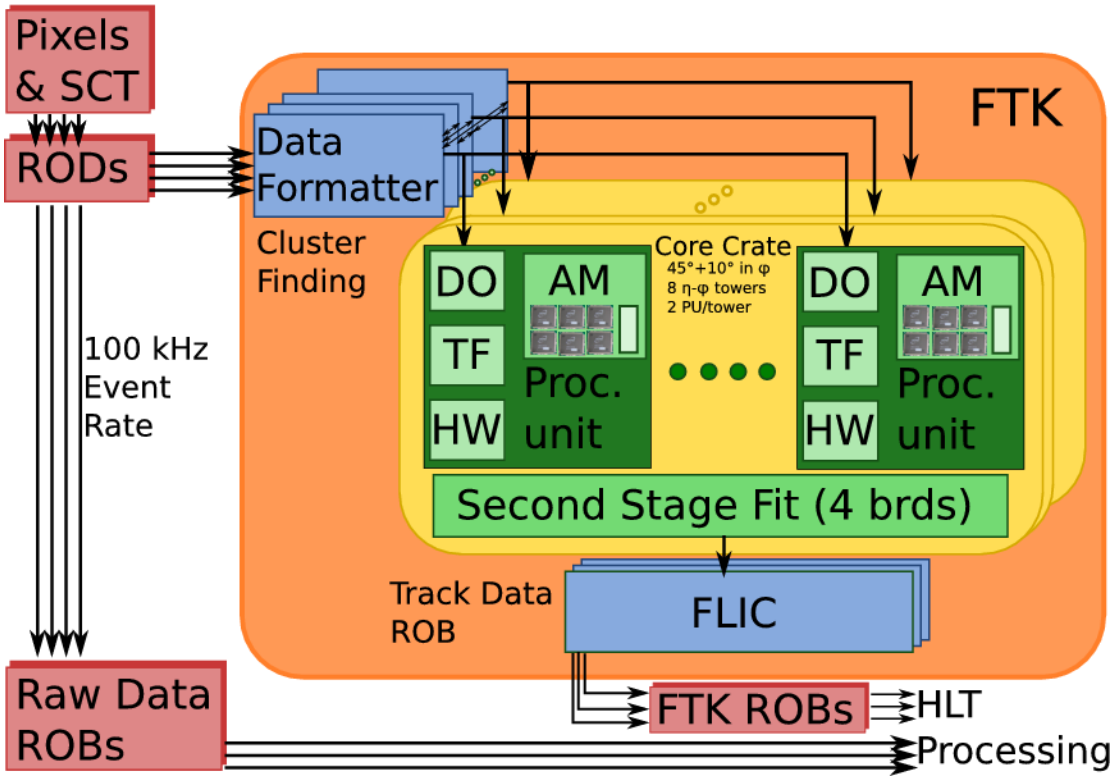


Fast Tracker (FTK) in ATLAS Trigger System

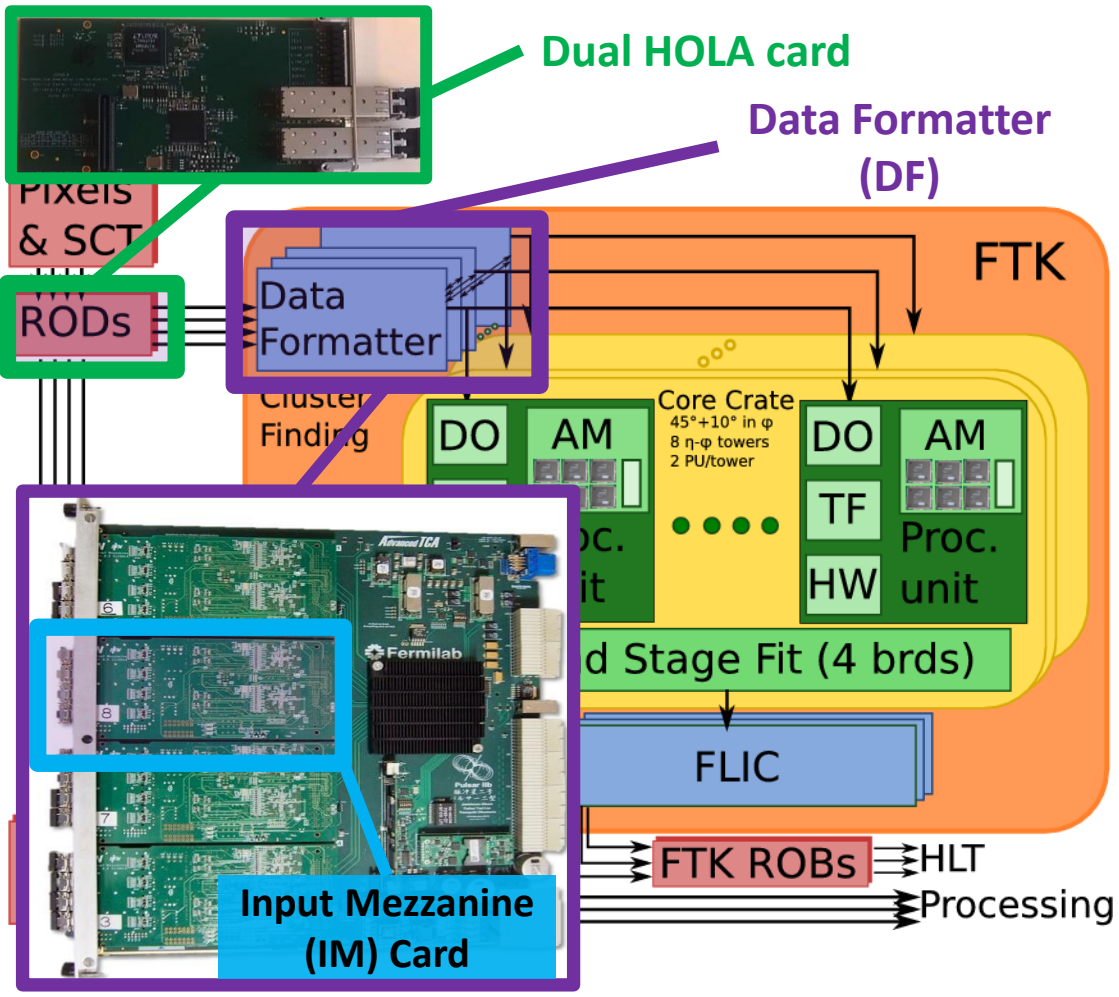
- FTK is a similar architecture to the CDF Silicon Vertex Trigger (SVT) project.
  - It will have the difficult task to handle level1 accepted events **(~100M channels from silicon detector) at 100kHz**
- For each L1 accepted event it will fit tracks for particles with $P_T > 1GeV$.
- It will provide these tracks and associated hits to the HLT : **full resolution information (pT, d0, z0, eta, phi) from all 12 layers of the silicon detector.**
- Thus, the HLT will have the time to enhance/enrich its reconstructing algorithms.



FTK Design and its Boards



FTK Design and its Boards

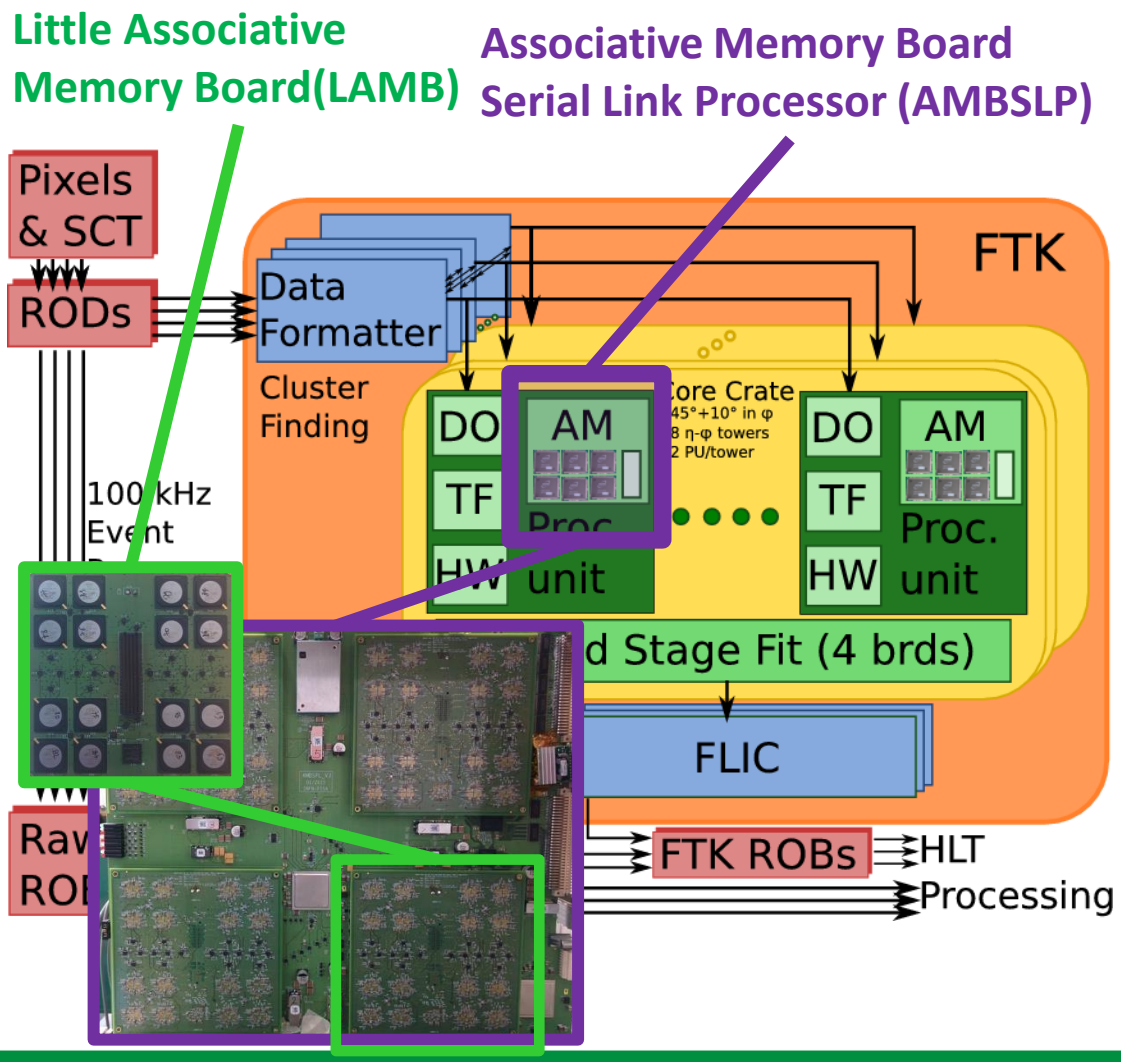


FTK divides ATLAS in to 64 η-φ towers (8 regions)

Main steps:

1) **IM** receives the hits and does the grouping. **DF** re-maps the hits from the readout chain into projective towers.

FTK Design and its Boards



FTK divides ATLAS in to 64 η-φ towers (8 regions)

Main steps:

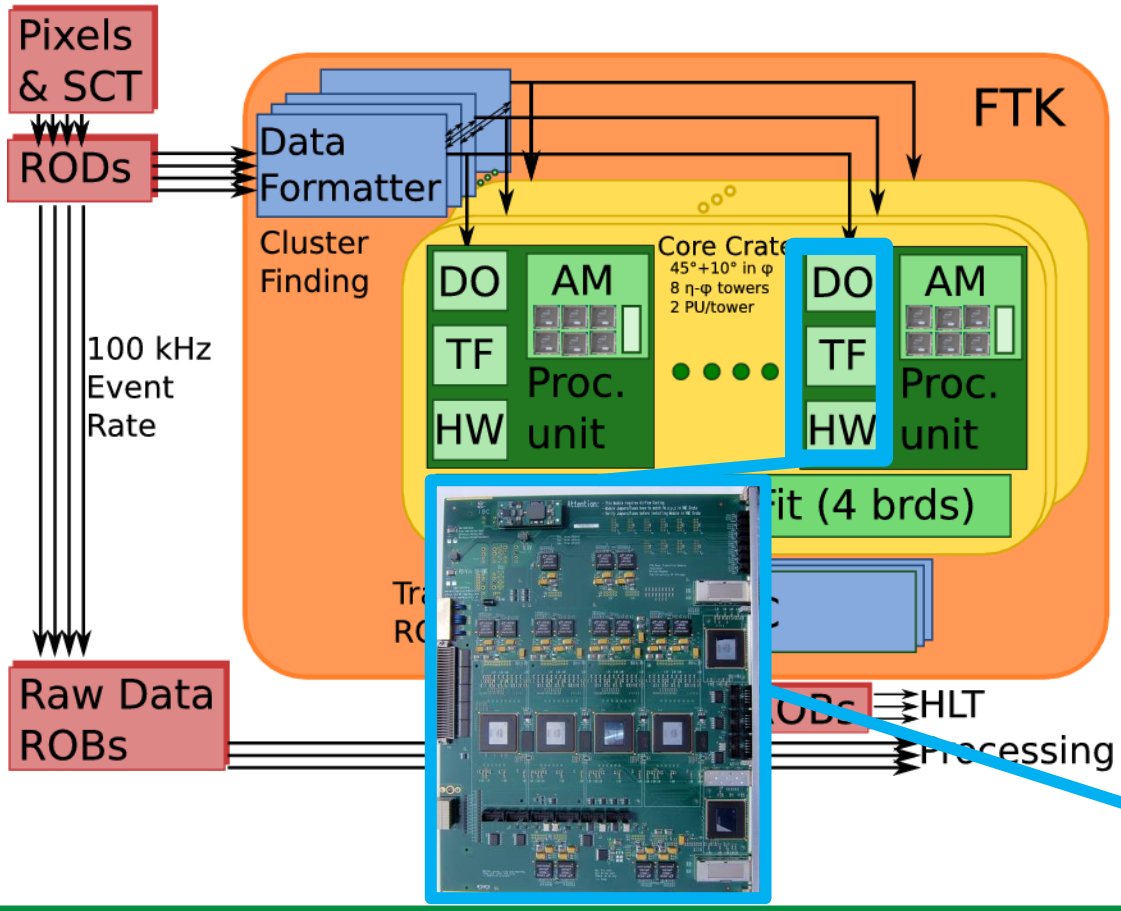
1) IM receives the hits and does the grouping. DF re-maps the hits from the readout chain into projective towers.
2) AM chips (LAMB) perform pattern matching on the hits received (low resolution track fitting)

FTK Design and its Boards

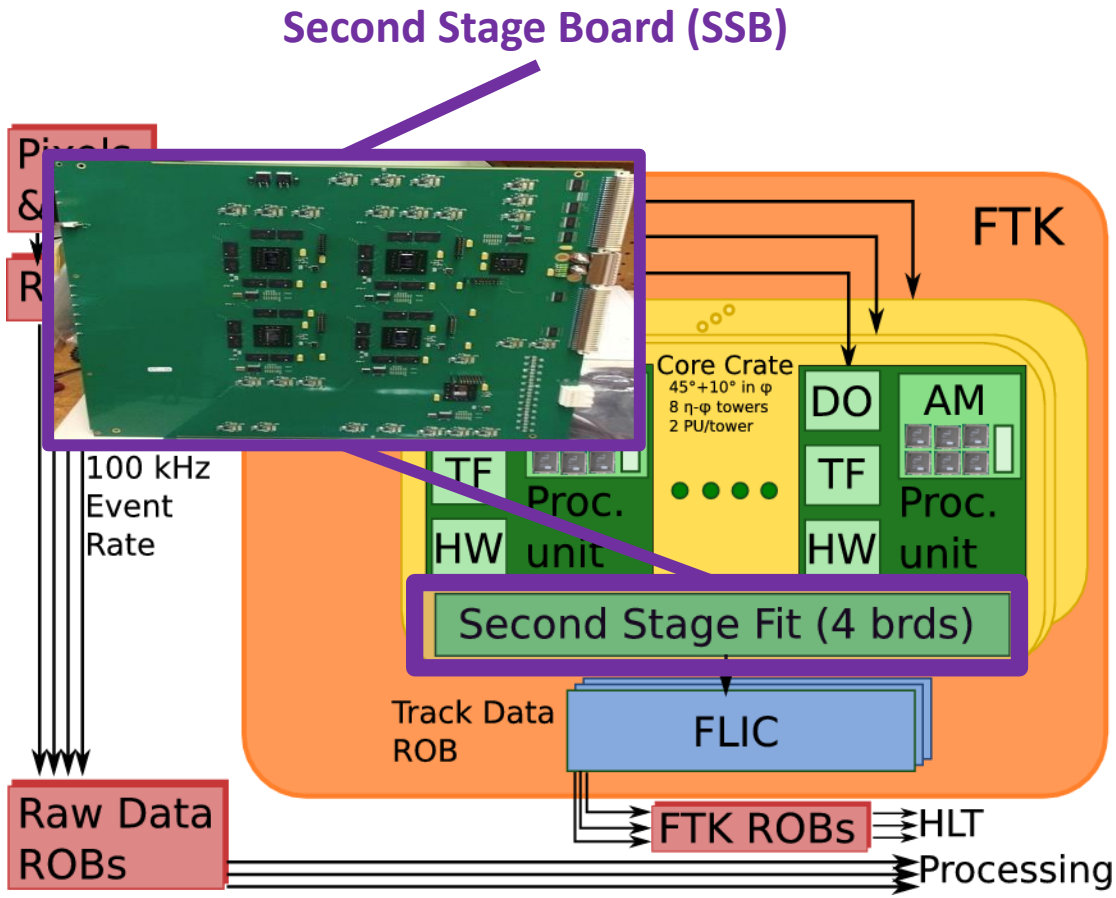
FTK divides ATLAS in to 64 η-φ towers (8 regions)

Main steps:

1) IM receives the hits and does the grouping. DF re-maps the hits from the readout chain into projective towers.
2) AM chips (LAMB) perform pattern matching on the hits received (low resolution track fitting)
3) **AUX** performs full resolution track fitting on the matched patterns and removes fake tracks by χ^2



FTK Design and its Boards

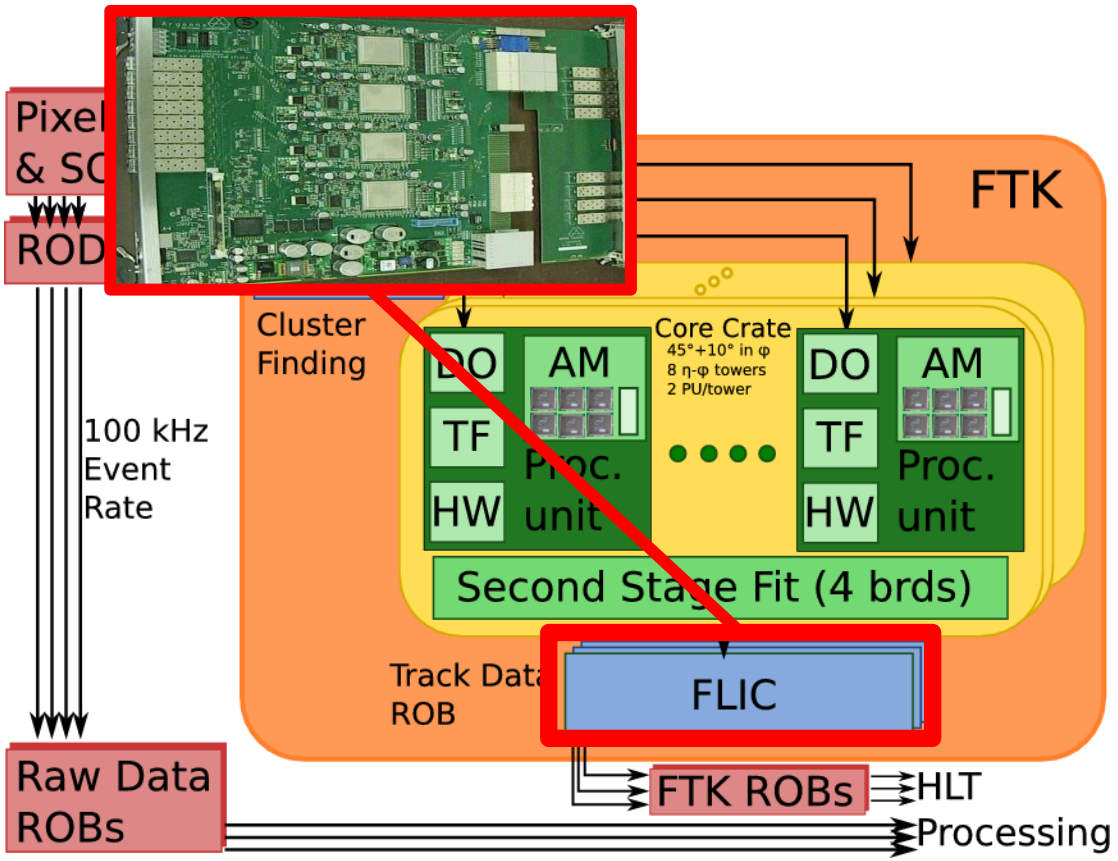


FTK divides ATLAS in to 64 η-φ towers (8 regions)

Main steps:

1) IM receives the hits and does the grouping. DF re-maps the hits from the readout chain into projective towers.
2) AM chips (LAMB) perform pattern matching on the hits received (low resolution track fitting)
3) AUX performs full resolution track fitting on the matched patterns and removes fake tracks by χ^2
4) **SSB** uses the remaining strip layers to remove fake tracks and computes track parameters

FTK Design and its Boards



FTK divides ATLAS in to 64 η-φ towers (8 regions)

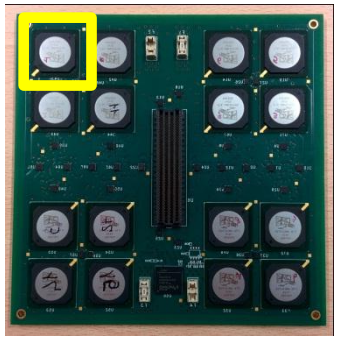
Main steps:

1) IM receives the hits and does the grouping. DF re-maps the hits from the readout chain into projective towers.
2) AM chips (LAMB) perform pattern matching on the hits received (low resolution track fitting)
3) AUX performs full resolution track fitting on the matched patterns and removes fake tracks by χ^2
4) SSB uses the remaining strip layers to remove fake tracks and computes track parameters
5) The FLIC formats the FTK output record into the ATLAS standard and maps the track hits from the tower to ATLAS global coordinates.

Associative Memory (AM) Chip

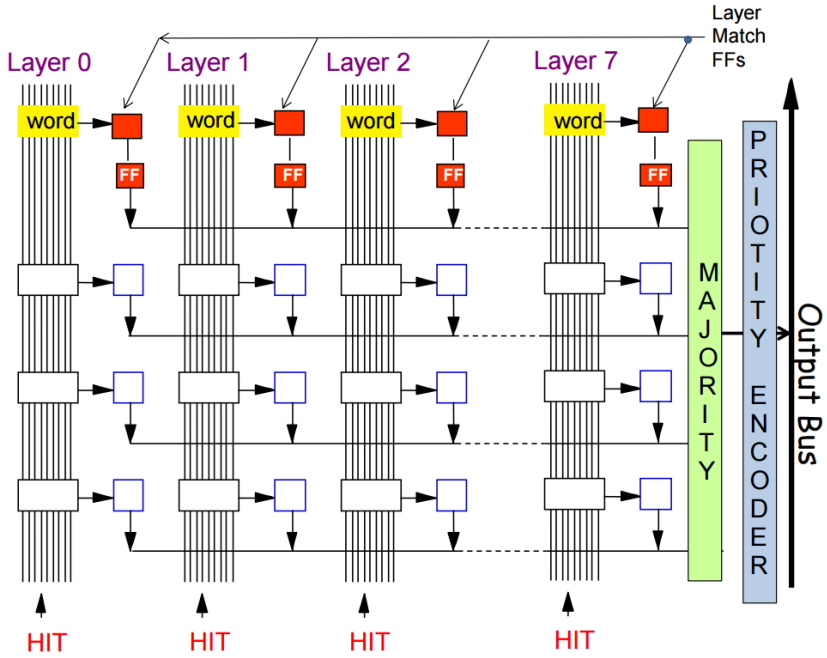
Random Access Memory (RAM):
Designed to return the value of a specific memory address.

Content-Addressable Memory (CAM):
Designed to search for a value in the entire memory in a single operation.



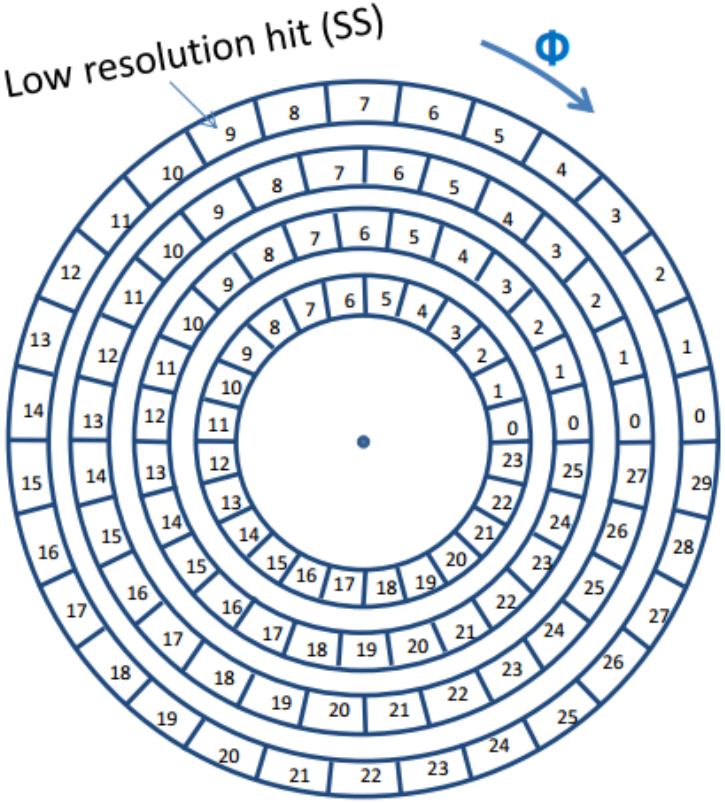
AM chip is a **CAM** (custom designed ASIC)

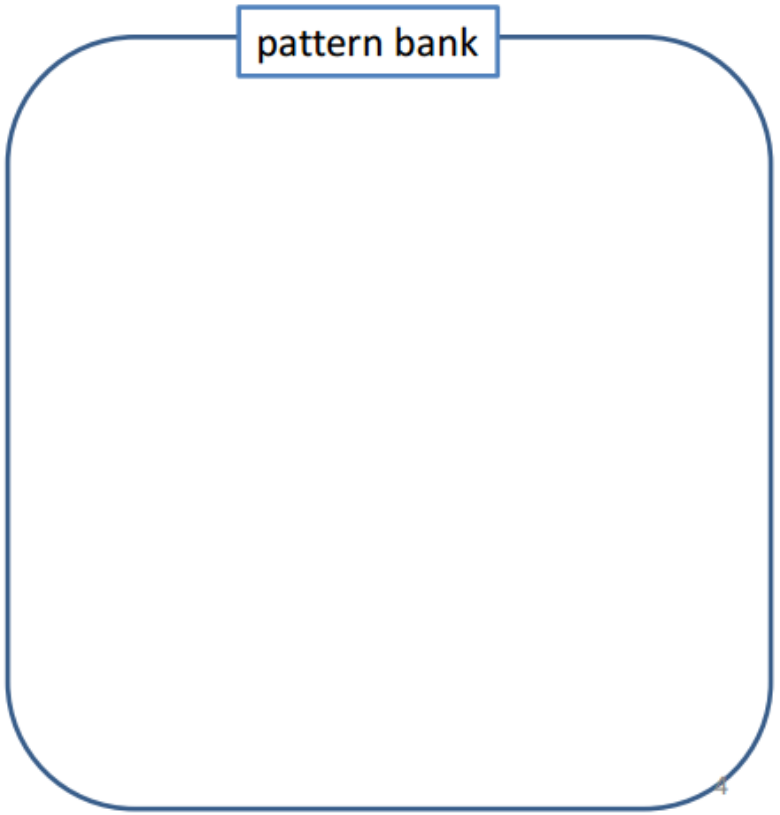
- AM06 (currently used) can contain 128k patterns. AM05… ~2k patterns
- In total 8192 AM chips for FTK
- ~ 3Watt power consumption each



FTK key feature: Pattern Matching

This process uses grouped pixel hits called **Super Strips** (SS) and not full resolution of the tracker

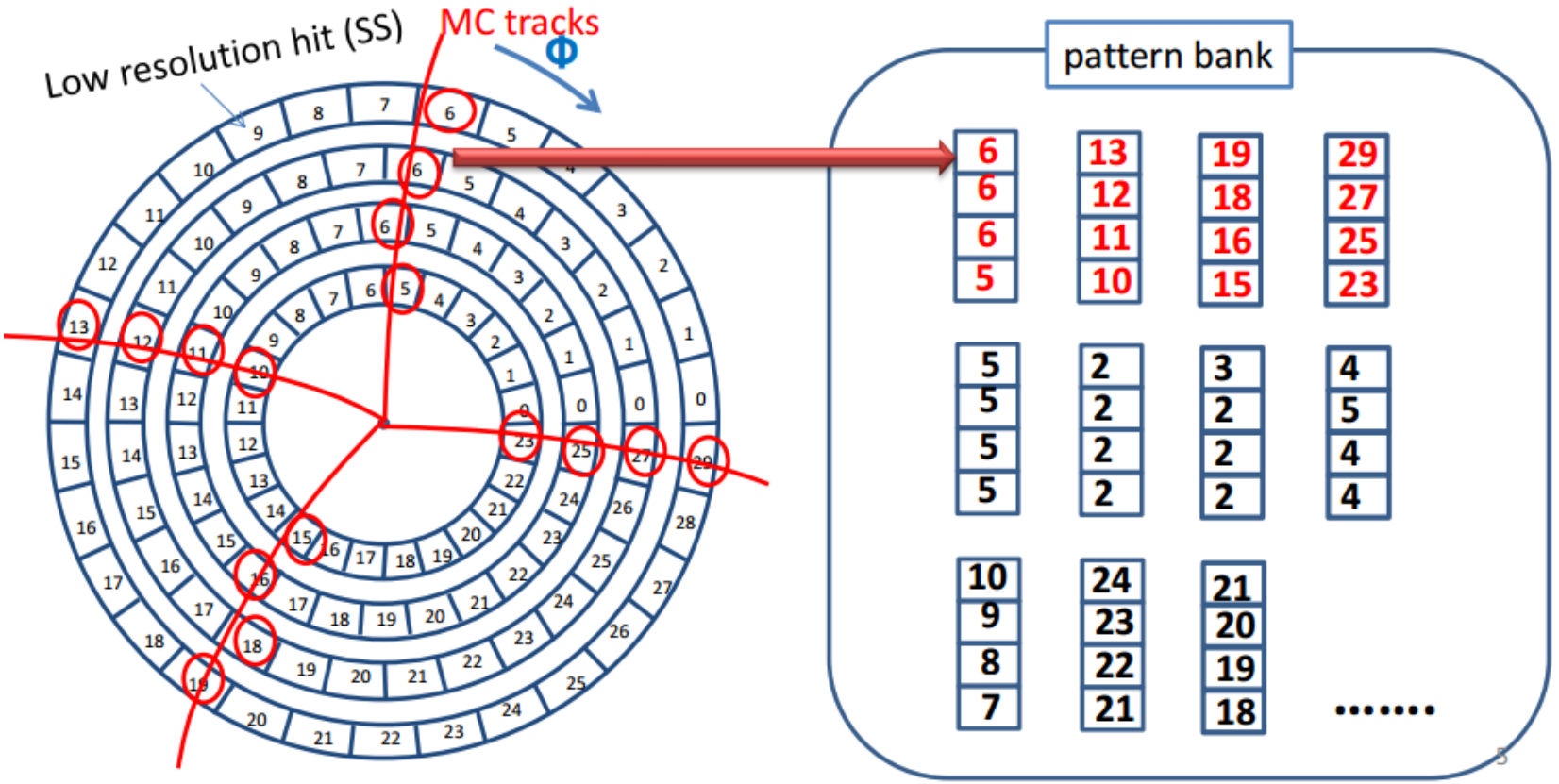




FTK key feature: Pattern Matching

Find low resolution track called "pattern".

1. Generate all possible patterns using **MC simulation** using 8 out of 12 layers mentioned earlier. More than 50 billion tracks are used for pattern generation.

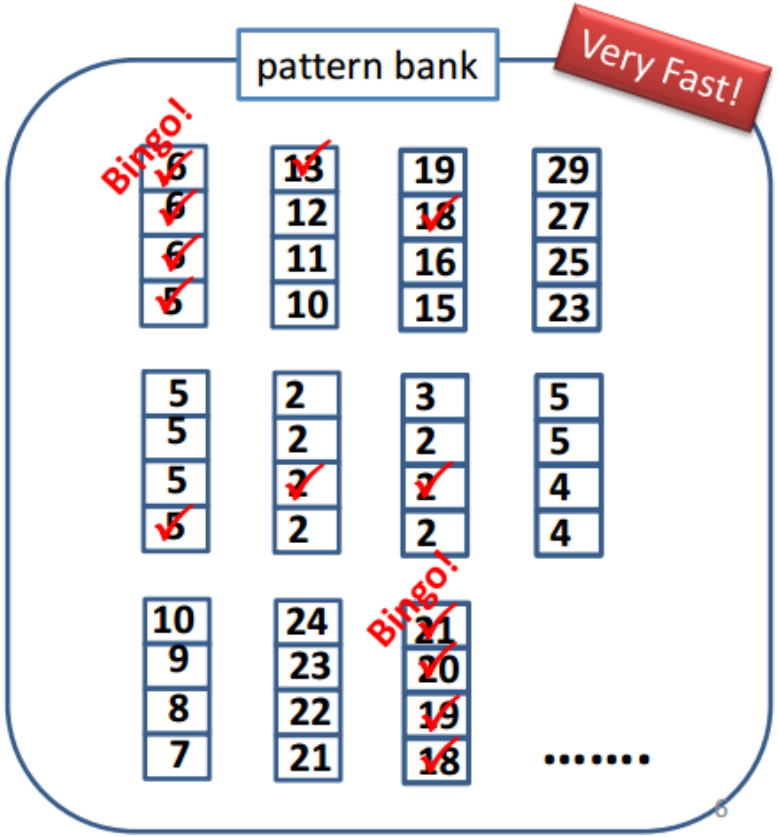


FTK key feature: Pattern Matching

Find low resolution track called as "pattern".

2. Match the pattern in real data using **pattern recognition**

   For real data, detector hits sent to pattern bank sequentially, and patterns are recognized like a bingo game. All patterns are matched when all hits have arrived.



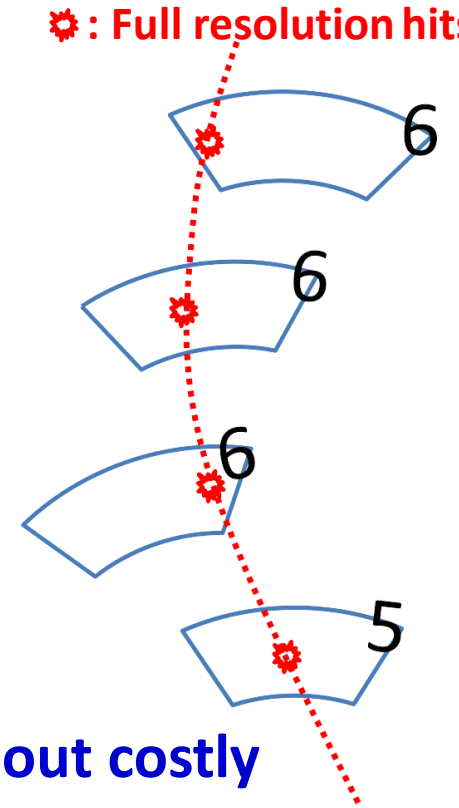
FTK Track Fitting

Estimate track parameters using full resolution hit information in a linearized fit approximation.

5 parameters
d0, z0, eta, phi, P_T

1. Pre-Calculate the constants for the 5 parameter's **linear approximation** as a function of hit coordinates using MC simulation.
2. Estimate the track parameters using linear **approximation** equation with pre-calculated constants and **full resolution** hit coordinate.

$$\tilde{p_i} = \sum_{l=1}^{N} C_{il} x_l + q_i$$



Parameters

$\tilde{p_i}$: Track Parameters (i=0-4)

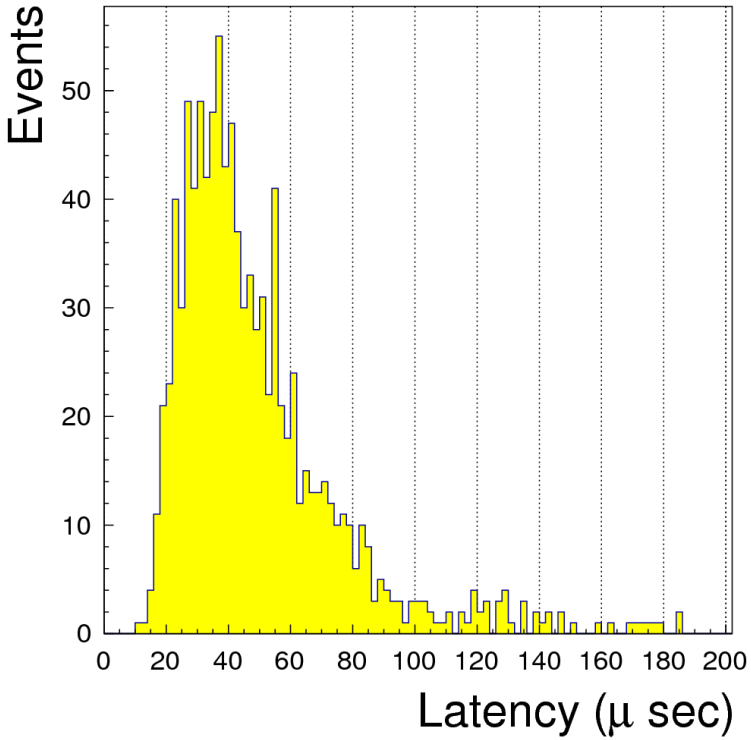
x_i : Hit Coordinate

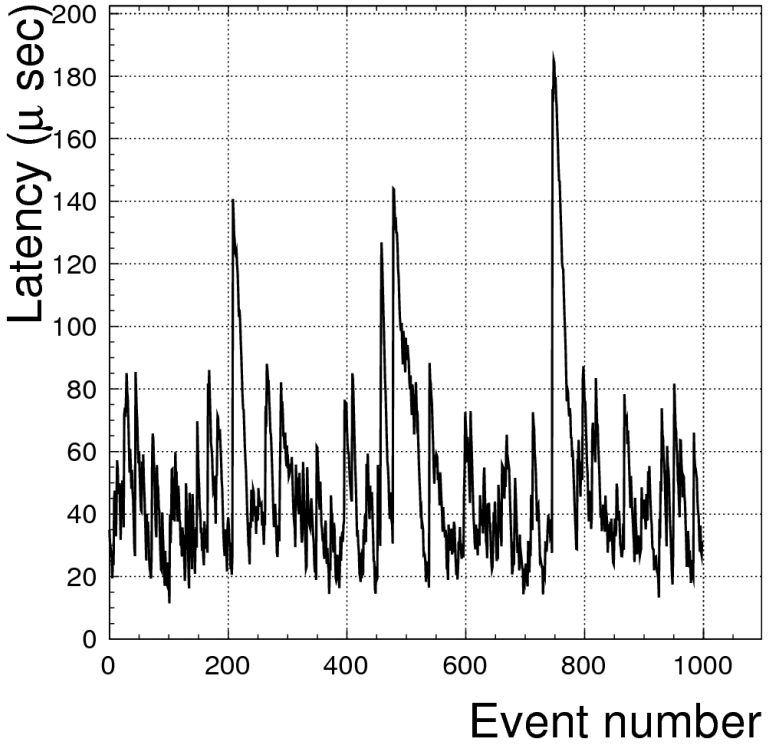
$\vec{C}_i$ q_i : Constant

FTK estimates track information very quickly without costly looping in minimization.

FTK Latency

- Average latency of the system is $50\mu sec$
- At high occupancy it can rise up to some hundreds of μsec but it still meets HLT requirements

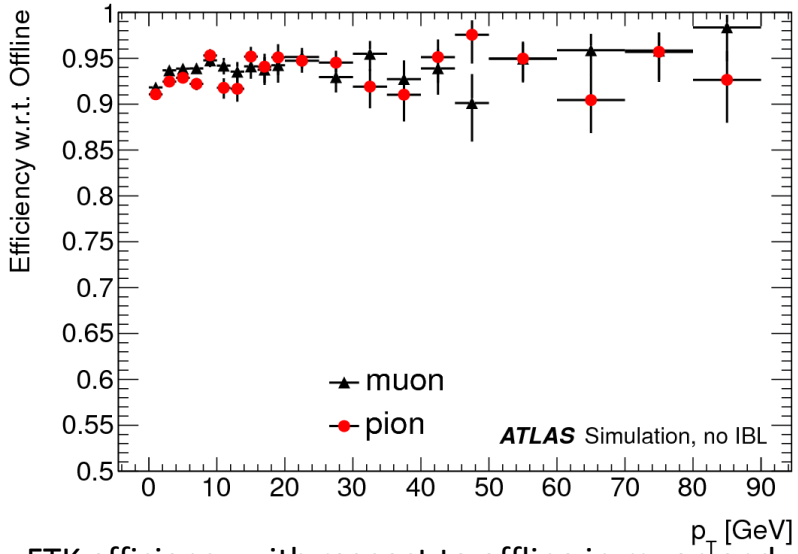




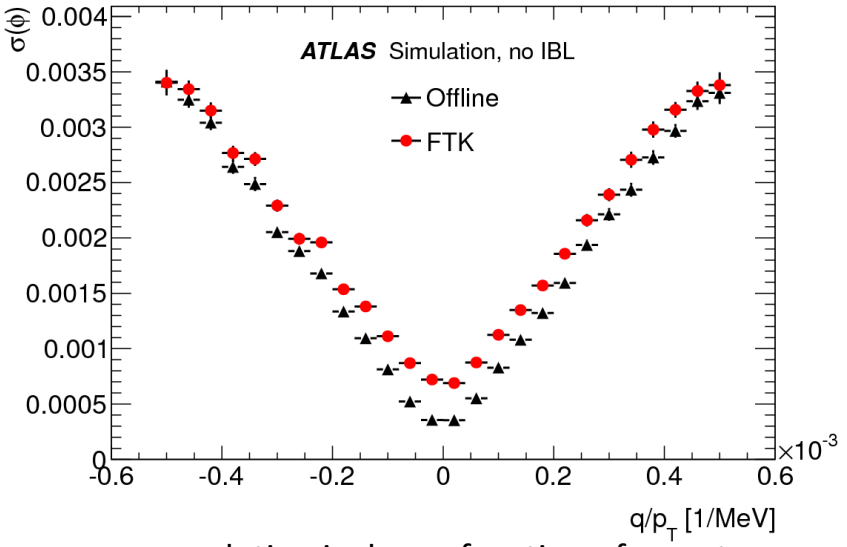
** As presented in the [Fast TracKer Technical Design Report]

FTK Tracking Performance

- High single track efficiency compared to offline tracking (>90%)
  - Efficiency depends on the size of the pattern bank.
- Different logic from offline tracking algorithms:
  - Simple hit clustering
  - Linear tracking approximation
  - No use of TRT
- No patterns trained for $\mathrm{pT} < 1GeV$

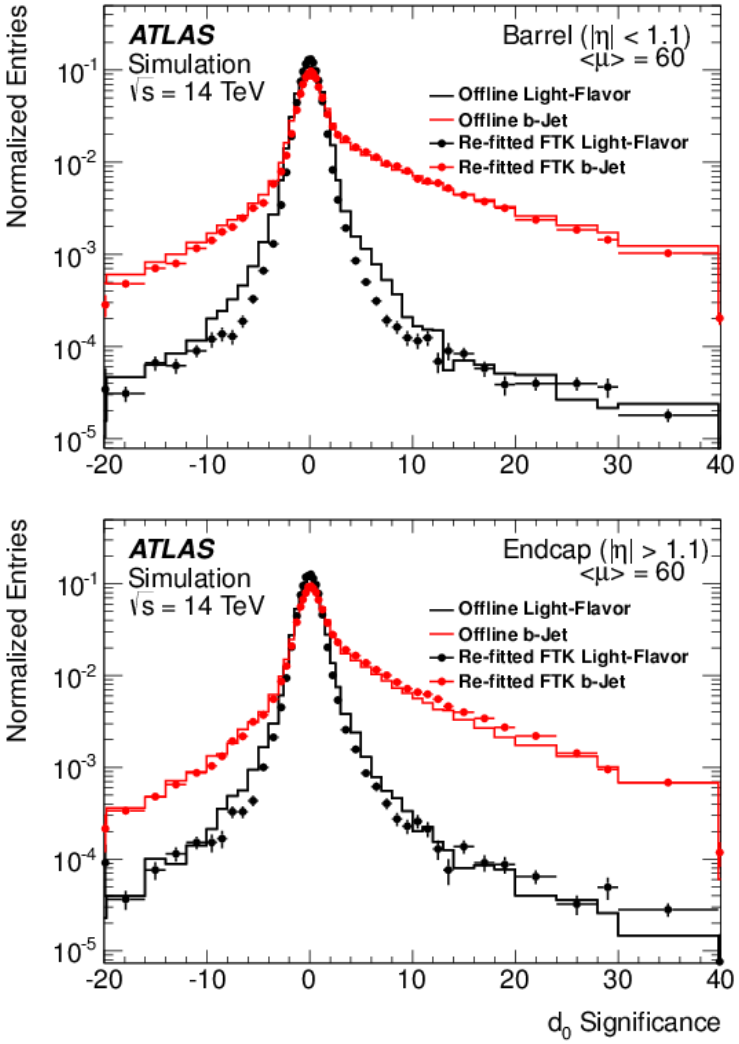


FTK efficiency with respect to offline in muon and pion samples versus p_T

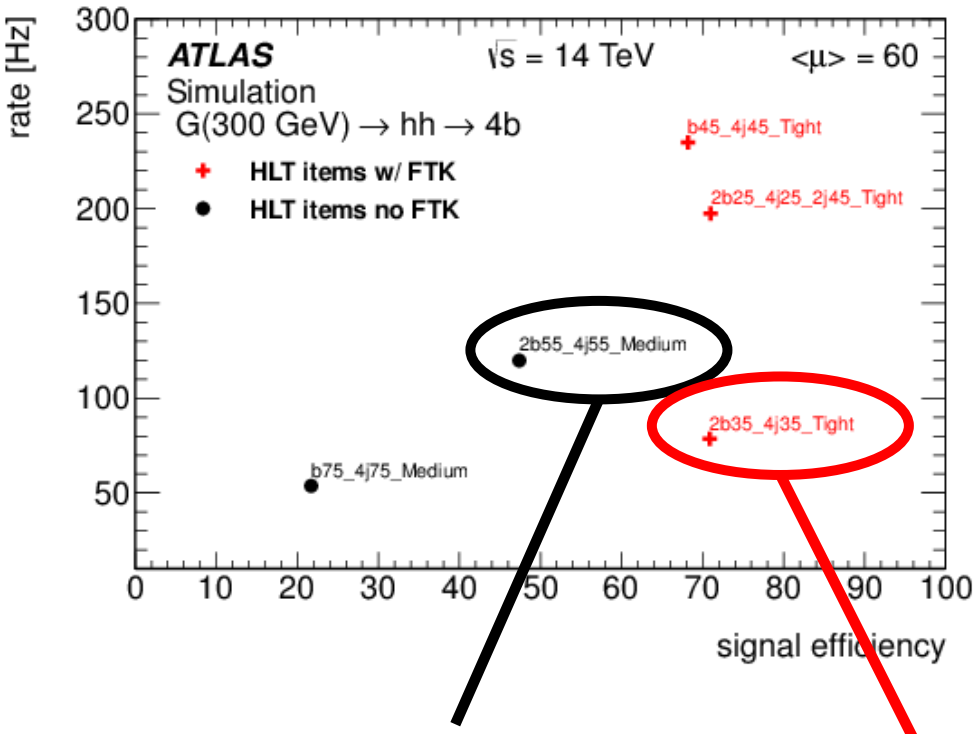


muon resolution in ϕ as a function of curvature

Advantage in b-jet triggering



FTK allows b-jet algorithms to be run with looser HLT jet pT thresholds.



55 GeV Medium 2b-tag with 55 GeV 4th jet

35 GeV Tight 2b-tag with **35 GeV** 4th jet

Commissioning at CERN

2013 2014 2015 2016 2017

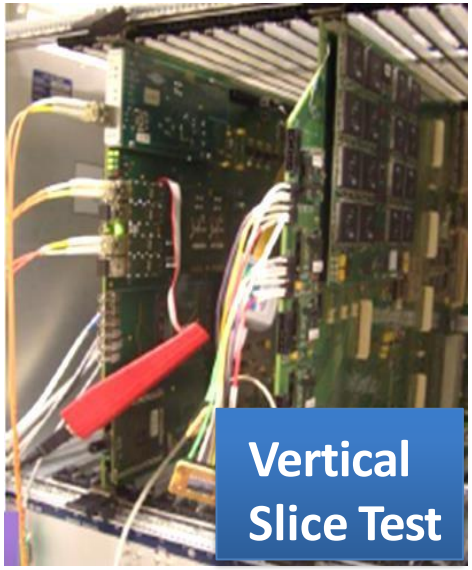
Test room integration

Boards get moved to ATLAS once stable data flow is achieved.

Start operation in limited region

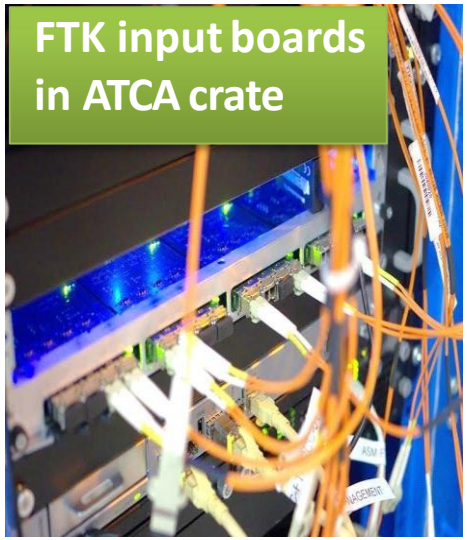
Vertical Slice Test (VS Test)

Only SCT, test inputs with simulated 70 kHz L1 data



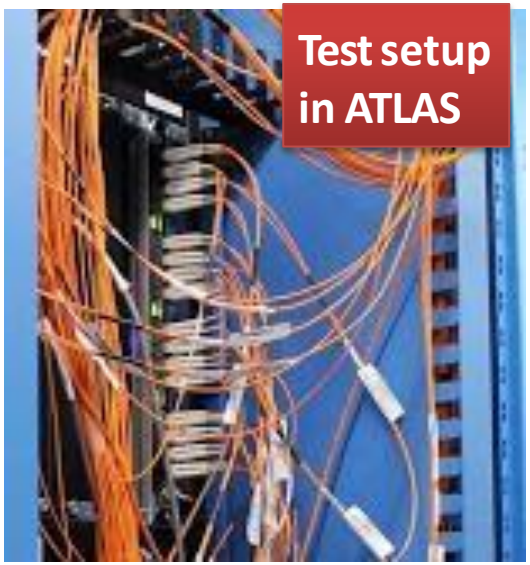
Global Integration Test

SCT and Pixel, real inputs with Cosmic or test data with maximum 100 kHz Test trigger.



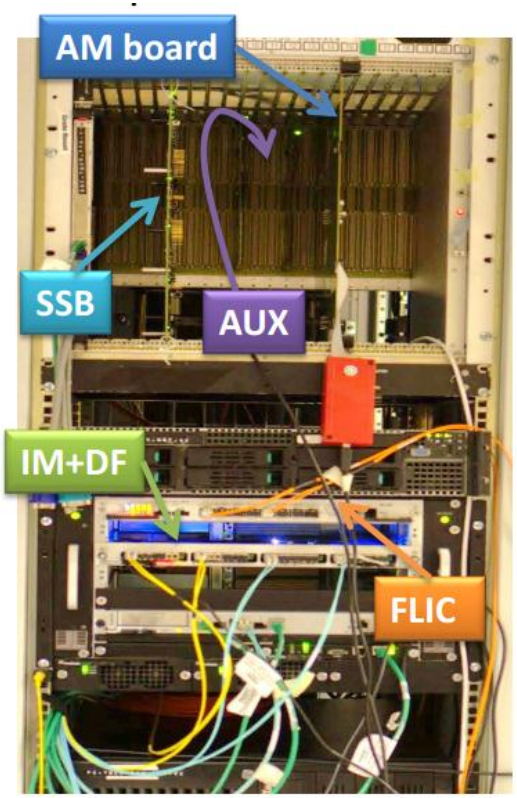
Commissioning in ATLAS

SCT, Pixel and IBL with Real pp and HI Collision data with ~ 50 kHz



Current Commissioning Status

- Data flow tests are ongoing both on test stands and in ATLAS
- Operational experience keeps leading to firmware optimization



An all-boards test

Installed DF and IM boards

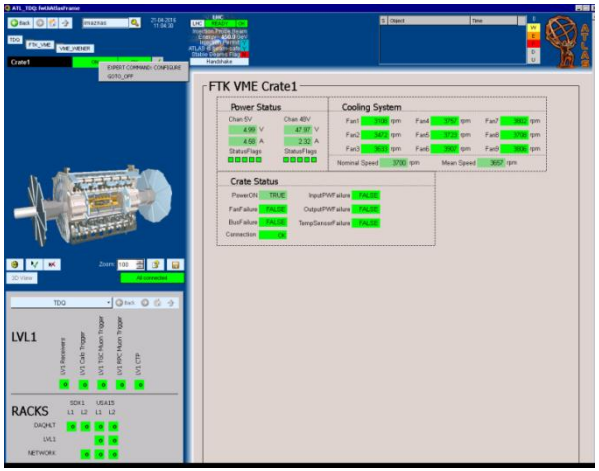
Integration in ATLAS: Run Control

FTK included in the main ATLAS DAQ Infrastructure

FTK Control System and its Special Needs

- In ATLAS it is called Detector Control System (DCS). Because of its complexity in FTK, it was split into two projects. One for ATCA chassis and one for VME bins.

ATCA chassis



Integrated FTK DCS project in ATLAS for a VME crate

VME bin

- Each VME bin hosts 16 AMBSLPs
  - Each AMBSLP has power consumption around 230W. (great heat production)
  - If cooling is not sufficient, boards can reach more than 90°C.

FTK Control System and its Special Needs

Custom fan tray

- Special custom-made Arduino-controlled fan trays were developed as a cooling system for the VME bins (replacing the standard ones). This proved to keep the temperatures to acceptable values.

- Direct monitoring of the boards was rendered mandatory. Open Platform Communications (OPC) Server had to be configured/developed using DAQ libraries and it runs on the Single Board Computer (SBC) of the VME. New for ATLAS as DCS *interacts with/uses* DAQ and SBCs are not configured for DCS purposes.

DCS project under development aiming to monitor custom equipment and the boards' thermal state

Future Plans

2015 Dec

Jan — Installation of the whole FTK input system. 128 IM and 32 DF ✓

Feb

2016 Mar

Apr

May

Jun

July — Installation of a full FTK chain with a PU of the final AM chip version ✓

Aug

Sep

Oct

Nov

Dec — FTK will cover central part of the ATLAS detector.

2017 Jan

Feb

Mar — Whole FTK system will be installed and ready for data taking.

Summary

- FTK provides full track information above $P_T > 1$ GeV to the HLT. HLT can use track information as needed.
- Board development, firmware development, installation and commissioning are progressing well.
- Already started data taking in Run II with limited detector coverage and board restrictions . Full coverage in 2017.
- FTK Technical Design Report

http://cds.cern.ch/record/1552953/files/ATLAS-TDR-021.pdf

- FTK Public Results:

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/FTKPublicResults