The NSW Trigger Processor Hardware Selection Criteria

Preliminary Design Review

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**(thanks to John Oliver and Nathan Felt
for the internal review of the two options)**

NSW PDR - CERN

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https://indico.cern.ch/event/354058/

Specifications Comparisons

- ATCA carrier boards have required interfaces
- Xilinx Virtex FPGAs with required resources
  - Footprints: 485T upgradable to 690T
- Optical I/O for Detector Data and Sector Logic
  - Each Trigger Processor should be capable of operating independently
    - Needs 14 fiber output running at 6.4 Gbps
    - Needs 32 fiber inputs (4.8 Gbps for MM, perhaps 6 Gbps for sTGC)
  - SRS Mezzanine
    - Avago µPod optical modules: 3 transmitters + 3 receivers
    - 36 i/o channels
  - LAr Mezzanine
    - Avago µPod optical modules: 4 transmitters + 4 receivers
    - 48 i/o channels ==> 36 i/o channels

Specifications Comparisons

- Mezzanine to mezzanine lateral communication
- 8 candidates need to be transferred in 1 BC
  - 21 bits of data (2+5+6+8) x 8 candidates + 6 bits (BCID) + 1 (overflow)

Field:	sTGC type	MM type	$\Delta\theta$ (mrad)	ϕ index	R index	spare
Num of bits:	2	2	5	6	8	1

  - = 175 bits/BC = 7.0 Gbps
- SRS Mezzanine:
  - Two TP FPGA per card (MM + sTGC) with 64 low-latency LVDS connections
  - Connections need to run at least at 110 MHz

Specifications Comparisons

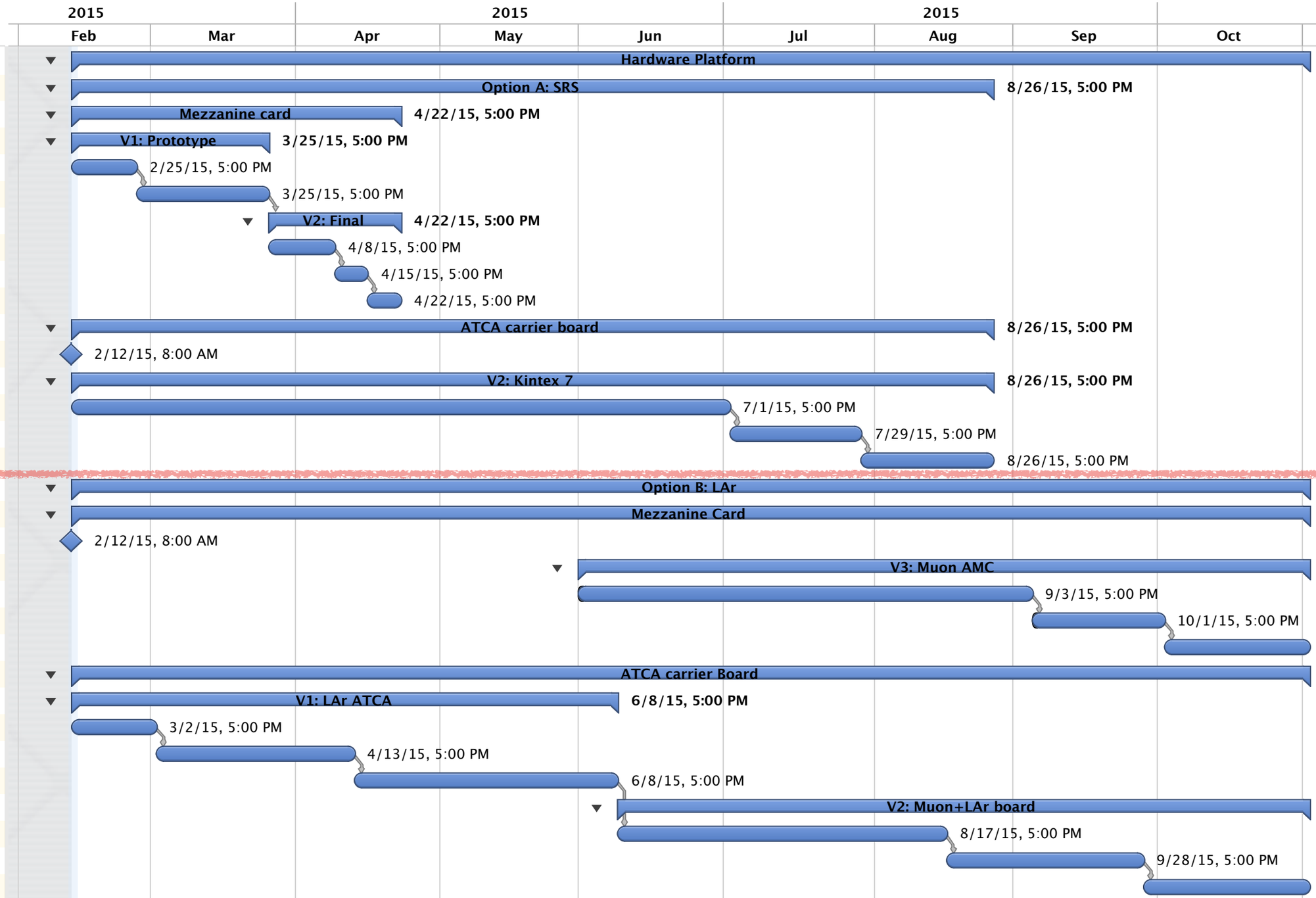
- **LAr Mezzanine:**
  - Each FPGA in independent card, connected by 8 low-latency LVDS lines via FPGA in carrier board
  - Connections tested to ~500 Mbps, but not through the FPGA
  - Designers plan to double the number of lines (16)
    - Enough to transmit 175 bits at ~440 MHz
    - A few more would be desirable, specially if we want to use one for a frame

Availability

- **LAr Option:**
  - Mezzanine
    - V2 available (enough for testing one trigger processor using μTCA crates
    - Final in Nov. 2015
  - ATCA board (in design)
    - First version in June
    - Final version in Nov. 2015
- **SRS Option:**
  - Mezzanine (in fabrication)
    - Available in April
  - ATCA board
    - First version (with Virtex 6) available — probably enough
    - Second version (with Kintex 7) in September

Schedule

Title	Effort
Hardware Platform	97w 4d
1.1) Option A: SRS	38w
1.1.1) Mezzanine card	10w
1.1.1.1) V1: Prototype	6w
1.1.1.1.1) Fabrication	2w
1.1.1.1.2) Board Testing	4w
1.1.1.2) V2: Final	4w
1.1.1.2.1) Design	2w
1.1.1.2.2) Fabrication	1w
1.1.1.2.3) Board Testing	1w
1.1.2) ATCA carrier board	28w
1.1.2.1) V1: Virtex 6	
1.1.2.2) V2: Kintex 7	28w
1.1.2.2.1) Design	20w
1.1.2.2.2) Fabrication	4w
1.1.2.2.3) Board Testing	4w
1.2) Option B: LAr	59w 4d
1.2.1) Mezzanine Card	22w 1d
1.2.1.1) V2: LAr OTC	
1.2.1.2) V3: Muon AMC	22w 1d
1.2.1.2.1) Design	13w 4d
1.2.1.2.2) Fabrication	4w
1.2.1.2.3) Board Testing	4w 2d
1.2.2) ATCA carrier Board	37w 3d
1.2.2.1) V1: LAr ATCA	16w 3d
1.2.2.1.1) Design	2w 3d
1.2.2.1.2) Fabrication	6w
1.2.2.1.3) Board Testing	8w
1.2.2.2) V2: Muon+LAr board	21w
1.2.2.2.1) Design	10w
1.2.2.2.2) Fabrication	6w
1.2.2.2.3) Board Testing	5w



Selection Criteria

1. **Delivery of required lateral bandwidth of 7.0 Gbps**
   - Having more bandwidth to transmit more information within a BC for a possible more complex algorithm in Phase-II is desirable
2. **Latency of lateral communication**
3. **Guaranteed support for additions or corrections**
   - Assurances from US ATLAS for support of Stonybrook are required
   - Clarification of details of support from Bucharest and commercial company. Guarantee of non-exclusive contract with company.
4. **Timescale of availability of cards for testing**
5. **Cost of each option**

Schedule

Title	Effort	Start	Finish
1) Hardware Platform	97w 4d	Feb	11/2/15, 5:00 PM
1.1) Option A: SRS	38w	Feb	8/26/15, 5:00 PM
1.1.1) Mezzanine card	10w	Feb	4/22/15, 5:00 PM
1.1.1.1) V1: Prototype	6w	Feb	3/25/15, 5:00 PM
1.1.1.2) V2: Final	4w	Mar	4/22/15, 5:00 PM
1.1.2) ATCA carrier board	28w	Feb	8/26/15, 5:00 PM
1.1.2.1) V1: Virtex 6		2/12/15, 8:00 AM	
1.1.2.2) V2: Kintex 7	28w	Feb	8/26/15, 5:00 PM
1.2) Option B: LAr	59w 4d	Feb	11/2/15, 5:00 PM
1.2.1) Mezzanine Card	22w 1d	Feb	11/2/15, 5:00 PM
1.2.1.1) V2: LAr OTC		2/12/15, 8:00 AM	
1.2.1.2) V3: Muon AMC	22w 1d	Jun	11/2/15, 5:00 PM
1.2.1.2.1) Design	13w 4d	Jun	9/3/15, 5:00 PM
1.2.1.2.2) Fabrication	4w	9/3/15, 5:00 PM	10/1/15, 5:00 PM
1.2.1.2.3) Board Testing	4w 2d	10/1/15, 5:00 PM	11/2/15, 5:00 PM
1.2.2) ATCA carrier Board	37w 3d	Feb	11/2/15, 5:00 PM
1.2.2.1) V1: LAr ATCA	16w 3d	Feb	6/8/15, 5:00 PM
1.2.2.1.1) Design	2w 3d	Feb	3/2/15, 5:00 PM
1.2.2.1.2) Fabrication	6w	3/2/15, 5:00 PM	4/13/15, 5:00 PM
1.2.2.1.3) Board Testing	8w	4/13/15, 5:00 PM	6/8/15, 5:00 PM
1.2.2.2) V2: Muon+LAr board	21w	Jun	11/2/15, 5:00 PM
1.2.2.2.1) Design	10w	Jun	8/17/15, 5:00 PM
1.2.2.2.2) Fabrication	6w	8/17/15, 5:00 PM	9/28/15, 5:00 PM
1.2.2.2.3) Board Testing	5w	9/28/15, 5:00 PM	11/2/15, 5:00 PM
2) Firmware	190w	Feb	
2.1) Ancillary Functions	128w 2d	Feb	
2.1.1) Basic	16w	Feb	6/3/15, 5:00 PM
2.1.2) Enhanced	112w 2d	6/3/15, 5:00 PM	
2.2) sTGC Trigger Algorithm	28w	Feb	7/29/15, 5:00 PM
2.3) MM Trigger Algorithm	21w 3d	Feb	6/3/15, 5:00 PM
2.4) sTGC+MM Merging	12w	Feb	5/6/15, 5:00 PM
3) Testing	0h	May	12/1/15, 8:00 AM
3.1) Vertical Slice Start		12/1/15, 8:00 AM	
3.2) Cosmic Ray Tests Start		9/1/15, 8:00 AM	
3.3) MSW Start		5/1/15, 8:00 AM	
4) External factors	1d	Feb	9/1/15, 8:00 AM
4.1) VMM2 Chip Ready	1d	2/12/15, 5:00 PM	
4.2) VMM3 Chip Ready		9/1/15, 8:00 AM	