TGC FEB Specification

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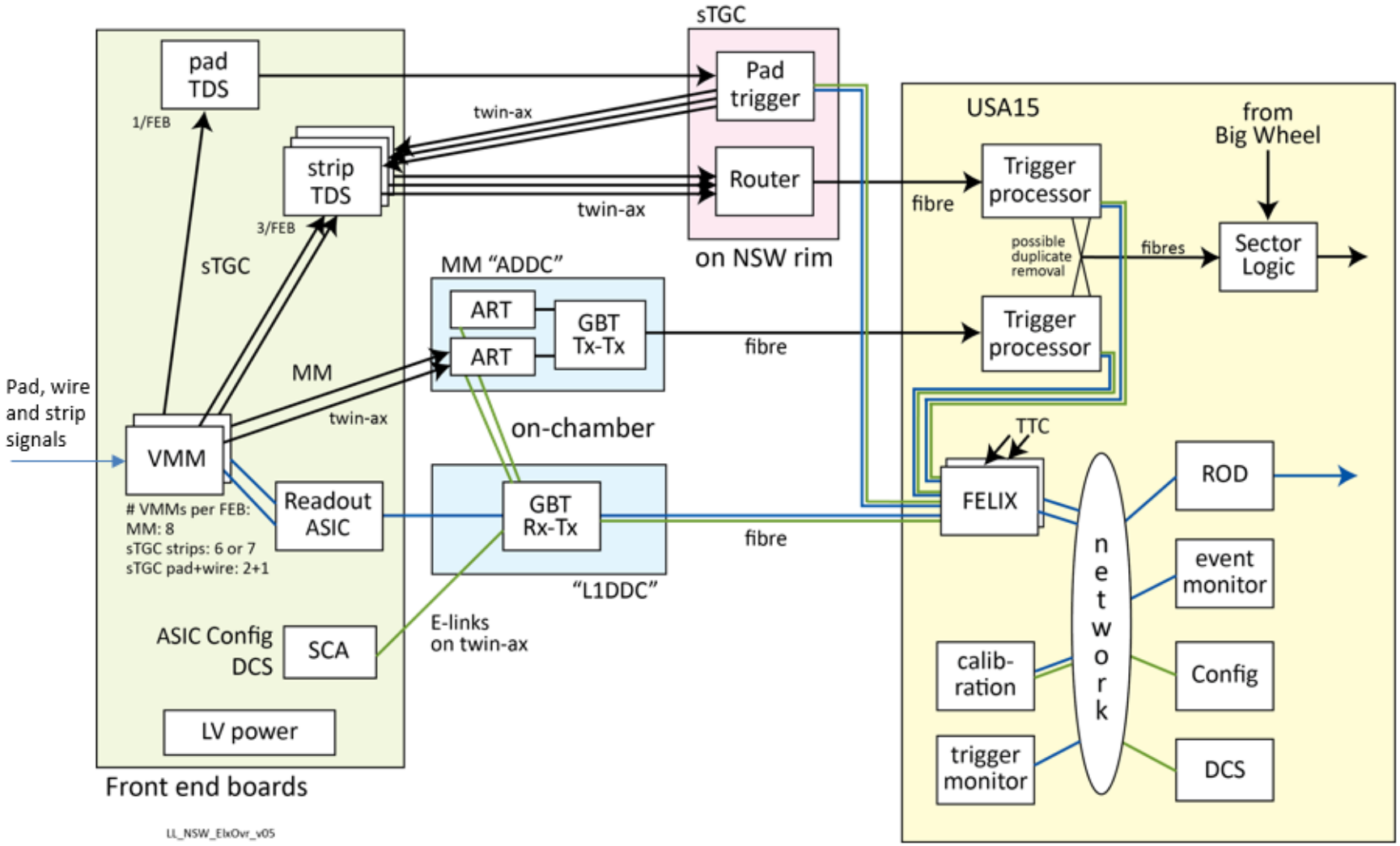
USTC

TGC FEB Overview

- TGC FEB is the interface between the sTGC detectors and Trigger (Router) and L1DDC
- TGC FEB will receive 3 different types of signal: pad, wire and strip.
- TGC FEB will read in all the signals, digitalize them in a 64-channel VMM chip, and convert signal of each channel into 2 types of data, L1 raw data and trigger data
- 2 types of FEB: sFEB for readout strip signals, pFEB for readout pad+wire signals.

NSW Electronics Trigger and dataflow



ASIC chips

- VMM: designed by BNL. Each VMM can handle 64 analog inputs, send trigger data of all the 64 channels to TDS, and serial outL1 raw data to ROC.
- TDS: designed by Michigan University. Each TDS handles128 channels of trigger data, namely output from 2 VMM chips. TDS canpick out real triggered pads or strips, serialize and send data to Pad Trigger Logic or the Route via mini SAS-36 connector.
- ROC: has not been decided yet. Its function is to readout L1 raw data from VMM and send the data to L1DDC by E-link.
- GBT-SCA: designed by CERN GBT group. Its function is to receive data from L1DDC by E-link and transfer it to I2C to configure VMM, TDS and ROC.
- DS2401: the function is PCB identification. Suggest to deploy it on the adapter board between sTGC and FEB.

Strip FEB specification

- The aim of sFEB is to readout sTGC strip signals, and it has two functions:

1. to digitalize strip charge signal and arriving time of signal, serialize and transmit to L1DDC;
2. to pick up trigger information and transmit to L1 trigger processor via the Route.

- The inputs of sFEB connect to sTGC strip adapter via two GFZ-30 connector each of them can handle 256 strip signals.

- Each sFEB serves one sTGC plane which has 384-448 strips.

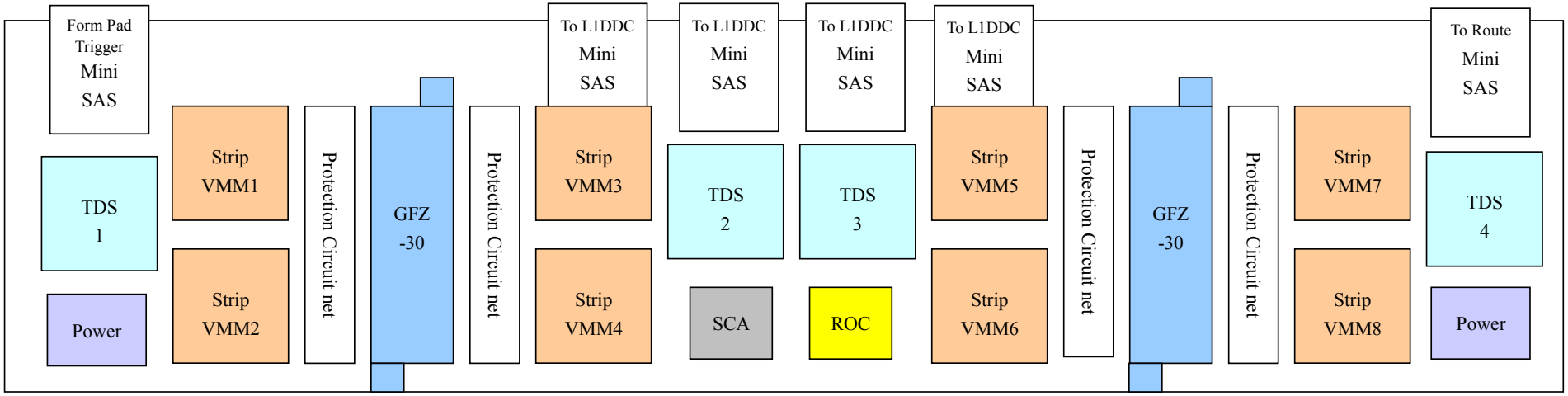
- Four sFEBs will be used in a sTGC module, in which two of them are located at one side of sTGC and the other two at the opposite side.

- Total 768 sFEBs will be assembled on NSW.

sFEB Features

- 512 inputs to meet the number of 384 to 448 sTGC strip outputs
- Up to 8 VMMs are designed on one sFEB
- 4 TDSs are used for readout VMMs trigger information, serialize trigger data and output to the Router by a mini SAS. Each TDS handles 2 VMMs.
- 4 input pins for sTGC plane ID
- 2 Samtec GFZ-30 connectors will be used to connect sFEB to sTGC adapter board.
- 6 mini SAS-36 connectors will be used for pad trigger in, TDS trigger out, ROC data out and SCA in.
- 1 ROC chip will be developed to read VMM output raw data and sendthe L1 data to GBT by E-link. 4 mini SASs will be used for raw data transmission
- 1 GBT-SCA will be used for configuration of VMM and TDS
- 1 power connector (04P MTA156 HDR ASSY FL/STR SN) will be used for power.

The layout of sFEB.



Pad FEB specification

- pFEB is to readout TGC pad signals, as well as wire signals. For pad, it has two functions:

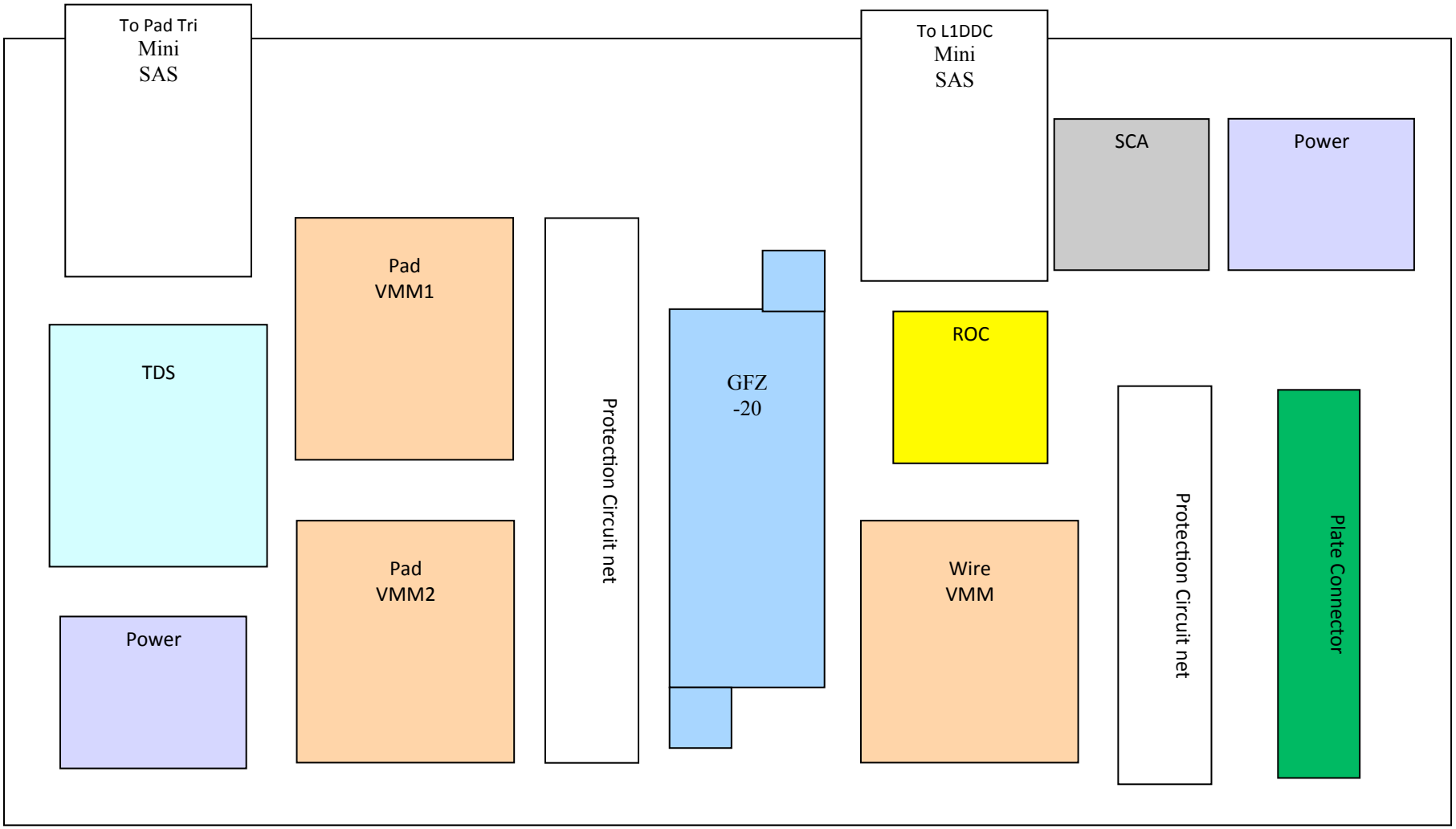
1. To digitalize pad charge signal and arriving time of signal, serialize and transmit to L1DDC;
2. to pick up trigger information and transmit to pad trigger unit via twin-ax cable.

- The inputs of pFEB connect to sTGC pad adapter via one GFZ-20 connector, which can handle 64-104 pad signals depending on the position of the sTGC;
- 1 flat cable connector will be used to connect wires of TGC.

- One pFEB serves one sTGC plane. There are four pFEBs in a sTGC module, in which two of them are located at one side pf sTGC and the other two are at the opposite side.

- Total 768 PFEBs will be assembled on NSW.

The layout of pFEB (pad+wire)



pFEB Features

- 104 inputs will be read as pad signal output, and 64 inputs as wire signal output
- 2 VMMs for readout sTGC pad signals, discriminating trigger for TDS, digitalizing timing and amplitude and output to ROC;
- 1 VMM for readout sTGC wire signals, digitalizing timing and amplitude and output to ROC.
- 1 TDS for readout pad VMM trigger information, serializing trigger data and output to pad trigger unit by a mini SAS.
- 4 input pins for sTGC plane ID
- 1 Samtec GFZ-20 connector will be used to connect sFEB to sTGC adapter board.
- 1 flat cable connector will be used to connect wires of TGC.
- 2 mini SAS-36 connectors will be used for TDS pad trigger out, ROC data out and SCA in.
- 1 ROC for readout VMM output raw data and send the L1 data to GBT by E-link. A mini SAS connector will be used for raw data transmission.
- 1 GBT-SCA will be used for configuration of VMM and TDS
- 1 power connector (04P MTA156 HDR ASSY FL/STR SN) will be used for power.

Mechanical issuls-PCB

- sFEB:

1. Size limit: 29×6cm
2. ASIC on the top of PCB
3. SamTec GFZ and miniSAS on the bottom

- pFEB

1. Size limit:15×6cm
2. ASIC on the top of PCB
3. SamTec GFZ and miniSAS on the bottom
4. Flat cable connector on the top?

sFEB and pFEB versions

There will be 4 versions of FEB to develop before mass production

- V1(VMM2/FPGA): Version 1 is actually a prototype based on current no-trigger-output VMM2, and uses FPGAs pending delivery of TDS and ROC chips. The aims of this version are to realize the basic functions, such as configuration, TGC signal input, data read out. This version can be used to test FEB real performances and also can be used to test sTGC.

- V2 (VMM3/TDS/ROC/SCA):Version 2 is basic FEB with all special designed and commercial chips, such as VMM3, TDS1, ROC, SCA, through these chips still keep to be developed. Test should include electronics test, detector test and beam test. All functions and performances of FEB should be carefully tested, to get information for next version.

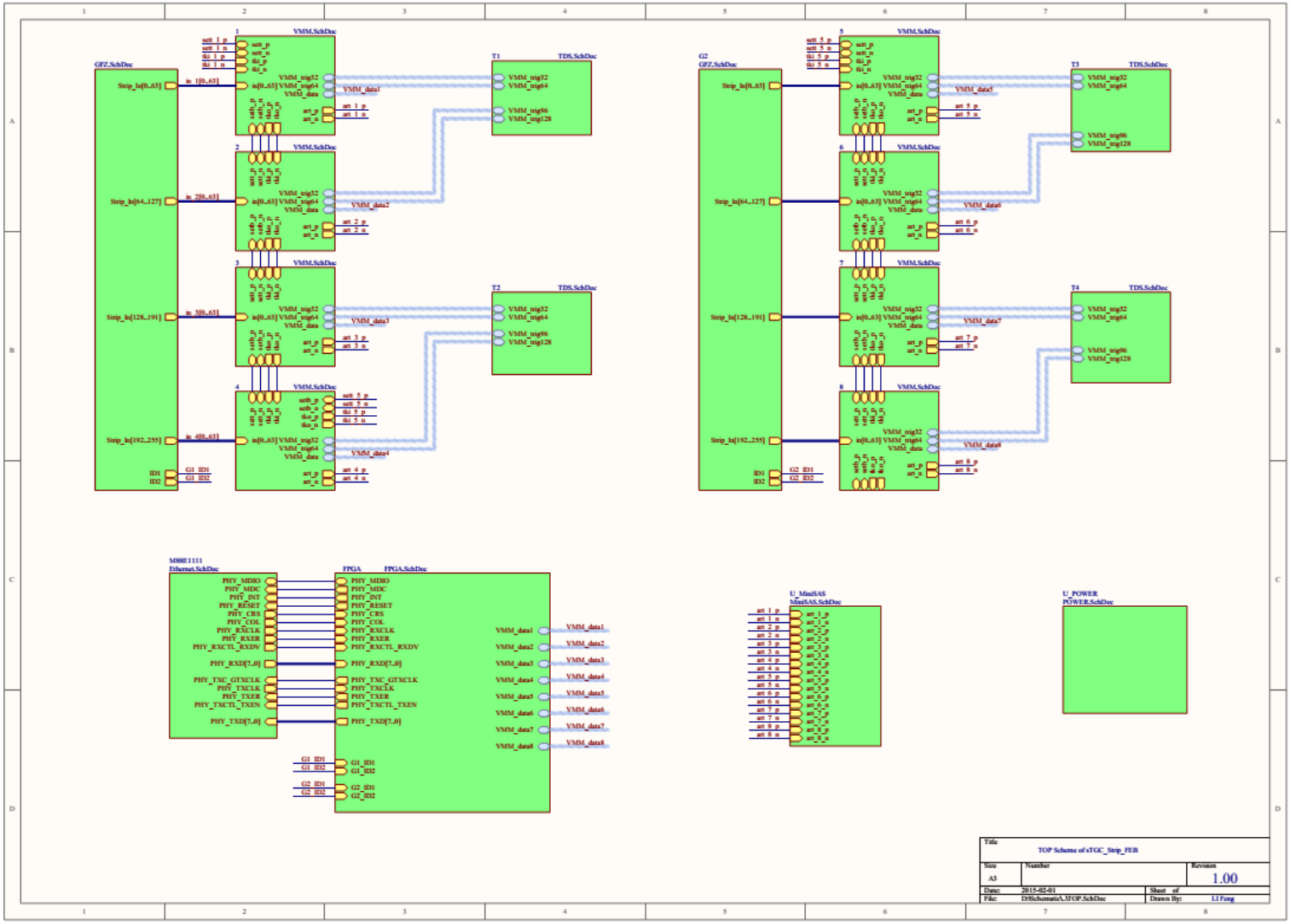
- V3 Preproduction (VMM3A /TDS/ROC/SCA):Version 3 is an approved production version with approved special IC, such as VMM3A, TDS2, ROC, SCA and power chip. All chips on the board are final version.

- V4 Production (VMM3A /TDS/ROC/SCA):Version 4 is the final product that will be mass produced. It is almost as same as V3, but may allow to be optimized in layout, size, package, tab, assembly, etc.

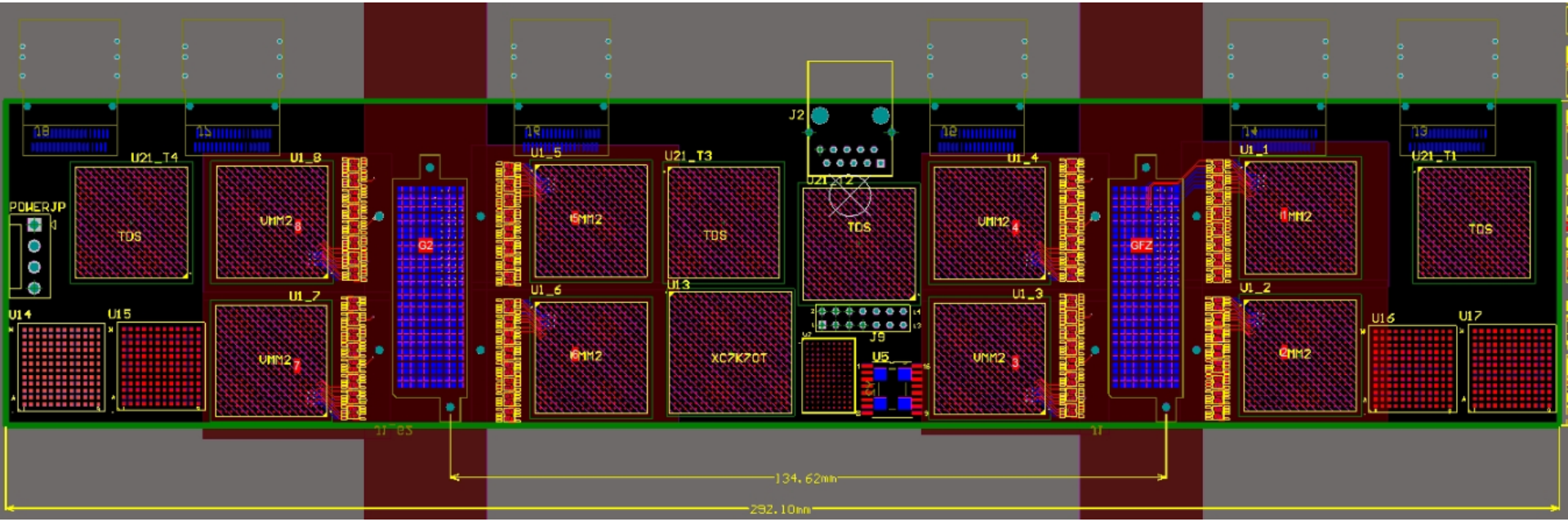
sFEB V1

- 8 VMM2 will be used and maximum 512 inputs can be fed in. The idea of 8 VMM design is to keep the symmetry of all channels and make it easily assembled on both sides of sTGC module
- 4 FPGAs is used to replace 4 TDS for studying the layout
- 1 FPGA is used to readout data and configure VMM.

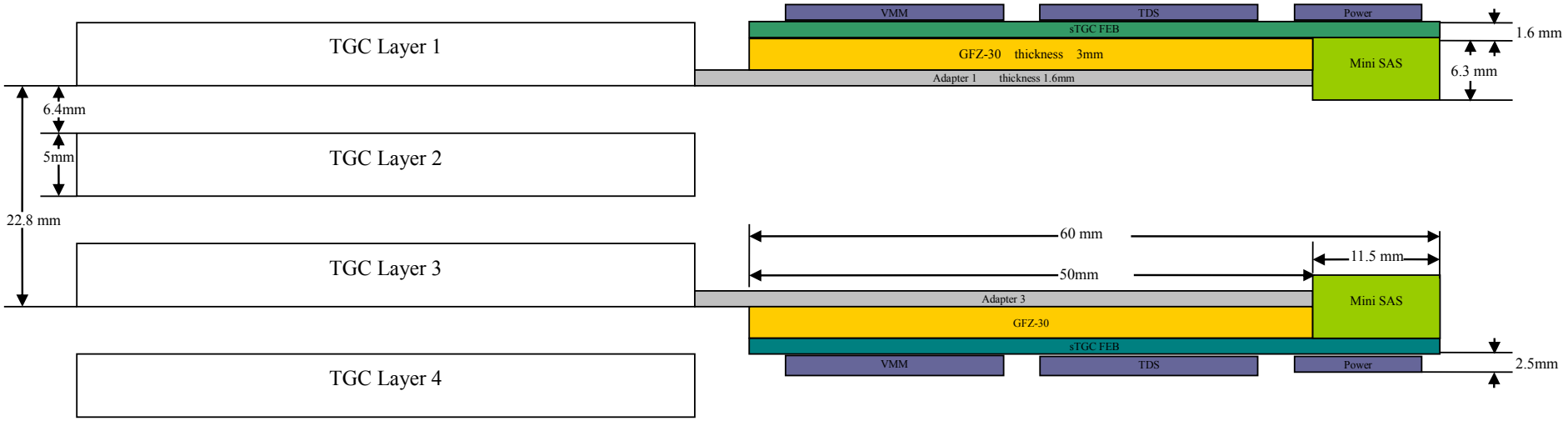
The top of schematic of sFEB V1



PCB of sFEB V1



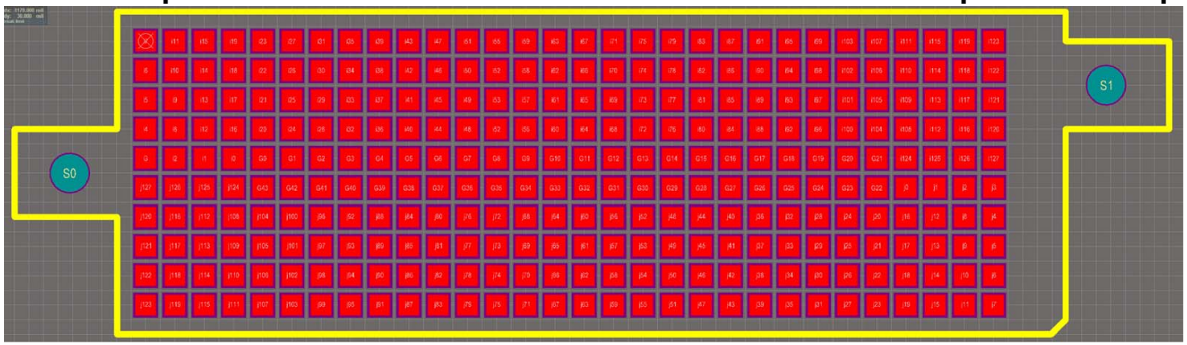
Mechanical issuls-Assembly



- the side view of the FEB assembly onto adapter board to sTGC plane.
- The odd-numbered boards, FEB1 and FEB3, are fix on the right side of the detector module;
- The even-numbered boards, FEB2 and FEB4, go to the left side.

GFZ-30 pin definition

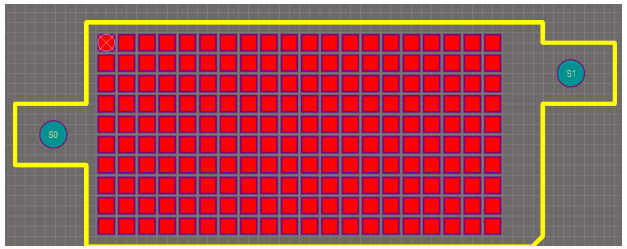
- FEB should use the top footprint and placed it on the bottom layer; while adapter board should use the bottom footprint and placed it on the top layer.



Position / Row	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
1	i7	i11	i15	i19	i23	i27	i31	i35	i39	i43	i47	i51	i55	i59	i63	i67	i71	i75	i79	i83	i87	i91	i95	i99	i103	i107	i111	i115	i119	i123
2	i6	i10	i14	i18	i22	i26	i30	i34	i38	i42	i46	i50	i54	i58	i62	i66	i70	i74	i78	i82	i86	i90	i94	i98	i102	i106	i110	i114	i118	i122
3	i5	i9	i13	i17	i21	i25	i29	i33	i37	i41	i45	i49	i53	i57	i61	i65	i69	i73	i77	i81	i85	i89	i93	i97	i101	i105	i109	i113	i117	i121
4	i4	i8	i12	i16	i20	i24	i28	i32	i36	i40	i44	i48	i52	i56	i60	i64	i68	i72	i76	i80	i84	i88	i92	i96	i100	i104	i108	i112	i116	i120
5	i3	i2	i1	i0	G	G	G	G	G	G	G	G	G	G	ID1	G	G	G	G	G	G	G	G	G	G	G	i124	i125	i126	i127
6	j127	j126	j125	j124	G	G	G	G	G	G	G	G	G	G	G	ID2	G	G	G	G	G	G	G	G	G	G	j0	j1	j2	j3
7	j120	j116	j112	j108	j104	j100	j96	j92	j88	j84	j80	j76	j72	j68	j64	j60	j56	j52	j48	j44	j40	j36	j32	j28	j24	j20	j16	j12	j8	j4
8	j121	j117	j113	j109	j105	j101	j97	j93	j89	j85	j81	j77	j73	j69	j65	j61	j57	j53	j49	j45	j41	j37	j33	j29	j25	j21	j17	j13	j9	j5
9	j122	j118	j114	j110	j106	j102	j98	j94	j90	j86	j82	j78	j74	j70	j66	j62	j58	j54	j50	j46	j42	j38	j34	j30	j26	j22	j18	j14	j10	j6
10	j123	j119	j115	j111	j107	j103	j99	j95	j91	j87	j83	j79	j75	j71	j67	j63	j59	j55	j51	j47	j43	j39	j35	j31	j27	j23	j19	j15	j11	j7

GFZ-20 pin definition

- FEB will use top layer pin map of GFZ. TGC adapter will use bottom layer pin map of GFZ.
- A 10 rows GFZ is split in two parts with 5 rows. Each 5 rows service 2 VMMs. The 2 pins in center will be used as TGC ID.



Position / Row	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
1	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
2	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G
3	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	G	P0	P1	P2	P3
4	P107	P106	P105	P104	G	G	G	G	G	G	G	G	G	G	G	G	P4	P5	P6	P7
5	P103	P102	P101	P100	G	G	G	G	G	ID1	ID3	G	G	G	G	G	P8	P9	P10	P11
6	P99	P98	P97	P96	G	G	G	G	G	ID4	ID2	G	G	G	G	G	P12	P13	P14	P15
7	P92	P88	P84	P80	P76	P72	P68	P64	P60	P56	P52	P48	P44	P40	P36	P32	P28	P24	P20	P16
8	P93	P89	P85	P81	P77	P73	P69	P65	P61	P57	P53	P49	P45	P41	P37	P33	P29	P25	P21	P17
9	P94	P90	P86	P82	P78	P74	P70	P66	P62	P58	P54	P50	P46	P42	P38	P34	P30	P26	P22	P18
10	P95	P91	P87	P83	P79	P75	P71	P67	P63	P59	P55	P51	P47	P43	P39	P35	P31	P27	P23	P19

Un-defined connectors

- Plate connector for wire: this connector with 64 pin is located on pad + wire adapter for wire input.
- Mini SAS-36 for Pad/Strip trigger out, and Pad trigger in on FEB
- Mini SAS-36 for ROC out on FEB.
- Power connector: A 4 pin power connector (04P MTA156 HDR ASSY FL/STR SN) will be used.

Test

- There are 3 kinds of test should be done during the development of FEB:

1. Electronics test
2. Beam test
3. Mass inspection.

Electronics preparation

- To test hundreds ofFEB channels, a signal generator with 256 outputs is being developed .There are five test modes can be applied to the signal generator:

1. Single mode: output a current pulse to a specified channel in a bunch clock to check a specified channel of FEB.

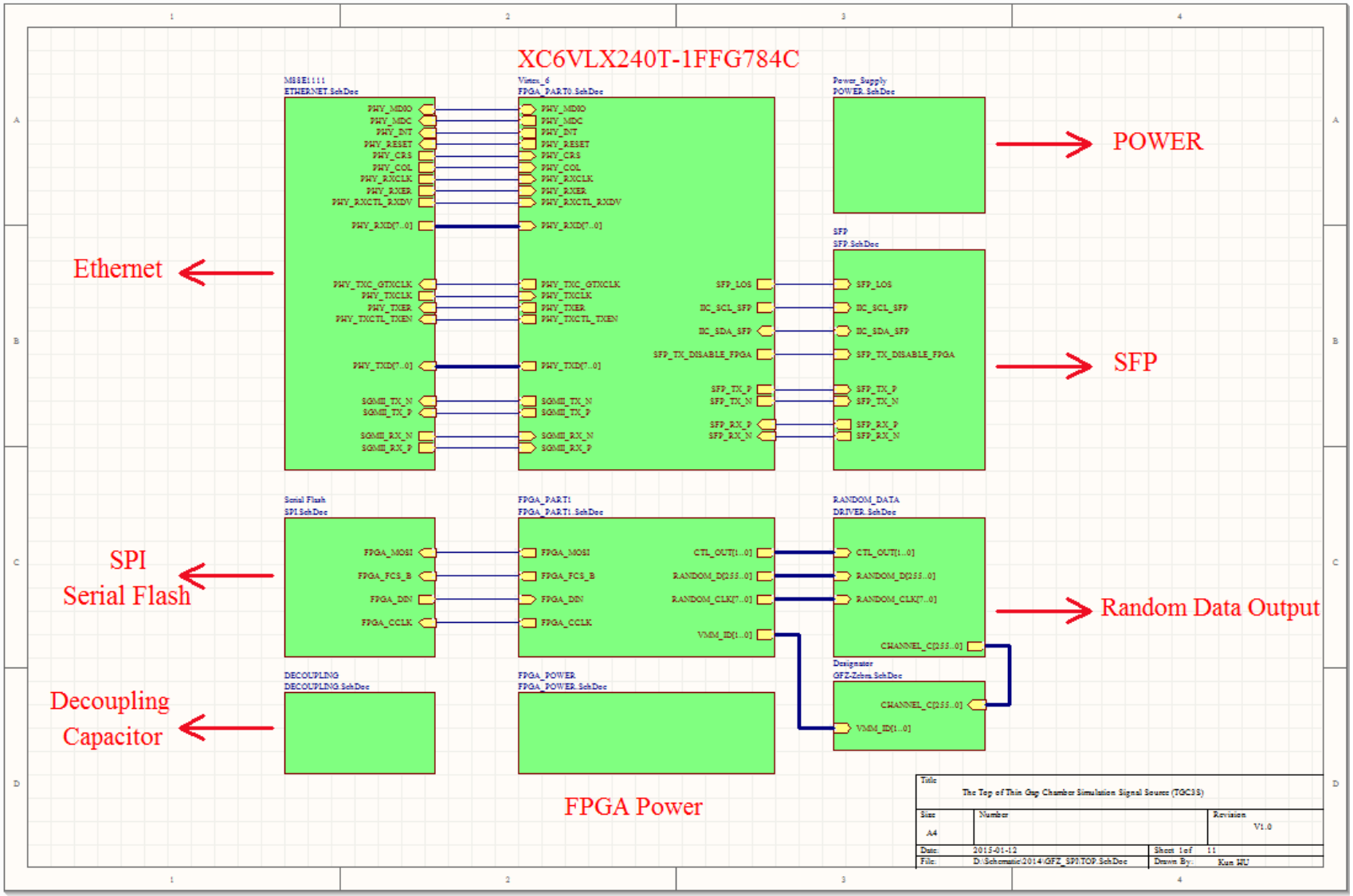
2. Scan mode: output a current pulse to every channel in sequence in each bunch clock to check every channel of FEB.

3. Full mode: output a current pulse to all channels at same time in a bunch clock to check consistency of all channels of FEB

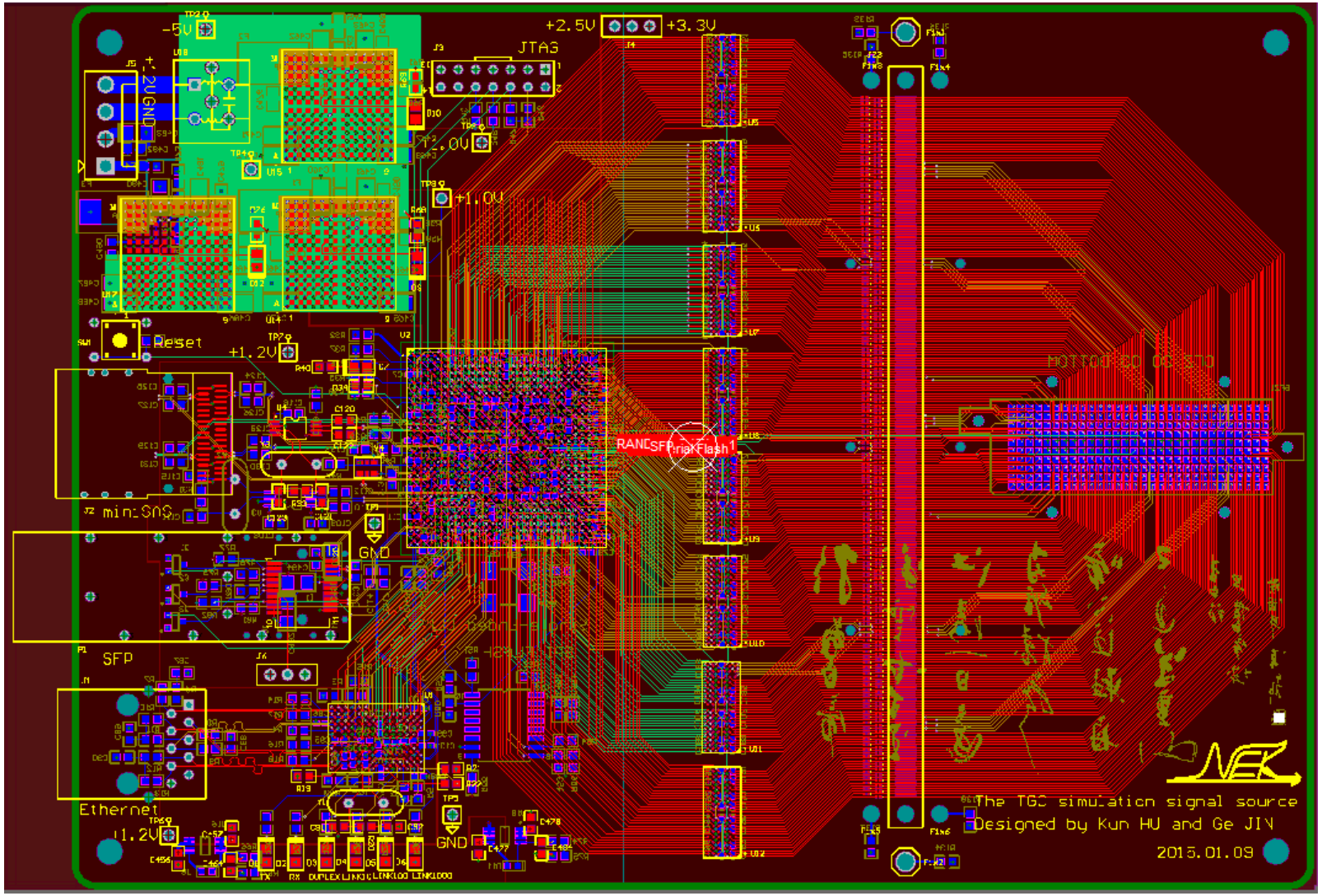
4. Event mode: output a group of current pulses in adjacent channels in a bunch clock to simulate sTGC event.

5. Strip + pad mode: 64 channels output pad trigger signal and 192 channels output strip trigger to check TDS functions.

The top of schematic of signal generator



The PCB layout of the signal generator



Schedule

sTGC Front End boards						
WBS	Activity ID	FEB Work	Activity Name	Original Duration	Start	Finish
1.02.02.00	FEB0000		Signal Generator	318	1-Jan-14	15-Nov-14
	FEB0010		Design	14	30-Apr-14	14-May-14
	FEB0020		Layout	15	15-May-14	30-May-14
	FEB0030		Firmware Development	165	1-Jan-14	15-Jun-14
	FEB0040		PCB Fabrication	17	3-Jun-14	20-Jun-14
	FEB0050		PCB Assembly	9	21-Jun-14	30-Jun-14
	FEB0060		Test	137	1-Jul-14	15-Nov-14
1.02.02.01	FEB1000		Signal Generator v1 (GFZ/Zebra)	226	16-Nov-14	30-Apr-15
	FEB1010		Design	14	16-Nov-14	15-Dec-14
	FEB1020		Layout	15	16-Dec-14	30-Jan-15
	FEB1030		Firmware Development	165	1-Feb-15	31-Mar-15
	FEB1040		PCB Fabrication	17	1-Feb-15	28-Feb-15
	FEB1050		PCB Assembly	9	1-Mar-15	15-Mar-15
	FEB1060		Test	45	15-Mar-15	30-Apr-15
	FEB1070		Assembly 4 copies	45	15-Apr-15	30-Apr-15
1.02.02.01	FEB1000		Mini FEB	547	1-Apr-14	30-Sep-15
	FEB1010		Design	228	1-Apr-14	15-Nov-14
	FEB1020		Layout	76	16-Nov-14	31-Jan-15
	FEB1030		Firmware Development	149	1-Feb-15	30-Jun-15
	FEB1040		PCB Fabrication	14	1-Jul-15	15-Jul-15
	FEB1050		PCB Assembly	15	16-Jul-15	31-Jul-15
	FEB1060		Test	60	1-Aug-15	30-Sep-15
1.02.02.02	FEB2000		TGC FEB v1 (VMM2/FPGA)	395	1-Oct-14	31-Oct-15
	FEB2010		Design	75	1-Oct-14	15-Dec-14
	FEB2020		Layout	74	16-Dec-14	28-Feb-15
	FEB2030		Firmware Development	152	1-Mar-15	31-Jul-15
	FEB2040		PCB Fabrication	19	1-Aug-15	20-Aug-15
	FEB2050		PCB Assembly	15	16-Aug-15	31-Aug-15
	FEB2060		Test	60	1-Sep-15	31-Oct-15
1.02.02.03	FEB3000		TGC FEB v2 (VMM3/FPGA/Comp/SCA)	152	1-Jul-15	30-Nov-15
	FEB3010		Design	14	1-Jul-15	15-Jul-15
	FEB3020		Layout	46	16-Jul-15	31-Aug-15
	FEB3030		PCB Fabrication	14	1-Sep-15	15-Sep-15
	FEB3040		PCB Assembly	14	16-Sep-15	30-Sep-15
	FEB3050		Test	60	1-Oct-15	30-Nov-15
	FEB3100		TGC FEB Preproduction V3 (VMM3A/TDS/Comp/SC	181	1-Jan-16	30-Jun-16
	FEB3110		Design	14	1-Jan-16	2016-1-15
	FEB3120		Layout	24	16-Jan-16	2016-2-9
	FEB3130		PCB Fabrication	18	10-Feb-16	2016-2-28
	FEB3140		PCB Assembly	30	1-Mar-16	31-Mar-16
	FEB3150		Test	90	1-Apr-16	30-Jun-16
	FEB3200		TGC FEB Production V4 (VMM3A/TDS/Comp/SCA)	199	16-Jul-16	31-Jan-17
	FEB3210		Design	14	1-Jul-16	15-Jul-16
	FEB3220		Layout	15	16-Jul-16	31-Jul-16
	FEB3230		PCB Fabrication	30	1-Aug-16	31-Aug-16
	FEB3240		PCB Assembly	76	15-Aug-16	30-Oct-16
	FEB3250		Test	241	1-Nov-16	30-Jun-17
	FEB3260		Ship to construction sites	211	1-Jan-17	31-Jul-17