ATLAS Muon New Small Wheel
Grounding, Power and Interconnect
-Guidelines and Policies-

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John Oliver

for the ATLAS Muon NSW Grounding Working Group:
Theo Alexopoulis, Jon Ameel, Dan Amidei, Ryan Edgar, John Huth, Mauro Iodice, Ken Johns, Agostino Lanza, Lorne Levinson, Nachman Lupu, Giora Mikenberg, John Oliver, Vinnie Polychronakos, Patrick Ponsot, Givi Sekhniaidze
[Ref 1]

- Standard grounding practices
- NSW specific issues
- "Gounding Doc" →NSW Grounding Signaling 20150202.pdf (on EDMS)

  Specifies all "Guidelines" and "Policies" for grounding and signal transmission in NSW detectors and electronics

[Ref 1] Many useful discussions with Veljko Radeka and Gianluigi De Geronimo are gratefully acknowledged

Standard practices

General principles

Detector, electronics, and power supplies completely contain their own currents. None leaks ***out to***, or ***in from***, the environment. ***No ground loops***.

•Each sector will be attached to its ***mechanical frame via insulated attachments***. This insures that the mechanical mounts do not constitute signal or power supply paths or allow unintended ground currents.

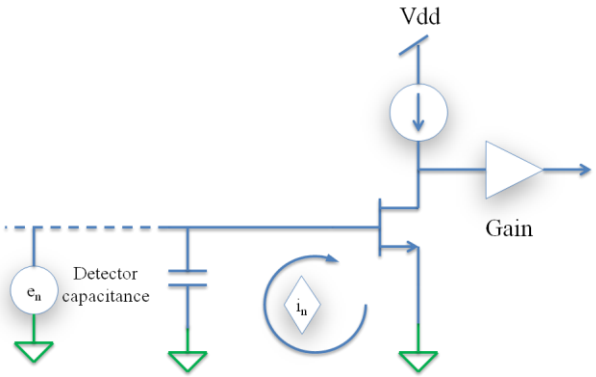
• Each Sector of the NSW will be connected to a common grounding point by means of a ***low inductance, low resistance ground strap.***

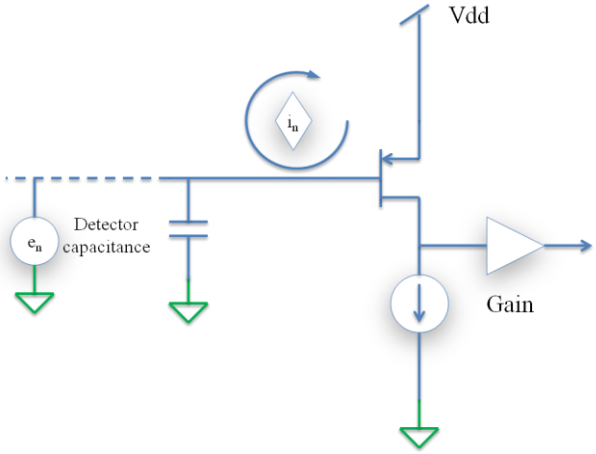
•The ***outer Faraday enclosure of each sector will be connected to this strap.***

•The ***ground strap must carry zero current*** (by design, not accident)
→Ground strap is **only** point of entry/exit for current to detector

• All DCS sensors (temperature, B field, etc) ***must be insulated from detector faraday enclosure (Ground)***

Frontend electronics issues – Hybrid vs ASIC (VMM)





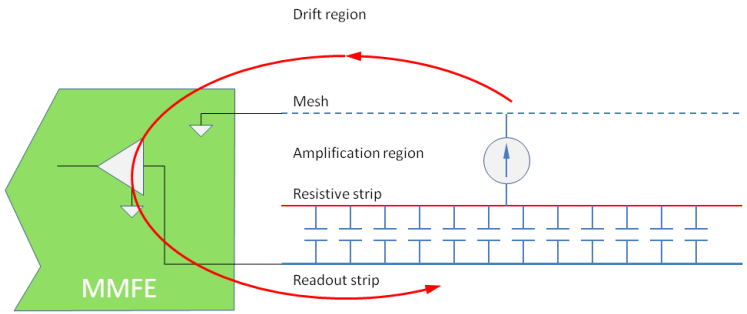
"Traditional" frontend amplifier

- Generally hybrid technology
- N-channel jfet chosen for low-noise, high transconductance
- Main "gain" junction is gate-source **(detector-AGND)**
- Bypassing Vdd is relatively easy. Amplifier has good PSRR
- Keep gate-source loop **small** and **well shielded**

ASIC frontend amplifiers (VMM)

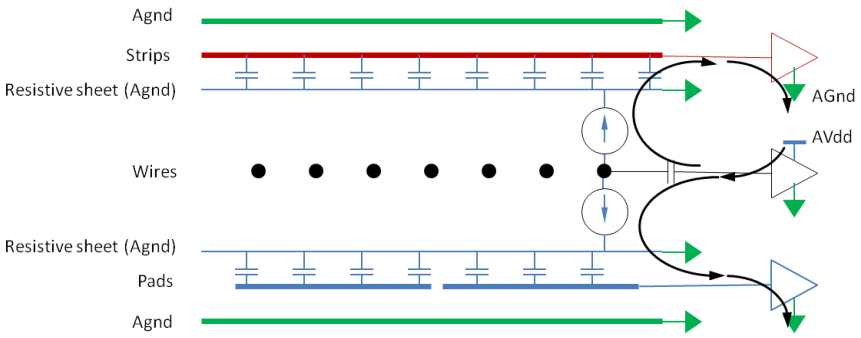
- Generally CMOS ASIC technology
- P-channel mosfet chosen for lower 1/f noise as compared with n-channel devices in same technology (Exception is MDT-ASD which used n-channel mosfet)
- Main "gain" junction is gate-source (**detector-AVdd**)
- Bypassing Vdd is more difficult. Amplifier has poorer PSRR
- Special attention to Vdd /AGND/Faraday cage bypassing.
- Frequently requires special attention to pcb "planes" used under ASIC and detector inputs → AVdd instead of AGND
- ASIC designers should be consulted on detailed frontend board designs.

Micromegas signal model



• Relatively simple (and small) signal flow loop.
• Approximately square pulse developed in amplification region → 50ns to 100ns wide depending on ion drift velocity.
• Signal developed between mesh (AGND) and resistive strip
• Detailed SPICE modeling done of signal flow & timing (G. De Geronimo, J. Oliver).
• Resistive strip tightly coupled to Readout Strip → ~ 15% signal loss
• HV biasing of resistive strip must by bypassed, ideally to Avdd, but this is not practical. → Bypass to AGnd
• High value resistance must be placed between bypass cap and resistive strip to avoid "end effect", or loss of gain at strip ends.
• Overlap of resistive strip beyond readout strip end constitutes needed bypass resistor – no discrete resistor necessary

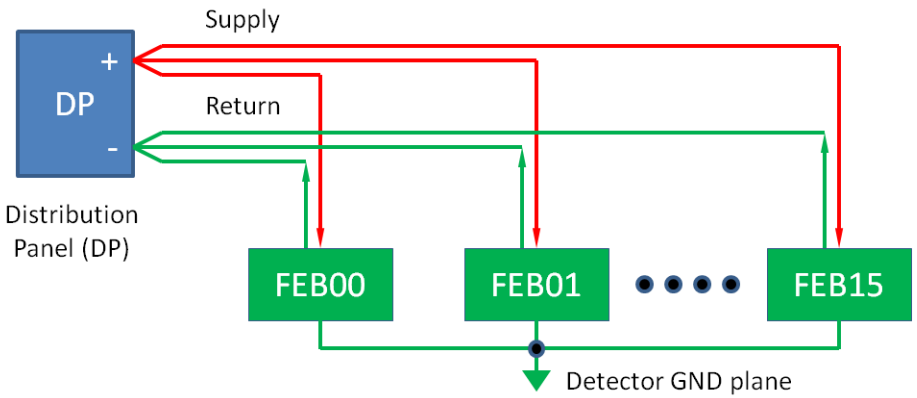
sTGC signal model



- Relatively complex signal loop path involving both boards and the AGND plane
- Ignoring resistive sheets, signals go from
  - Avdd
  - VMM_{wire}
  - Wires
  - Strips&Pads
  - VMM_{strip} & VMM_{pad}
  - AGND
- Adequate Vdd/AGND bypassing essential
- Must have very **low inductance, low resistance** paths from Frontend Board to sTGC AGND plane

LV Distribution

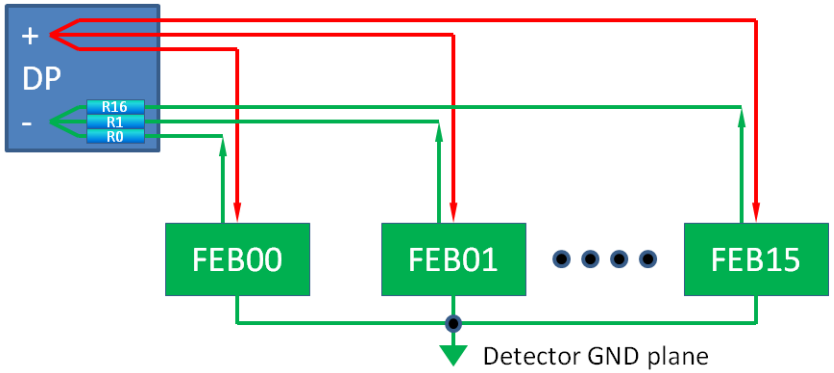
• Same situation exists for MM and sTGC → MM shown explicitly (Grounding Doc describes both)



• Supply line lengths vary from a few 10s of cm to ~ 4m
• Cable resistances vary accordingly (if all the same gauge)
• All return lines have same voltage drop → current can vary by large factors
• If average current is 1A, then return currents can vary from 1/4A for the farthest from DP to ~4A for the nearest.
• Large bulk supply currents would mix across detector Analog Ground planes.
• Note that **DC/DC converters on Frontend Boards are not ground isolated**. If they were, we wouldn't need to worry about equalizing return lines.

LV Distribution (cont)

• Remedy → Equalize return path resistances with discrete "ballast" resistors in Distribution Panel



• Careful resistor choice → Equalized return currents to ~10% or better
• Not required in supply lines because frontend board's DC/DC converters are tolerant to varying line drops
• Bulk supplies must have floating RETURN connection : NOT Grounded, but "Safety Grounds" may be required by CERN safety standards.

Possible fault modes

• Frontend board failure may result in
  - ❑Reduced total current
  - ❑ Excess current
  - ❑ Blown fuse (Zero current)[1]

• In each case, return currents will equalize for all boards, including the fault board
• Imbalanced current will be redistributed by detector's Agnd plane
• Consequences of this situation should be tested.

[1] Fused supply lines may be required by CERN safety regs to prevent cable fire or catastrophic failure. This is under investigation.

HV Distribution

• Similar (ground drop) condition does not exist for HV distribution because currents are much lower

• Safety regulations require that unlike LV, the HV **supply must be Grounded at supply**

• Ground **loop at point of HV delivery is "broken" by resistor** placed in the cable-to-detector ground connection.

• This is very standard as was done in MDTs and many other detectors

• Resistor of several 100s of Ohms to 1 kOhm are typical.

LVDS Cabling Convention

• LVDS will be used extensively between on-detector boards in both MM and sTGCs

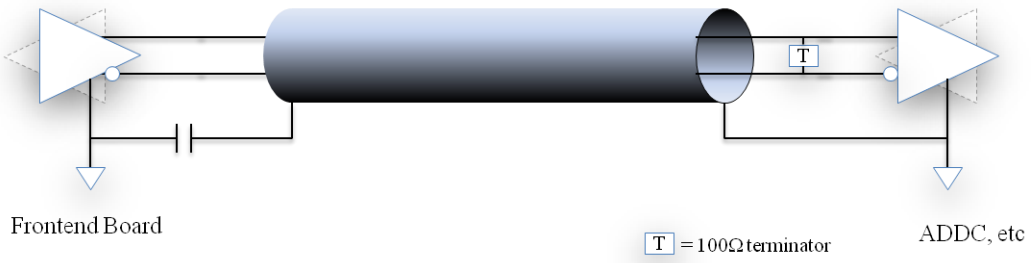
• LVDS lines couple “frontend” boards with first level DAQ and/or Trigger data collection boards. Lines go in both directions.

• Cable shield **grounds and drain wires must be AC coupled at one end only** to prevent web of ground loops which would otherwise occur. It has no impact on signal integrity.

• By convention, the **ground’s AC coupling is placed at the “Frontend Board”** regardless of which is driving or receiving end.

• **Signal lines should be DC coupled** as there will be no large common mode ground differences between boards.

•8b/10b is not required but would do no harm if used. ART Data (MM trigger) is serial with **no 8b/10b or dc balance encoding.**



Conclusion

Is a “NSW Grounding document” really necessary?

- “It prevents a lot of headache and grief later on”- NSW Grounding Working Group
- “I think it would be a very good idea” - M. Gandhi

References

1. Shielding and Grounding in Large Detectors – V. Radeka
2. Grounding of the ATLAS Experiment – G. Blanchot et al
3. ATLAS Muon Grounding – J. Huth, et al
4. MINOS Far Detector Grounding Proposal – J. Oliver
5. LVDS Owner’s Manual – National Semiconductor