February 2015 NSW Electronics design reviews
ART Data Driver Card

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Outline

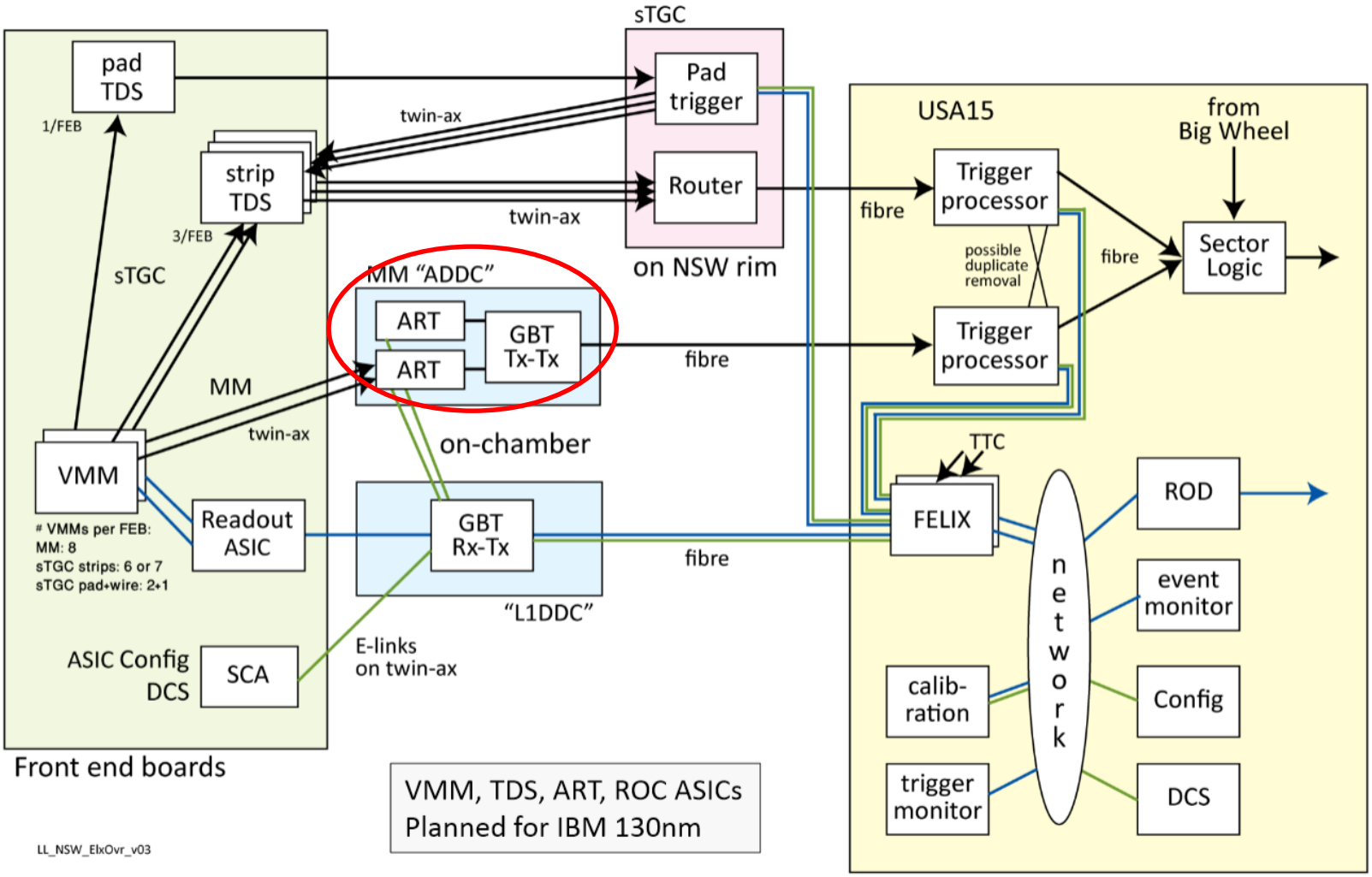
- Introduction
- ADDC Production Version Design
- ADDC Version 1 Prototype Design
- Time schedule and Manpower

ART Data Driver Card (ADDC)

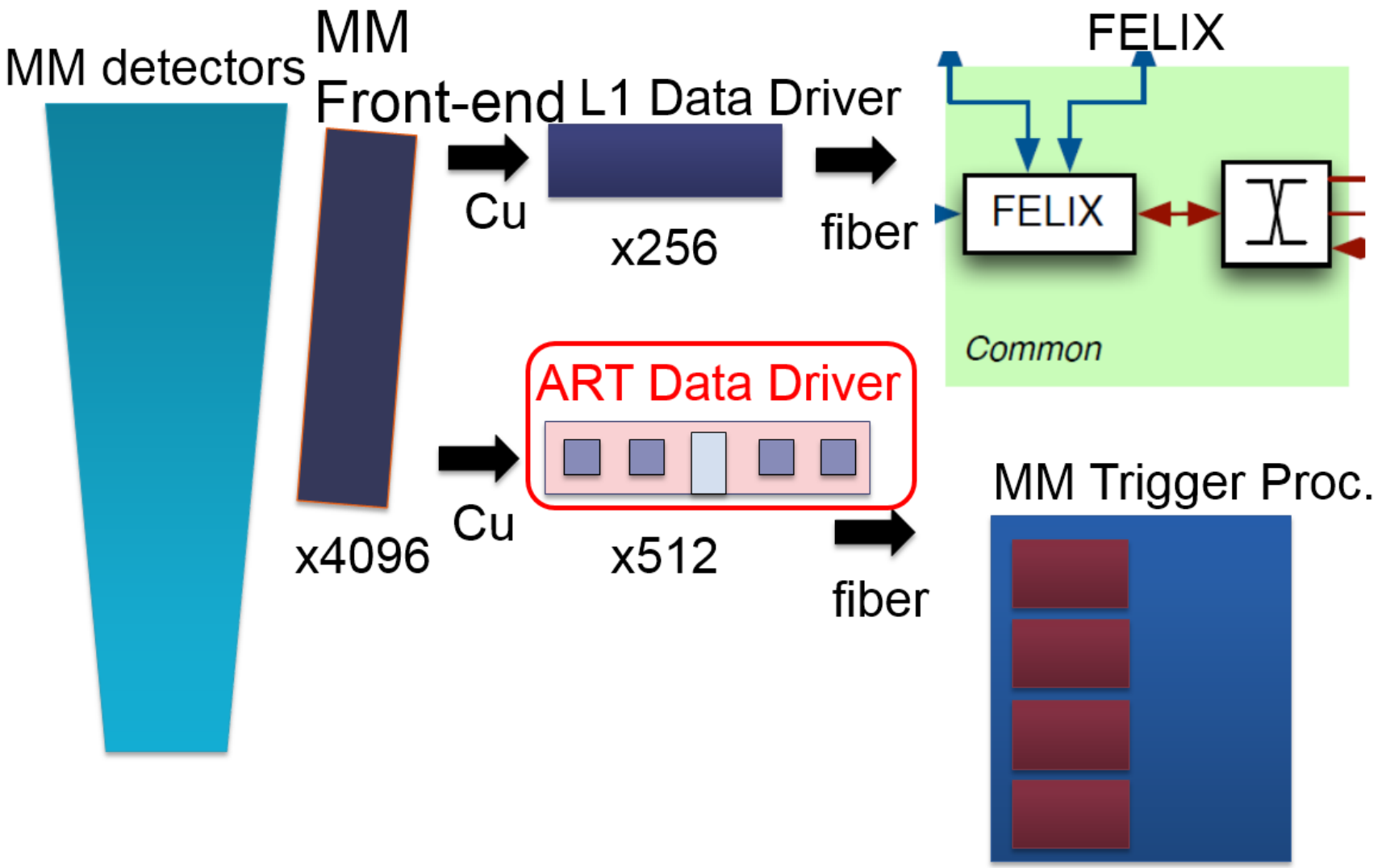
Introduction

Dataflow Overview

NSW Electronics Trigger & DAQ dataflow



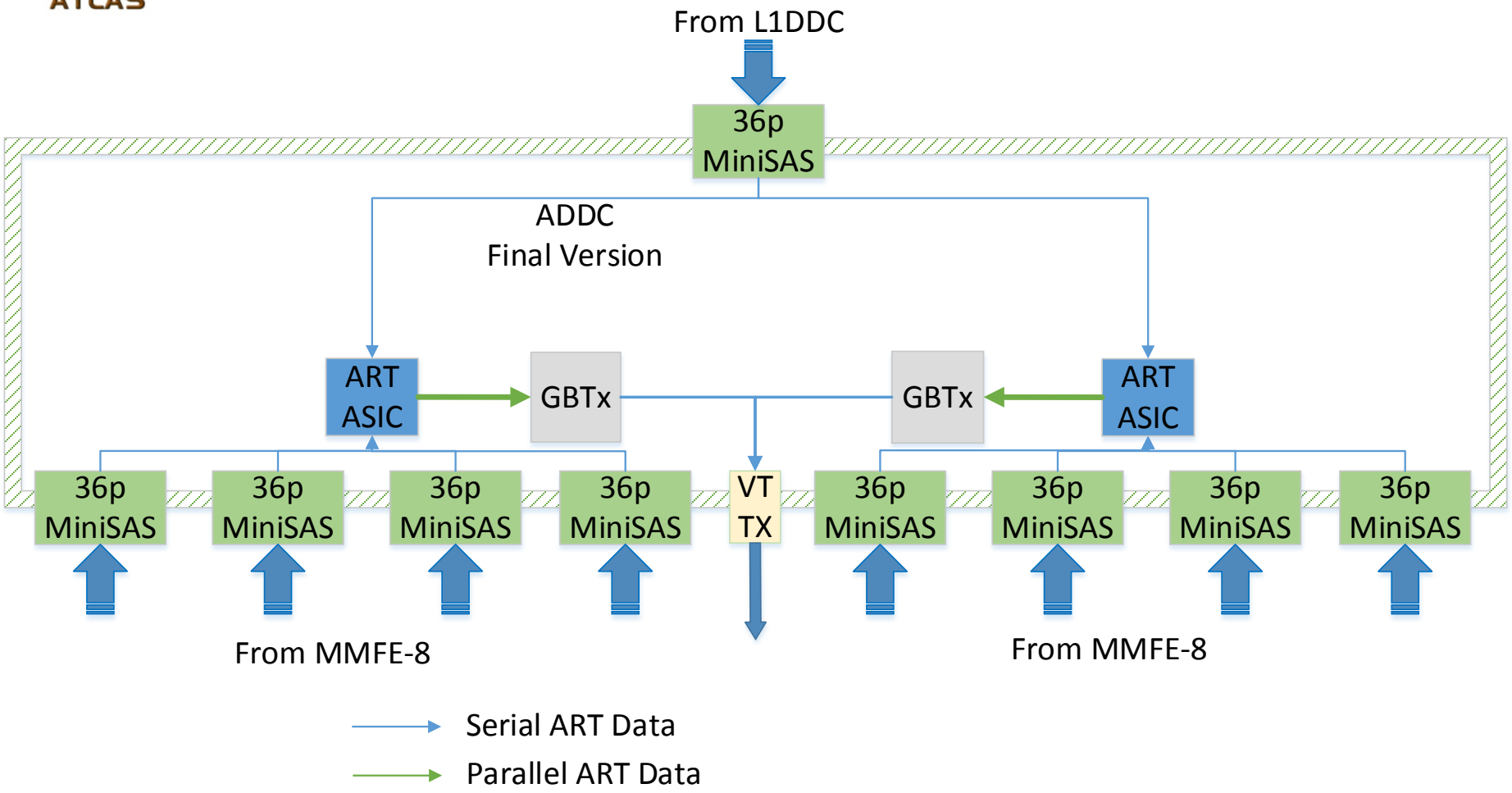
Boards connections



ART Data Driver Card (ADDC)

ADDC Production Version Design

ADDC Production Version Diagram



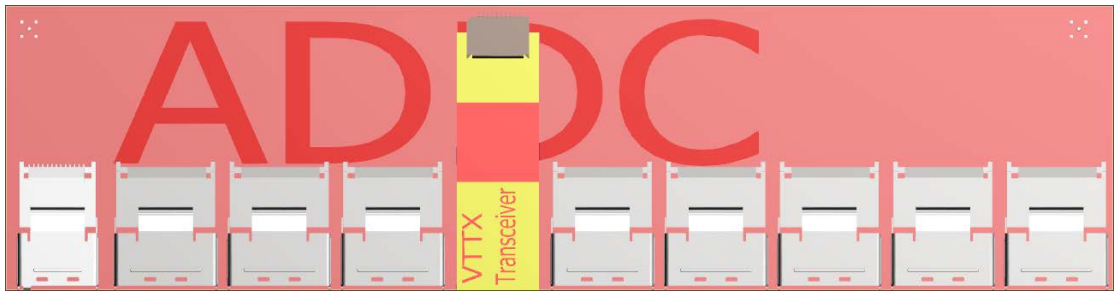
ADDC Production Version Diagram

- ART ASIC for processing, GBTx for transmission
  - 2 ART ASICs and 2 GBTx chips for each ADDC board
- Output interface
  - VT-TX: fiber connection
  - E-link: copper connection
  - 1 VTTX and E-link port for each ADDC board
- Input interface: 36p MiniSAS connector & cable
  - 9 MiniSAS connectors for each ADDC board, 8 for connections with 8 MMFE-8 boards, 1 for connection with L1DDC board

ADDC 3D view

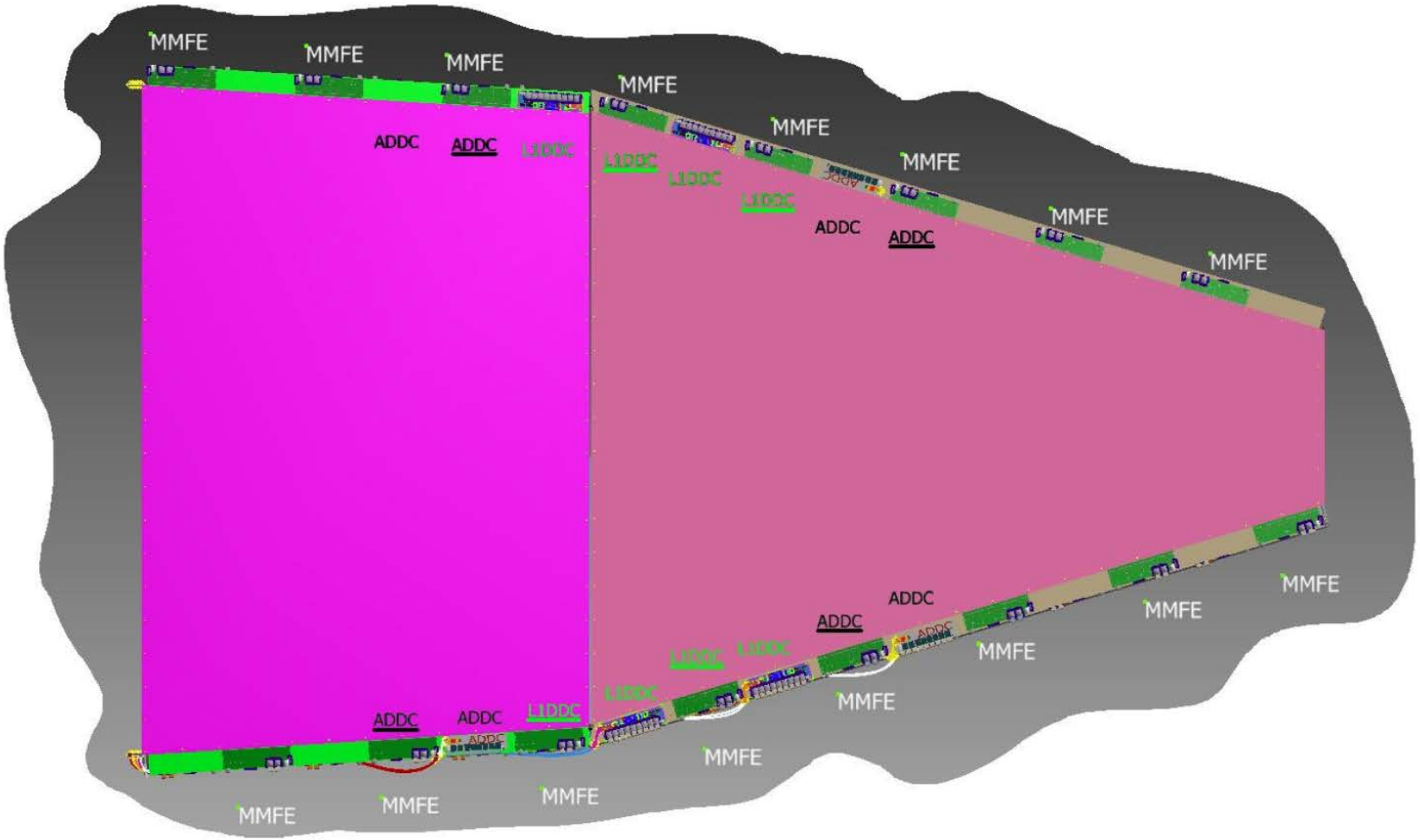
- Dimensions:
  - 200 mm x 50 mm
- Preliminary modeling, placement may be changed in later design
- The actual power chip choice in final design will be the same as the Front-End boards.

Top View



Bottom View

Micromegas wedge 3D model



ADDC on Micromegas wedge

- Underlined label signifies that placement of the boards is on the opposite (here not visible) side of the wedge

- Detailed positions and cable/fiber routing is not fully determined yet

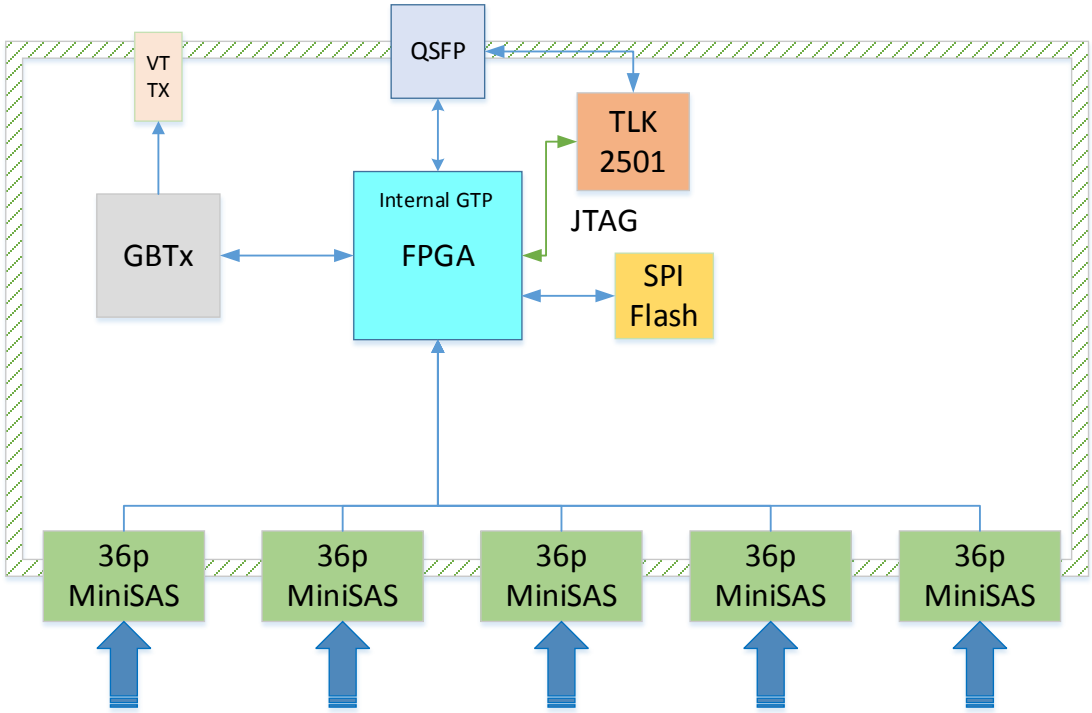
- The components need cooling are on the same side and will benefit from the cooling channel. The cooling solution will be common to all three on-chamber boards(MMFE, L1DDC, ADDC)

ART Data Driver Card (ADDC)

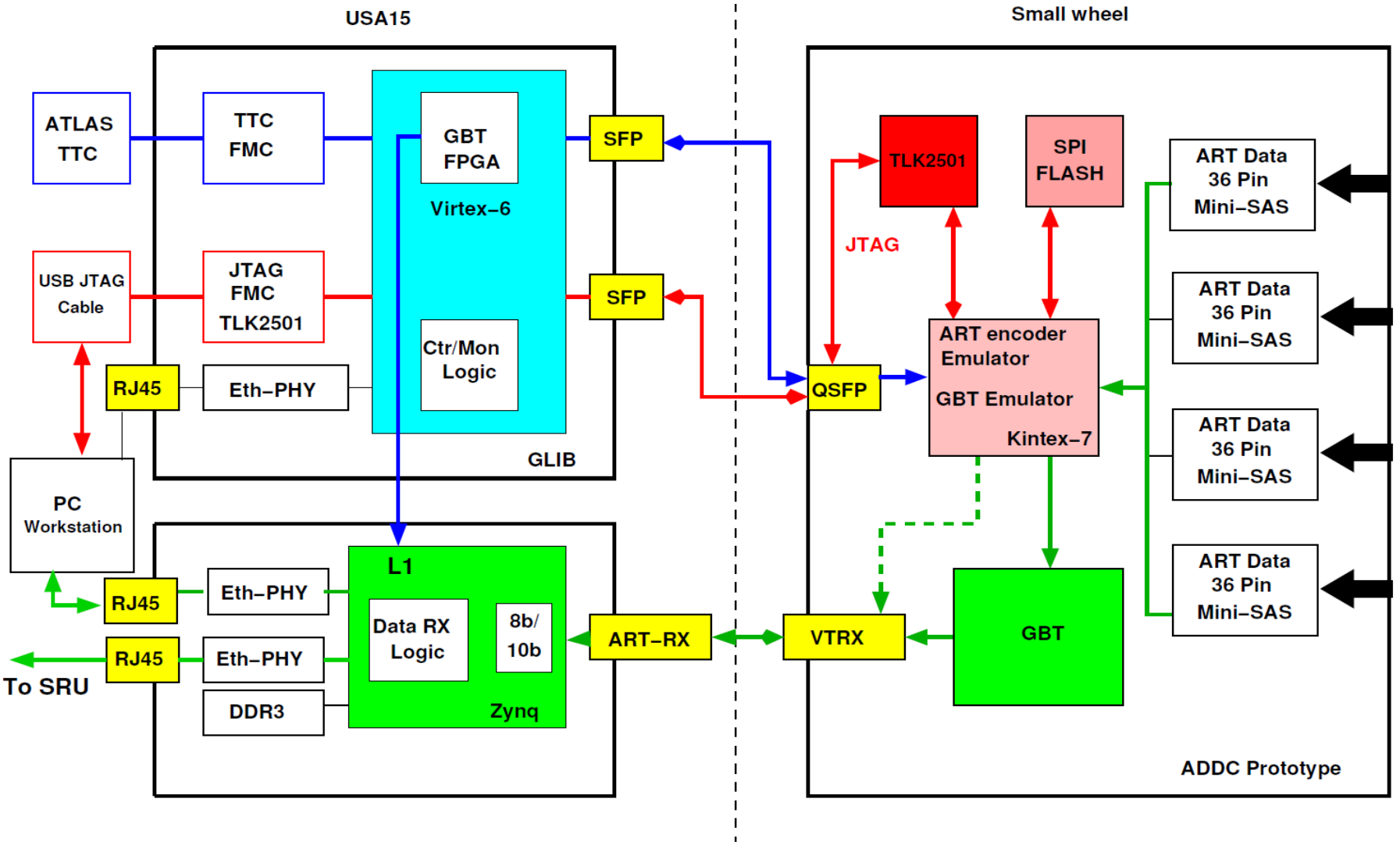
ADDC Version 1 Prototype Design

ADDC Version 1 (FPGA) Diagram

- FPGA is playing the role of ART ASIC
- 2 options for ART data output
  - GBTx transceiver
  - FPGA internal transceiver
- Remote configuration available

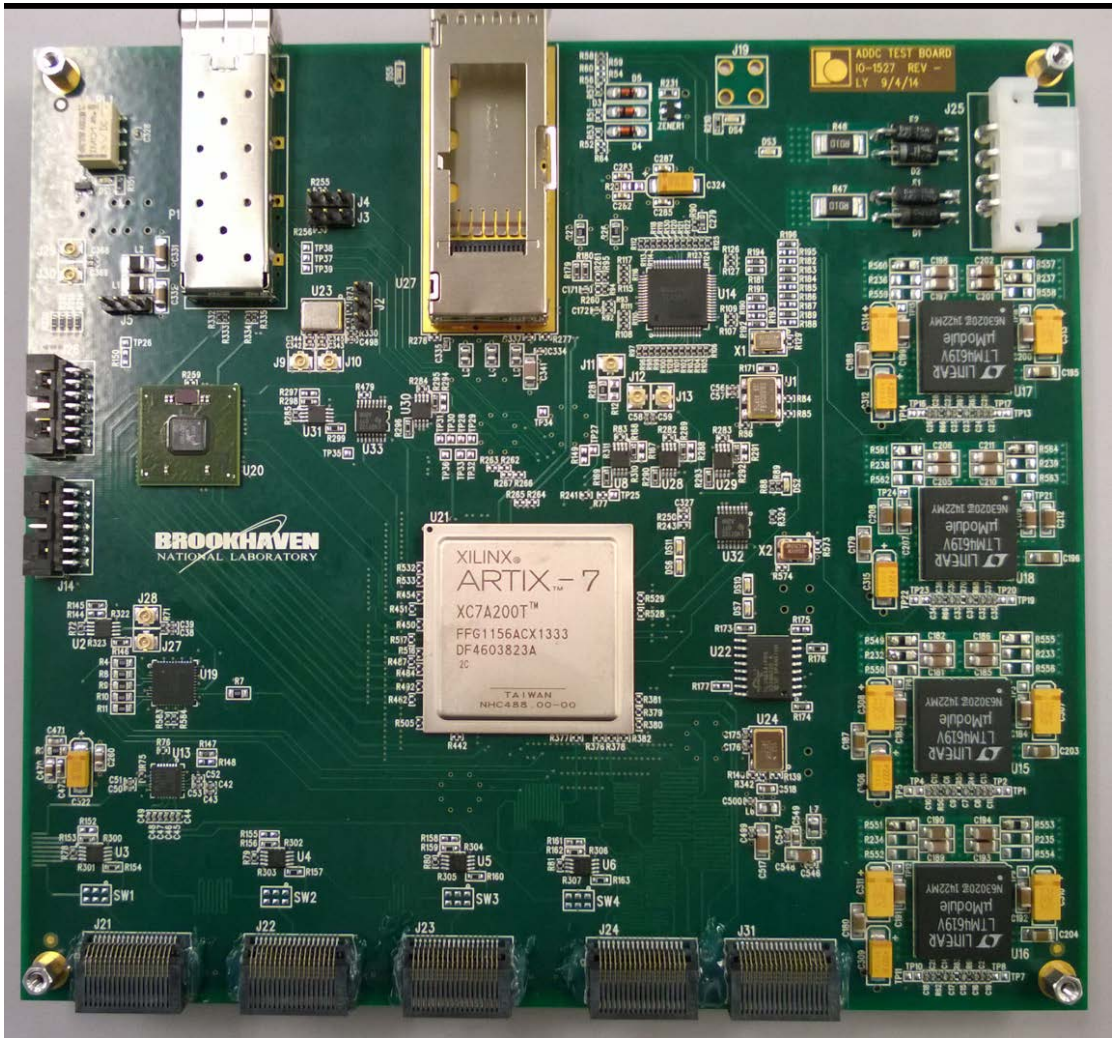


ADDC v1 prototype connections



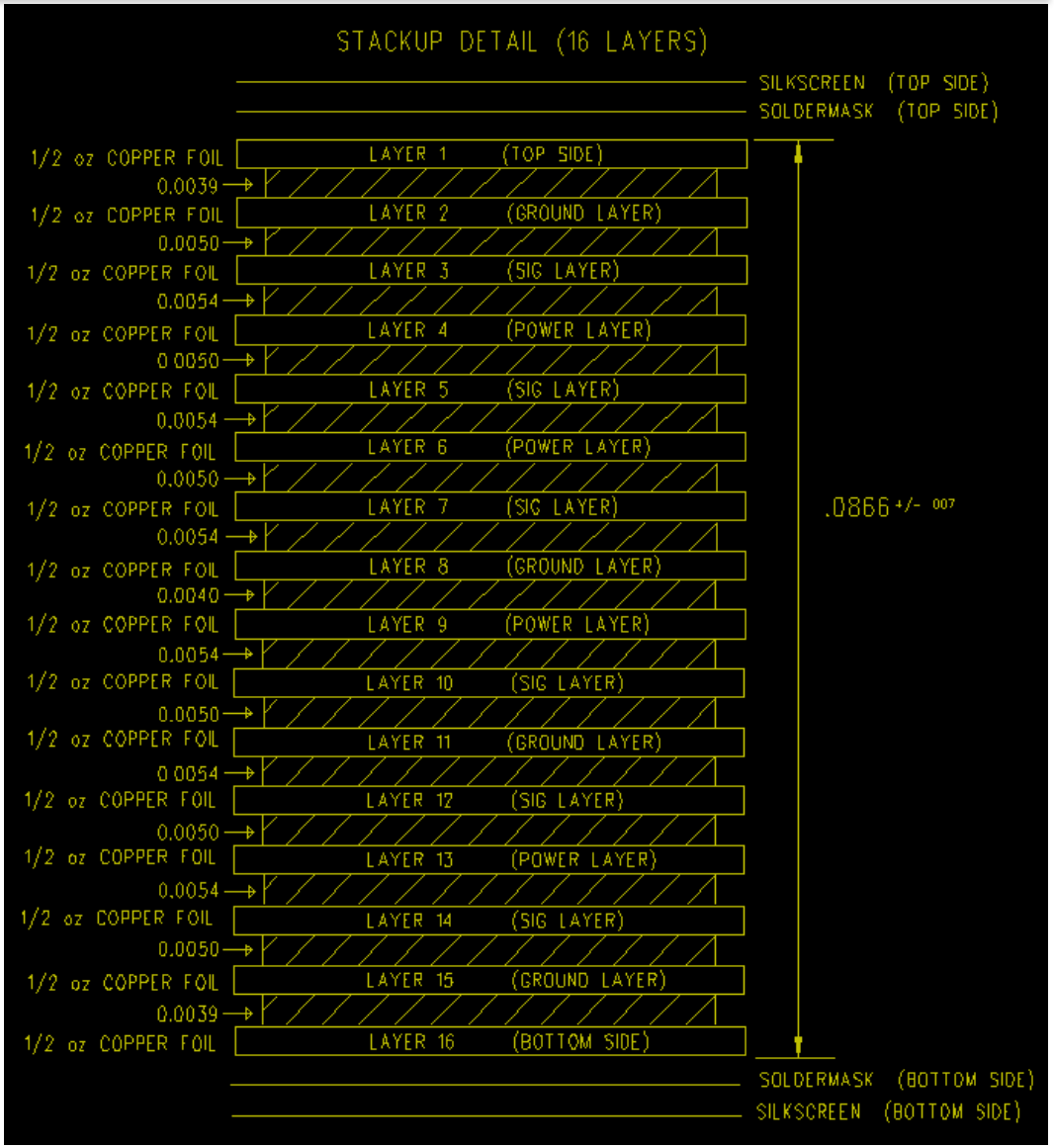
ADDC Version 1 Photo

- Dimensions:
  - 177.8 mm x 162.56 mm
- FPGA: Xilinx XC7A200T-2FFG 1156
- 4 LMT4619 power chips
- PCB material: FR4



PCB Stack-up

- 16 total layers
  - 8 signal layers
  - 8 power/gnd layers
- Thickness:2.2 mm(0.0866 inch)
- Differential pairs have a preset 4 mil width and 4 mil gap rule in design
- The actual width/gap is adjusted in fabrication to ensure the 100 ohm impedance

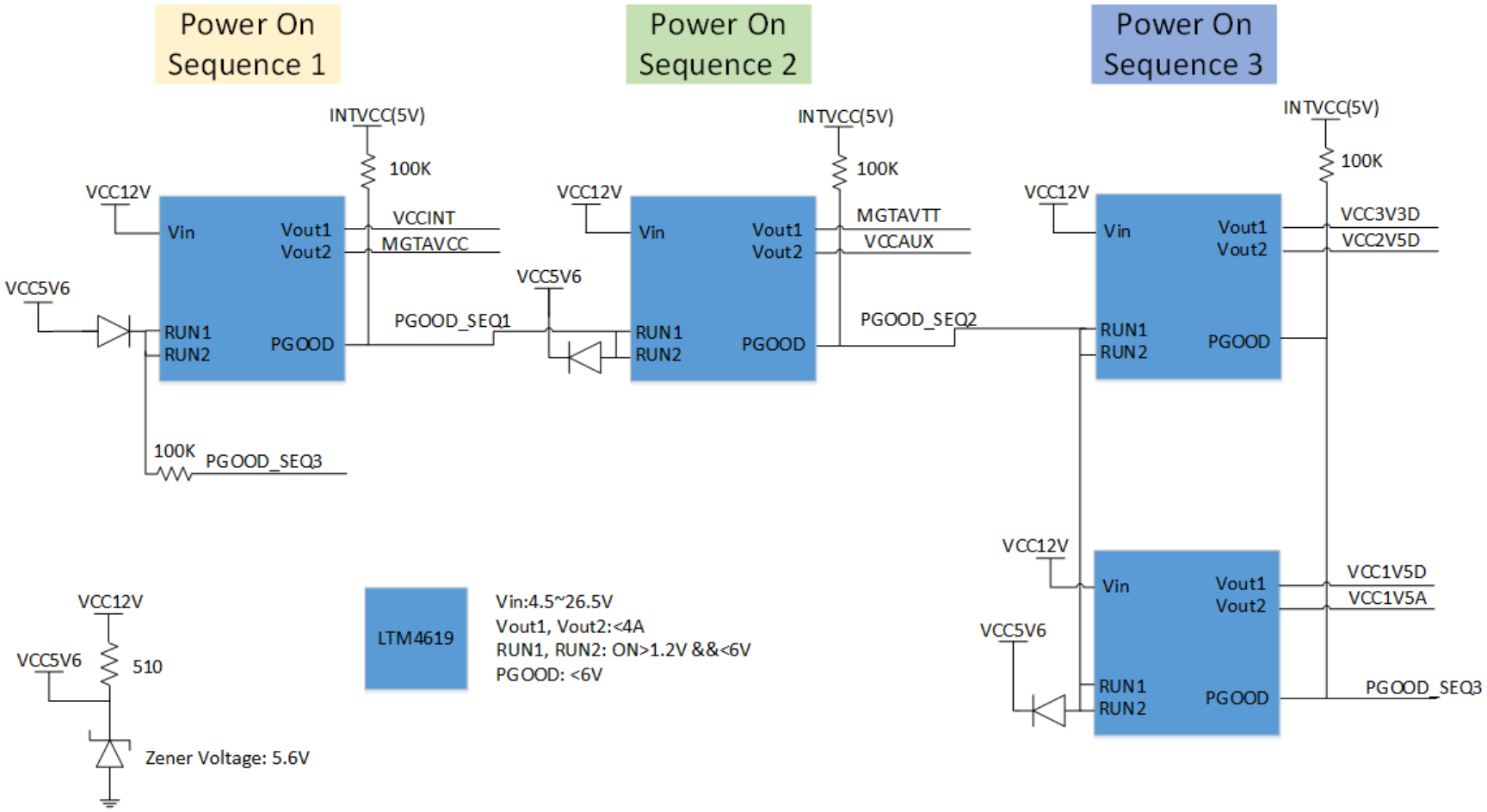


Power Estimation

- Considering the power chip efficiency, the total input power would be around 11.6 watt at 12V input, and around 10.57 watt at 5V input
- In the final ADDC board the power chip choice will be the same as the FEBs
- In final version the FPGA is waived, the power consumption will reduce to lower than 5 watt plus the power for the two ART ASICs

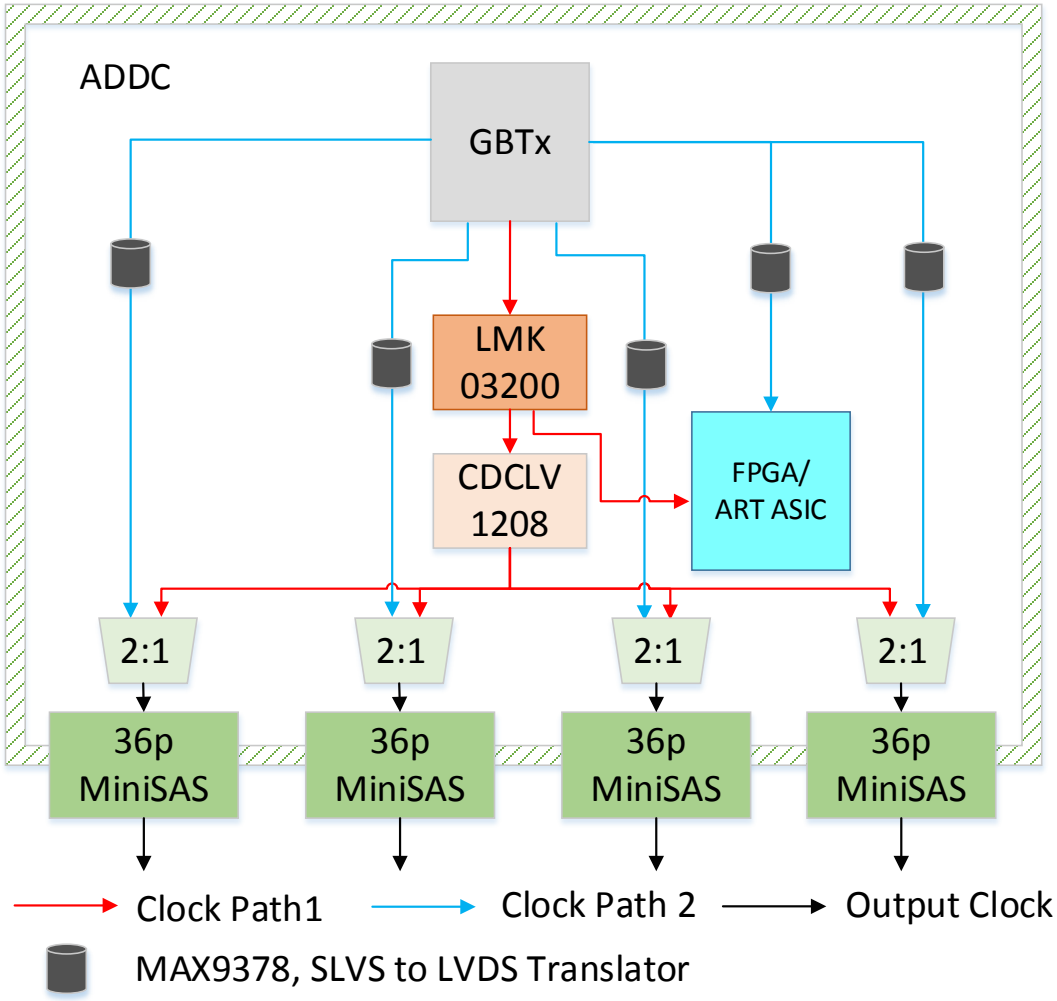
Power on Sequence	Power Chip Num.	Name	Output Voltage (V)	Current Consumption[1][2] (A)	LTM4619 Efficiency (Vin=12V)	Input Current (A)	Input Power (W)	LTM4619 Efficiency (Vin=5V)	Input Current (A)	Input Power (W)
1	1	VCCINT	1.0	1.239	80%	0.129	1.549	85%	0.292	1.458
		MGTAVCC	1.0	0.333	55%	0.050	0.605	65%	0.102	0.512
2	2	MGTAVTT	1.2	0.174	55%	0.032	0.380	60%	0.070	0.348
		VCCAUX	1.8	0.23	60%	0.058	0.690	70%	0.118	0.591
3	3	VCC3V3D[3]	3.3	0.823	85%	0.266	3.195	92%	0.590	2.952
		VCC2V5D[4]	2.5	0.723	80%	0.188	2.259	90%	0.402	2.008
	4	VCC1V5D[5]	1.5	1.218	82%	0.186	2.228	87%	0.420	2.100
		VCC1V5A[6]	1.5	0.279	60%	0.058	0.698	70%	0.120	0.598

Power on Stages for V1 prototype



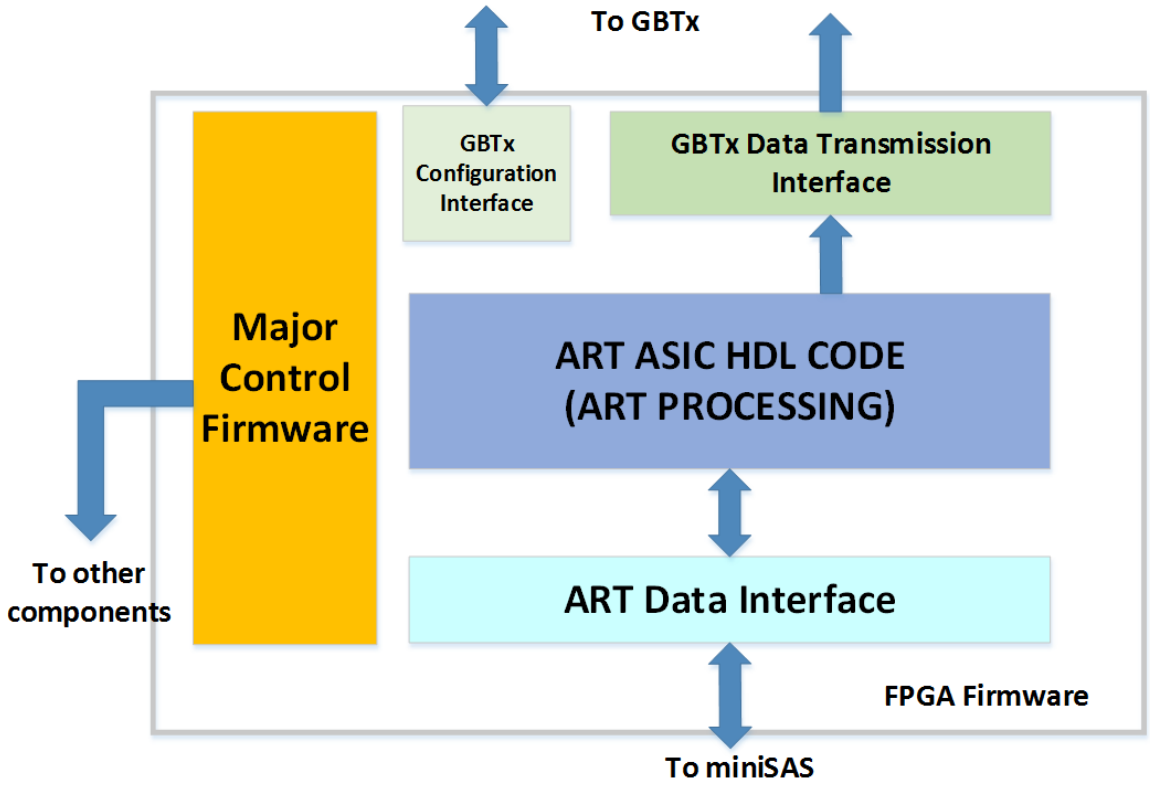
Clock Distribution Path

- The RX recovery clock from the GBTX chip will be the original clock source
- In future versions the clock from L1DDC board will be the clock source
- Two optional clock distribution path:
  - Directly through GBTx programmabler clock output
  - Through the LMK03200 clock chip and the CDCLV1208 fan-out chip



ADDC FPGA Firmware

- ART ASIC HDL CODE: ported from the ART ASIC with some modification to accommodate the FPGA features
- ART Data Interface: receive all the ART data and align them
- GBTx Data Transmission Interface : Communication with GBTx E-port
- GBTx Configuration Interface: I2C configuration for GBTx chip
- Major Control Firmware: interface for most of the rest onboard components



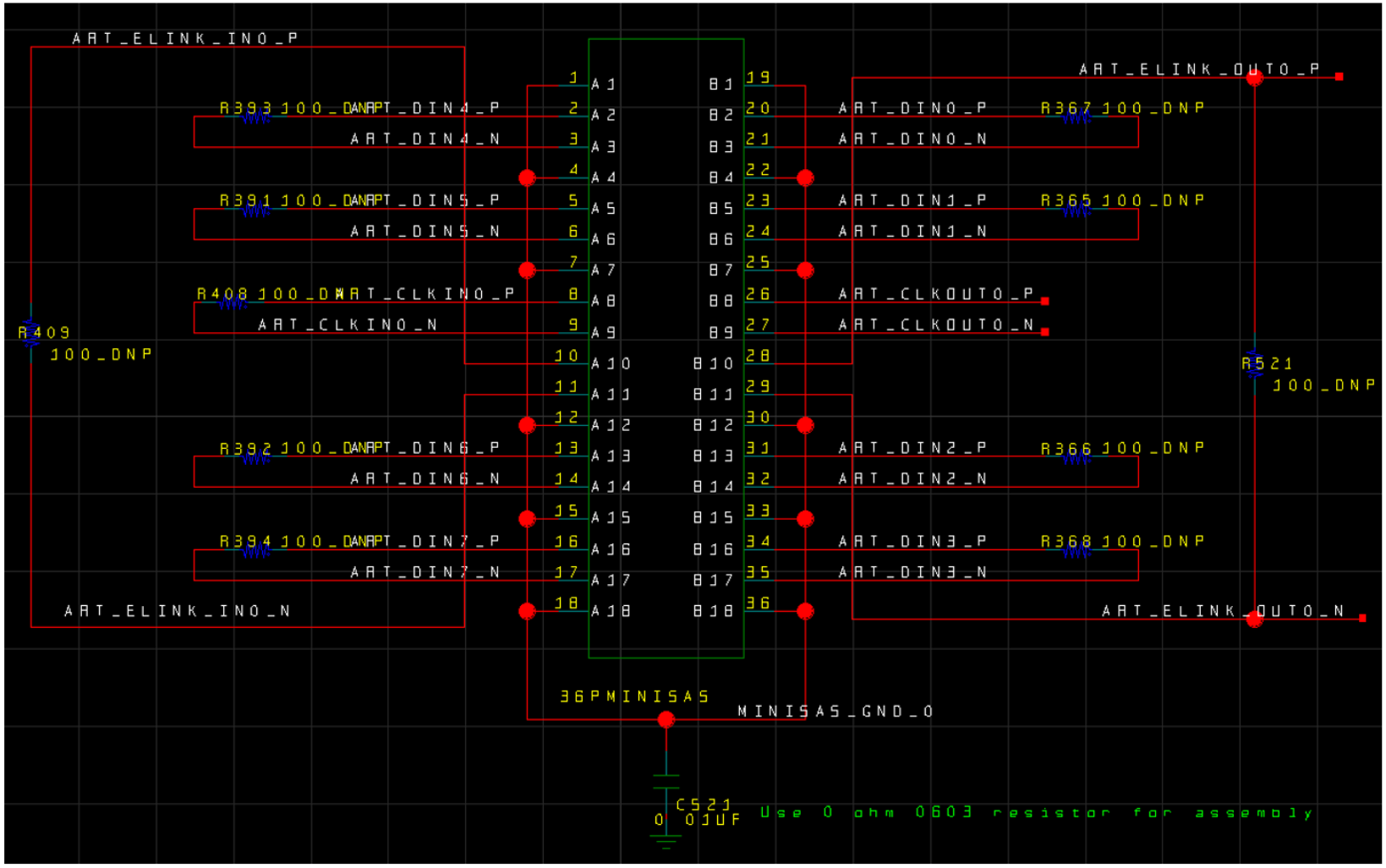
Interface with MMFE-8 boards

- Connector: MiniSAS 36 pin
- Number: 4 (version 1), 8 (final)
- Part Number: Molex 75783-0125
- Cable: 3M 8F36-AAA105-0.50

- Data Format:
  - 8 channels ART data, all inputs, 160 Mbps
  - 1 channel 160 MHz downlink clock (from ADDC to MMFE-8)
  - 1 channel 160 MHz uplink clock (from MMFE-8 to ADDC)
- Communication standards:
  - VMM Customized LVDS for ART data (600 mV +/- 150mV)
  - LVDS for clocks

MiniSAS cable & connector

Interface with MMFE-8 boards



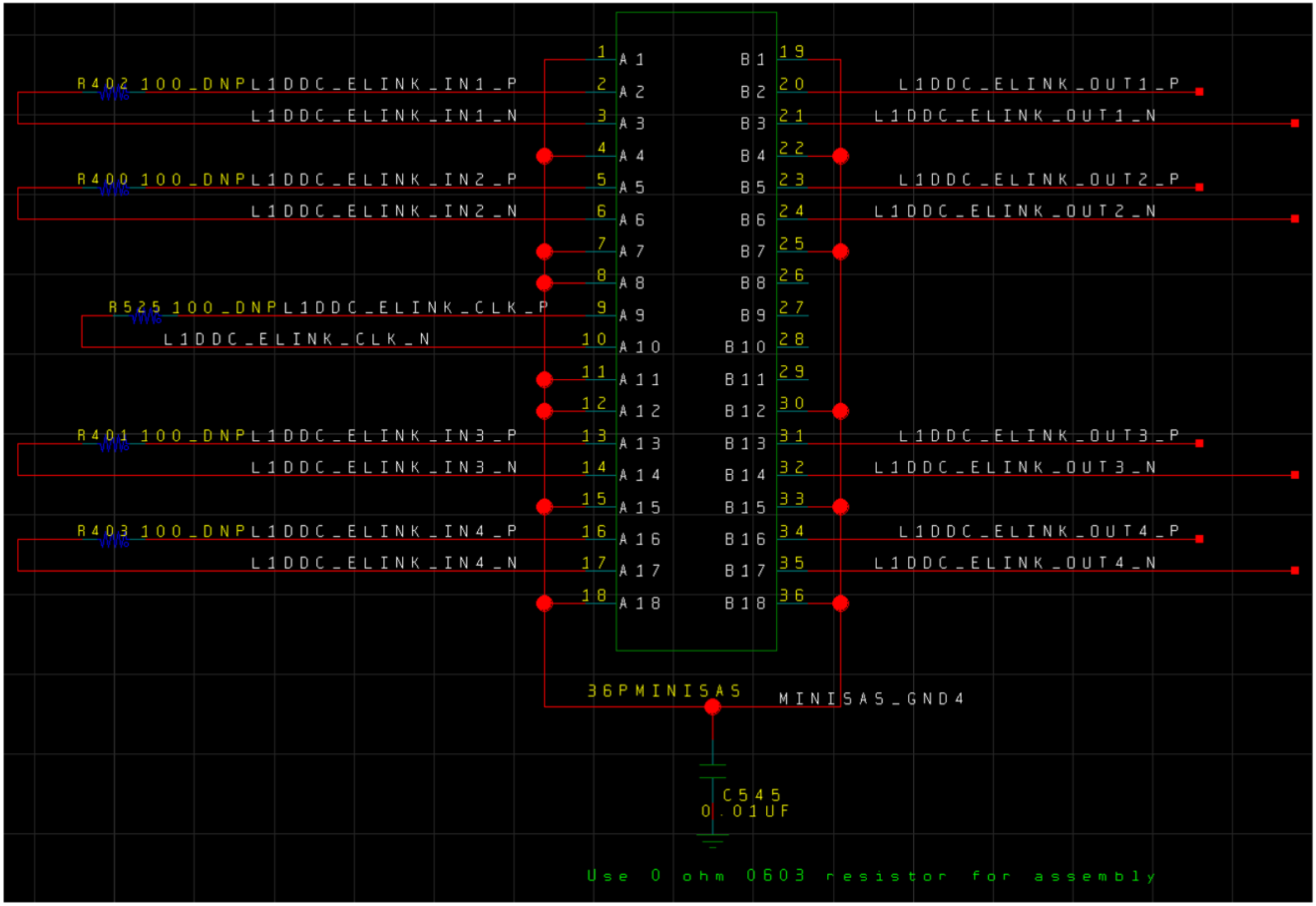
Interface with L1DDC boards

- Connector: MiniSAS 36 pin connector
- Number: 1
- Part Number: Molex 75783-0125
- Cable: 3M 8F36-AAA105-0.50

- Data Format:
  - 8 channels data, 160 Mbps (4 inputs, 4 outputs)
  - 1 channel 160 MHz clock (from L1DDC to ADDC)
- Communication standards: LVDS

- As required by the NSW Grounding rules, all the LVDS cables will be DC coupled to the ADDC prototype board ground through the MiniSAS connector

Interface with L1DDC boards



Interface with trigger processor

- Connector: Commercial SFP+ module (VTTx module will be used in future design)
- Number: 1
- Part Number: Avago AFBR-709SMZ
- Data Format: 4.8 Gbps serial data

Avago AFBR-709SMZ SFP+ Module

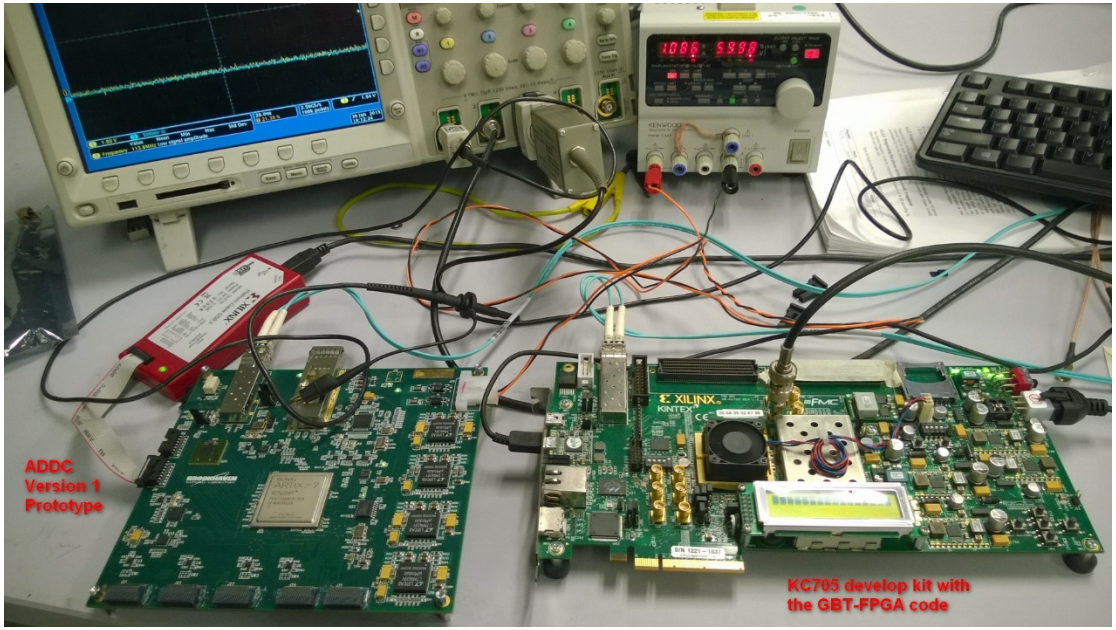
ART Data output format

- GBTx running under WideBus mode, 112 available bits
- HIT_CNT[3:0] = number of hits (range 0 - 8; 9 - 15 invalid)
- VMMIDx[4:0] = VMM channel ID (0..31)
- ARTDATA_PARITY[7:0] = parity bit of the ART data computed by each of the 32 ART de-serializer units. Each bit corresponds to one of the ART data field selected by the priority unit.
- ARTDATAx[5:0] = 6-bit ART addresses

GBT[111:108]	GBT[107:96]	GBT[95:56]	GBT[55:48]	GBT[47:0]
HIT_CNT[3:0]	BCID[11:0]	8xVMMIDx[4:0]	ARTDATA_PARITY[7:0]	8xARTDATAx [5:0]

Tests on version 1 prototype

- Some initial tests and data communication tests have been performed
- The Xilinx KC705 develop kit with GBT-FPGA 3.0.1 is used to communicate with ADDC v1 prototype



Tests on version 1 prototype

- The power chips and clock chips are working well
- The configuration of GBTx chip through I2C bus works.
- The e-port communication between GBTx and FPGA works well, the FPGA could recognize the GBTx SLVS output signals directly without the help of level translator chips.
- The programmable clock output feature of GBTx chip is tested, it could be configured correctly and the clock output is working as expected.

Tests on version 1 prototype

- A PRBS loop-back test has been performed with a KC705 develop kit and the GBT-FPGA code.
  - The data link is: KC705 FPGA→2 meter fiber→ADDC GBTx→ADDC FPGA→ADDC GBTx→2 meter fiber→KC705 FPGA.
  - The received PRBS data is compared with the sent data in KC705 FPGA.
  - No data error is observed within 24 hours test.

- An initial communication test with MM Trigger Processor prototype has been performed. Preset data is loaded into the ADDC FPGA, the MM Trigger Processor prototype have received and recognized the preset data from the receiver end.

- Currently we do not have a plan to do the radiation test for the version 1 prototype

Future testing plan on final boards

- Preset data will be fed to the MiniSAS connector as input
- Output result will be checked in the receiver end

- A card will be considered good if it meets the following requirements:
  - All preset events could be recognized correctly during the test.
  - No missing event or extra fake event found.
  - No bad codes seen in 10 minutes of running.
  - ART Data transmissions are stable during the test.
  - Current consumption within acceptable window (to be determined based on detailed testing of an initial batch).

- Some boards will be picked out randomly for long-term test and radiation hard environment test to evaluate the long-term stability.

ART Data Driver Card (ADDC)

Time schedule and Manpower

Time schedule

- Apr. 2015 ~ Jan. 2016: ADDC v2 prototype design, fabrication and testing
- Feb. 2016 ~ Nov. 2016: ADDC v3 prototype design, fabrication and testing
- Dec. 2016 ~ Feb. 2017: ADDC final version design
- Mar. 2017: ADDC production readiness review
- Apr. 2017 ~ Sep. 2017: ADDC final version fabrication and testing
- Aug. 2017 ~ Oct. 2017: Ship ADDC to CERN

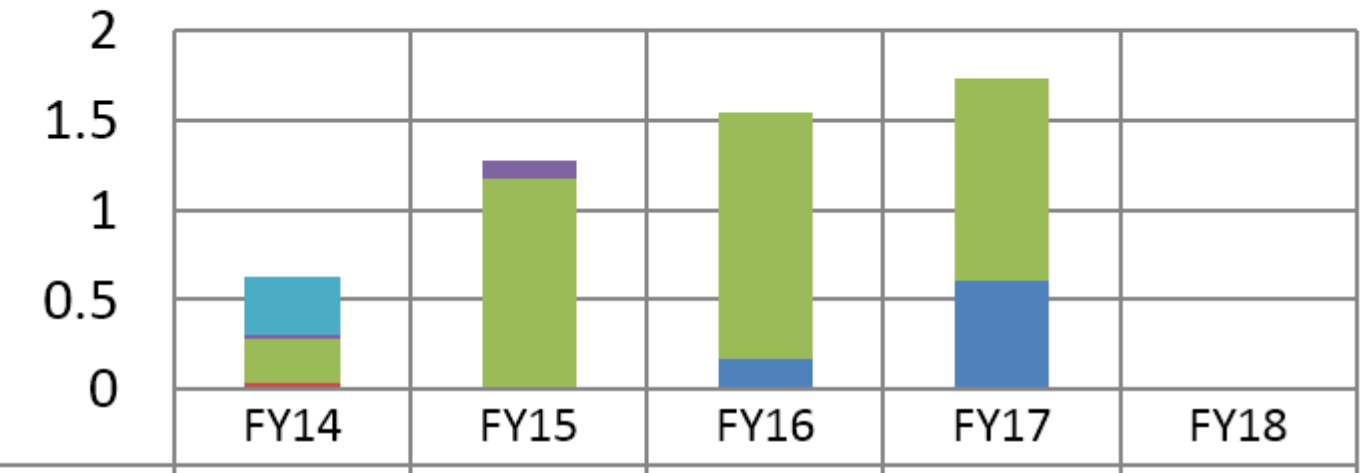
- Prototype 2: Designed with the ART ASIC sample chip
- Prototype 3: An improved design of prototype 2 with issues fixed

- The testing and shipment of final ADDC boards will be carried out gradually, first batch of the boards will be available in Aug. 2017 and all boards will arrive at CERN no later than Oct. 2017.

Manpower

- Dr. Sorin Martiou and his group in IFIN-HH Bucharest will be responsible for the design of ART ASIC
- The production of ART ASIC will be together with the VMM chip
- The design and fabrication of ADDC prototypes and final boards will be in Brookhaven Lab. Dr. Lin Yao is the main engineer working on the ADDC.

BNL FTE chart for ADDC



	FY14	FY15	FY16	FY17	FY18
ENGR (Act. through 4/2014)	0.32				
U-Stu	0.03	0.10			
Postdoc	0.24	1.17	1.37	1.12	0.01
Engineer	0.03				
Student			0.18	0.61	