NSW Electronics
Preliminary Design Review

Pad Trigger Logic Board

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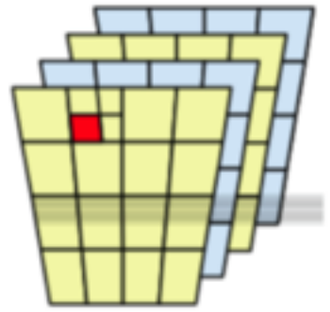
sTGC Trigger Main Tasks

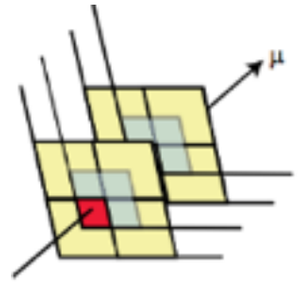
- Select muons coming from the interaction point.
- Elaborate strip and wire information off-detector.
- Minimise the bandwidth to the off-detector trigger processors.
- Send off-detector only strip information coming from the regions where a muon was detected.
- Perform coincidence of detector Pads to select interesting regions.

sTGC Trigger Detector Segmentation

- 16 sTGC sectors per NSW wheel.
- Each sector is divided in inner, middle and outer region.

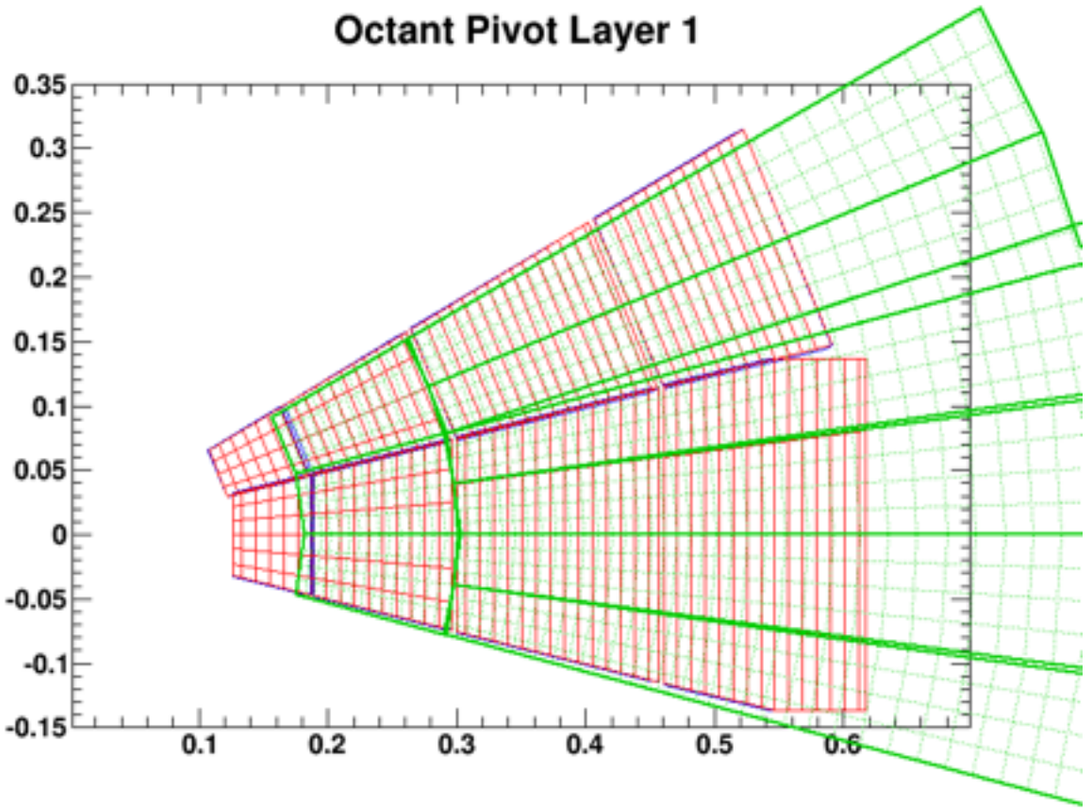


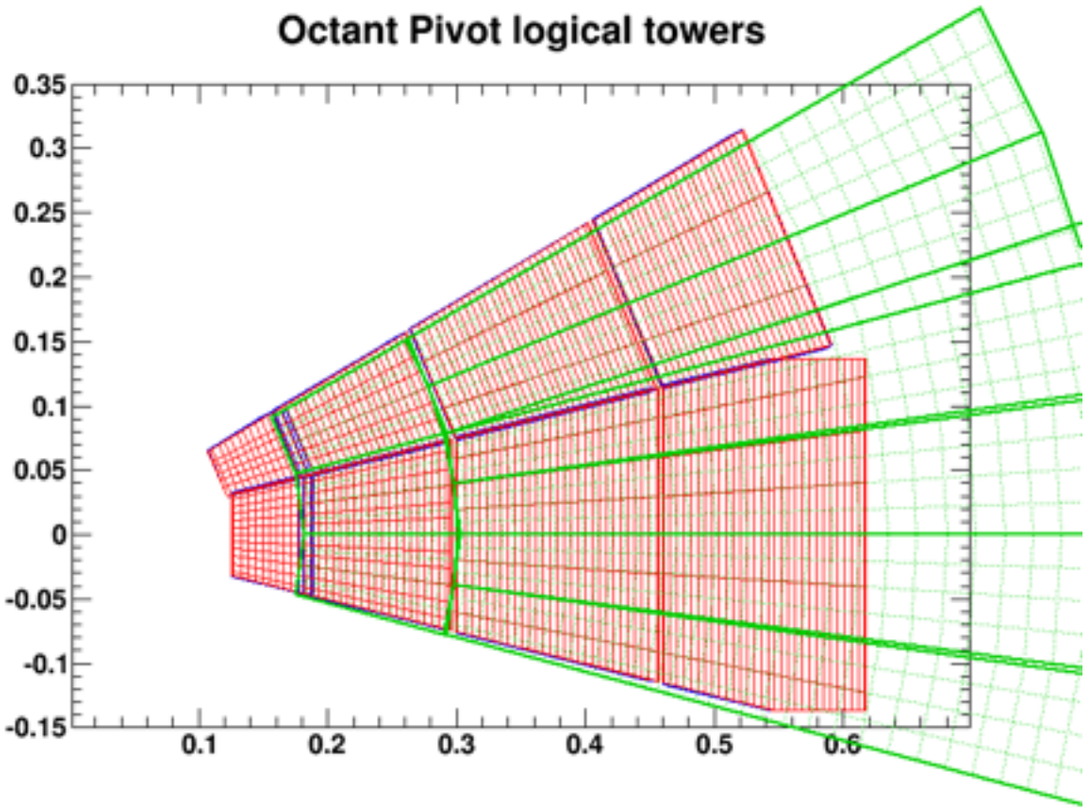
- 2 sTGC quadruplets (pivot + confirm) per sector.
- 4 layers of Pads and 4 layers of strips per quadruplet.



- Pads are staggered by half length in eta and phi on the 4 layers.
- A logical Pad is defined by the projection of the physical Pads in the different layers (1/4 of the Pad area).
- "Fuzziness" positioning is added in the last two layers of one quadruplet to minimise the number of Pads to be put in coincidence in a trigger tower.

sTGC Physical Pads and Logical Pads

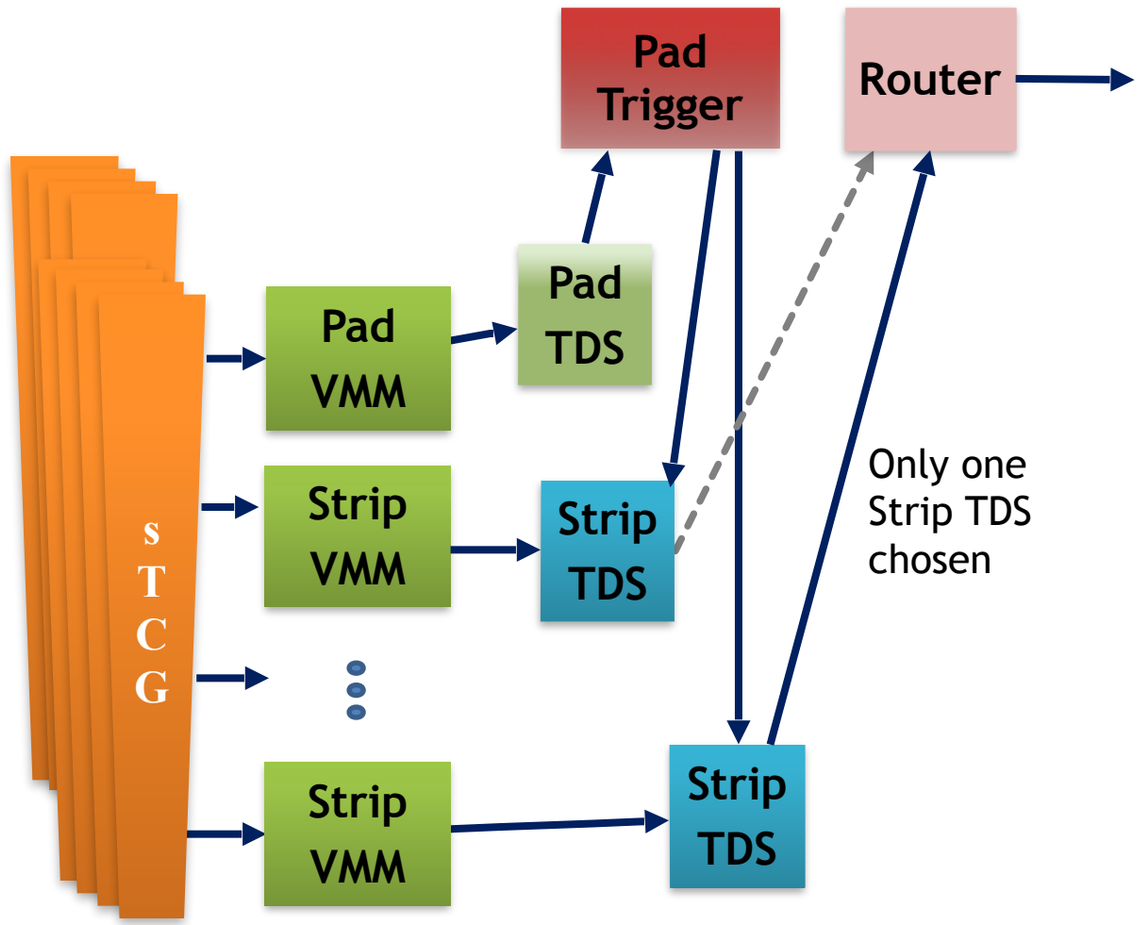




- Full system is composed by about 45000 physical Pads.

sTGC Trigger Logic

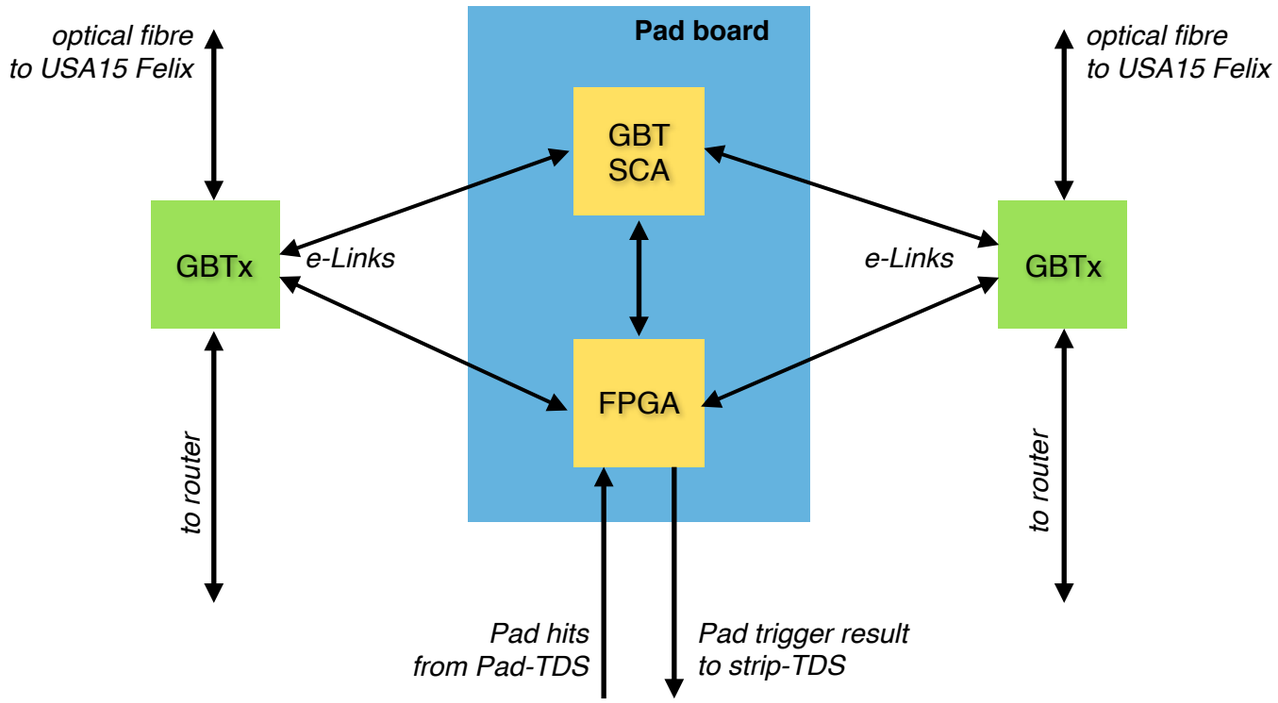
- Find a Pad hit coincidence in a tower of logical Pads within one Bunch Crossing.
- 3/4 majority logic is required on both sTGC quadruplet.
- Candidate geometrical coordinates and BCID sent to the front-end strip-TDS chips.
- Strip-TDS sends only selected strip data to the routers.



Pad Trigger Logic Board

- 16 Pad trigger logic boards on the rim of one wheel (1 per sector), for a total of 32 boards.
- Pad hit data from front-end Pad-TDS.
- 3/4 majority on each of the two sTGC quadruplet.
- The trigger candidates are associated with their strip band ID and phi coordinates and with their relative BCID.
- Up to 3 trigger words are sent every BC, one per detector region (inner, middle, outer) to the front-end strip-TDS chips.
- Readout logic is performed as well when a L1A is received.

Pad Board I/O signals



- Bi-directional: GBTx E-links from 2 GBTx (total number of E-links to be defined, most probably 1-2 for the clock(s), 1 for the GBT-SCA, 1-2 for the readout, so up to 5 E-links per GBTx).

- Input: sTGC Pad hit signals from front-end Pad-TDS chips (24 serial lines on TwinAX cables).

- Output: Pad logic trigger result (up to 3 trigger candidates) to front-end strip-TDS chips (5/6 serial lines on TwinAX cables).

- All I/O signals make use of differential LSVS or LVDS standards.

Pad Board GBT signals

- 2 GBTx chips per Pad board are foreseen for redundancy.
  - probably shared with the adjacent Router boards.
  - to be decided whether GBTx on the Pad board or not.
- GBTx provides TTC signals (CLK, L1A, BCR, ECR).
- GBTx used for board configuration/monitoring, in association with a local GBT-SCA chip.
- GBTx used for readout/busy/monitoring data through the Felix system.

Pad Board Trigger Signals

- Pad hits inputs: 24 serial differential lines on TwinAx cables, one per each Pad-TDS chip in one sector.
  - One Pad-TDS chip sends up to 96 Pad hits per BC each BC on one serial line.
  - Data format: 120 bits every BC, 4x30-bit packets, 4-bit header + 96-bit Pad hits + 12-bit BCID + 8-bit CRC.
  - Data transfer: 4.8 Gb/s.
- Pad trigger outputs: up to 3 trigger words (inner, middle, outer regions) sent each BC to the front-end strip-TDS chips on TwinAx cables.
  - Data format: 12-bit BCID + 8-bit road ID + 5-bit phi ID (BCID is common, 51-bit for 3 candidates).
  - Data transfer: last proposal 640 Mb/s (16-bit per BC, 320 MHz DDR) on 5 serial lines (3 data lines + 1 clock line + 1 frame line)

Pad Board Components

- FPGA + flash memory:
  - Xilinx Kintex-7 family.
  - A possible candidate is the XC7K355T, -1/-2 speed grade, FFG901 package type.
  - 24 GTX serdes blocks (max data rate 8.0 Gb/s), 300 HR I/O banks (LVDS max speed 625 Mb/s SDR, 950 Mb/s DDR).
  - The FPGA internal clock frequency: 240 MHz or 320 MHz.
  - We are exploring the possibility to use more powerful devices (Kintex-7 Ultrascale family) which would allow higher frequency clocks, to reduce the total latency.
- 1 GBT-SCA chip (I2C and JTAG protocols).
- 2 GBTx chips (it has to be decided whether they will be on the board or not).
- TI DS100BR410 booster quad chips, used to equalise signals coming from the Pad-TDS chips and to compensate for channel loss (this chip has negligible latency and very low power consumption).
- Voltage regulators, used to be able to independently power on/off all chips on the boards;
- Temperature and voltage monitor chips.
- MiniSAS connectors for TwinAX cables.

FPGA Trigger Logic

- Each BC the sTGC Pad hit serial data is sampled, deserialised and BCID tagged:
  - 4.8 Gb/s per serial line = 120 bit @ 40 MHz ➜ 20 bit @ 240 MHz from each GTX.
  - GTX can deserialise data with 10, 16, 20, 32, 40 bit packets.
- The trigger logic is based on coincidence windows to look for a 3/4 majority on each of the two sTGC quadruplet.
- The trigger candidates are associated with their strip band ID and phi coordinates and with their relative BCID.
- The trigger logic is performed independently and simultaneously on three sTGC regions (inner, middle, outer), so that up to three independent trigger words can be produced.
- The output trigger word is then serialised and sent to the front-end strip-TDS chips:
  - Kintex-7 OSERDES serialisers, 640 Mb/s (320 MHz DDR) per line (14-bit max per word).
- A local fan-out on the front-end boards may be needed to transmit the trigger data to all strip-TDS chips.

FPGA Readout Logic

- The sTGC Pad hit info are sent to the readout logic every L1A, through GBTx.

- Data packets can include error/monitoring words, SEU information, busy signal.

- Bandwidth and number of GBTx E-Links to be used to be evaluated.

FPGA Latency

- Latency calculation for a 240 MHz clock and a 20-bit GTX deserialisation word:

  a) time needed to sample and deserialise the input 120-bit Pad hit data: 40 ns;

  b) time needed to perform the trigger algorithm: 8 clock cycles = 34 ns;

  c) time needed to serialise the trigger output word: 16-bit @ 640 Mb/s per serial line = 25 ns.

- In this particular case the total latency is about 100 ns.

  - Total latency could be reduced with a higher clock frequency.

  - “c)” contribution may be reduced if more parallel lines are used.

Radiation Tolerance

- The radiation dose cumulated in 10 years of LHC running at a luminosity of $5x10^{34}$ $cm^{-2}s^{-1}$ is 84 Gy (TID) and 1.4×10^{12} p/cm^2 (safety factors included).

- Aim to use already certified devices.

- The FPGA actions against SEUs:

  - triple majority logic for the most important registers;

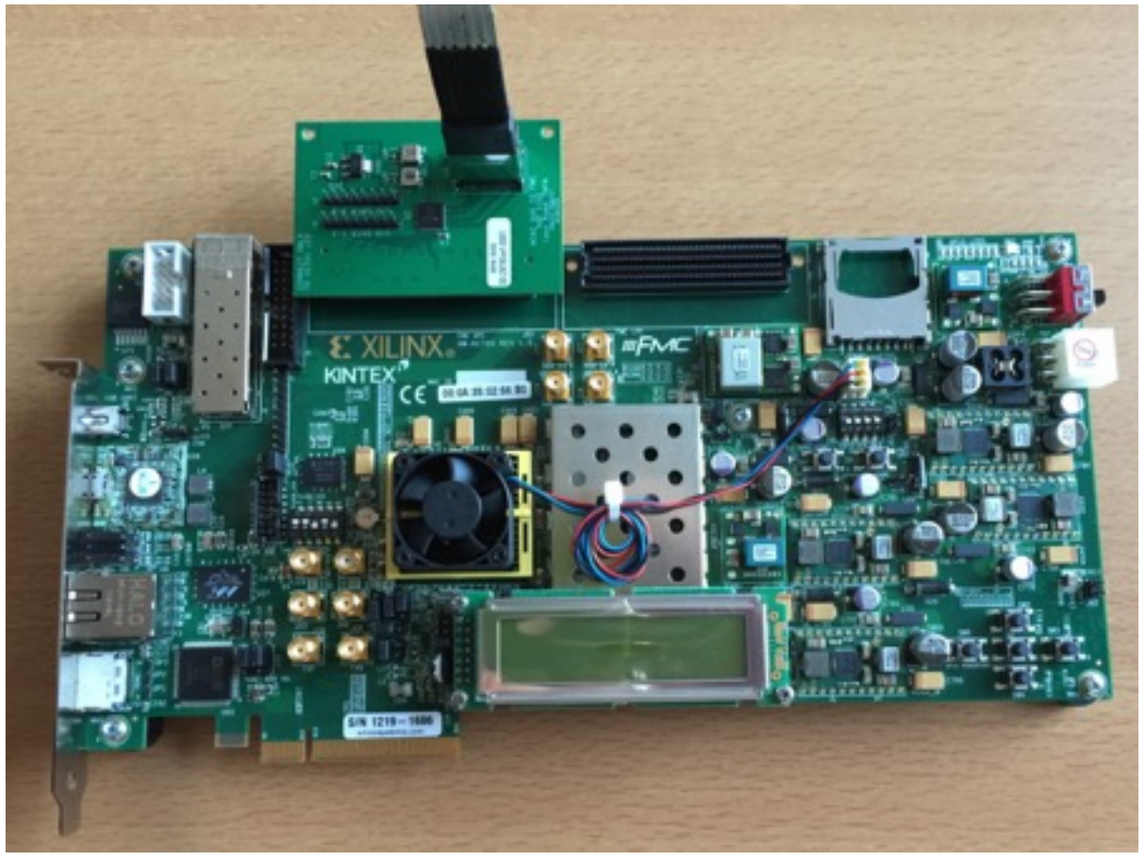
  - software/DAQ controlled FPGA/board reconfiguration/power cycle when a SEU is detected.

- The SEU foreseen rate (up to the Phase-II LHC luminosity) has to be evaluated to estimate the required rate of FPGA reconfiguration and the consequent data taking dead time.

Board Dimensions, Cooling, Power supply

- Evaluation board: Xilinx Kintex-7 KC705
- Dimension guess based on the evaluation board size: 30 x 20 x 5 cm.
- Power line per Pad board: 12V or 5V.
- Power consumption: assumption not to exceed 10 W.
- Cooling system may be needed for the FPGA (not desirable).

Test Setup



- Xilinx Kintex-7 evaluation board + TwinAx cable adaptor board hosting one TI DS100BR410 booster chip:

  - firmware (based on Xilinx embedded microprocessor) and software in order to configure the booster chip and to access the KC705 FPGA's internal registers via RS232 protocol.

  - This test setup will be used to prove I/O data transmission and protocol feasibility over the TwinAx cable and basic trigger algorithm logic.

Time Schedule

- Rome and Naples INFN groups are involved so far.

2015 Feb.	Preliminary Design Review
2015 Dec.	First Pad board prototype
2016 May	Final Design Review
2016 Sep.	Second Pad board prototype
2017 Apr.	Production Readiness Review
2017 Jun.	production of the 32 Pad boards + 4/5 spares
2017 Sep.	installation and commissioning

Conclusions

- No showstoppers detected so far.
- I/O data format to be defined as soon as possible.
- FPGA cost evaluation within next year to define final device.
- Power supply and cooling to be defined.
- Components radiation tolerance to be investigated.