The NSW Trigger Processor Overview

Preliminary Design Review

João Guimarães da Costa
Harvard University

(for the NSW Trigger Processor Working Group)

NSW PDR - CERN

February 13, 2015

https://indico.cern.ch/event/354058/

Agenda for today

Friday, 13 February 2015

09:00 - 17:30 **Friday 13 February: Trigger Processors**

Location: 40-S2-D01 - Salle Dirac

09:00 **NSW Trigger Processor Overview** *30'*

overview of NSW trigger system; interface to sector logic incl. data format, replication; compatibility with phase 2; Latency; project organization incl. schedule and responsibilities

Speaker: Joao Barreiro Guimaraes Da Costa (Harvard University (US))

10:00 **sTGC Interface and Trigger Algorithm** *20'*

incl. performance and testing

Speaker: Julia Narevicius (Weizmann Institute of Science (IL))

Material: **Slides**

Specifications, firmware, testing and performance

10:45 **Coffee** *15'*

11:00 **MicroMegas Interface and Trigger Algorithms** *20'*

including performance and testing

Speaker: David Lopez Mateos (Harvard University (US))

Material: **Slides**

11:40 **Lunch** *1h0'*

12:40 **Ancillary Functions** *20'*

Speaker: Lorne Levinson (Weizmann Institute of Science (IL))

Current Hardware Options

13:20 **Hardware Platforms: LAr/Stony Brook Option** *20'*

Speaker: John David Hobbs (State University of New York (US))

Material: **Slides**

13:55 **Hardware Platform: SRS/Bucharest Option** *20'*

Speaker: Sorin Martoiu (IFIN-HH Bucharest (RO))

14:30 **Hardware Selection Criteria** *20'*

Speaker: Joao Barreiro Guimaraes Da Costa (Harvard University (US))

15:15 **Reviewers' Closed session** *1h0'*

Documentation

- **Documentation:**
  - Main Trigger Processor Document:
    - https://edms.cern.ch/document/1470527/1
  - Hardware Platform Documents:
    - SRS Option: https://edms.cern.ch/document/1476256/1
    - LAr Option: https://edms.cern.ch/document/1476255/1
- **Other relevant documents from the review:**
  - https://edms.cern.ch/nav/P:ATLAS:V0/P:1546242771:V0

TP Review Outline

1 Introduction — This talk
- 1.1 Overview of the NSW trigger
- 1.2 System granularity and terminology
- 1.3 Requirements and Limitations

2 Trigger Processor Specifications
- 2.1 Trigger Processor Latency — This talk
- 2.2 Interface to Micromegas — David
  - 2.2.1 ART Data Protocol
  - 2.2.2 Decoding ART Data
- 2.3 Interface to sTGC — Julia
- 2.4 Interface to Sector Logic — This talk
  - 2.4.1 NSW Trigger Data Format
  - 2.4.2 Combination of sTGC and MM trigger data
  - 2.4.3 Matching to Sector Logic Boards
- 2.5 Ancillary Functions — Lorne

3 Trigger Algorithms and Performance
- 3.1 Micromegas Trigger Algorithm — David
  - 3.1.1 MM Fitter Algorithm
    - 3.1.1.1 Description
    - 3.1.1.2 Implementation
    - 3.1.1.3 Misalignment Configurations and Corrections
    - 3.1.1.4 Performance
    - 3.1.1.5 Summary
  - 3.1.2 MM Look-Up-Table Algorithm
    - 3.1.2.1 Principle of the algorithm
    - 3.1.2.2 Algorithm Implementation
    - 3.1.2.3 Algorithm Performance
    - 3.1.2.4 Summary
- 3.2 sTGC Trigger Algorithm — Julia
  - 3.2.1 The pre-trigger from the pad towers
  - 3.2.2 Finding track segments and calculating their parameters
  - 3.2.3 Compensating for misalignments

Hardware Platforms: LAr/Stony Brook Option — John Hobbs

Hardware Platforms: SRS/Bucharest Option — Sorin

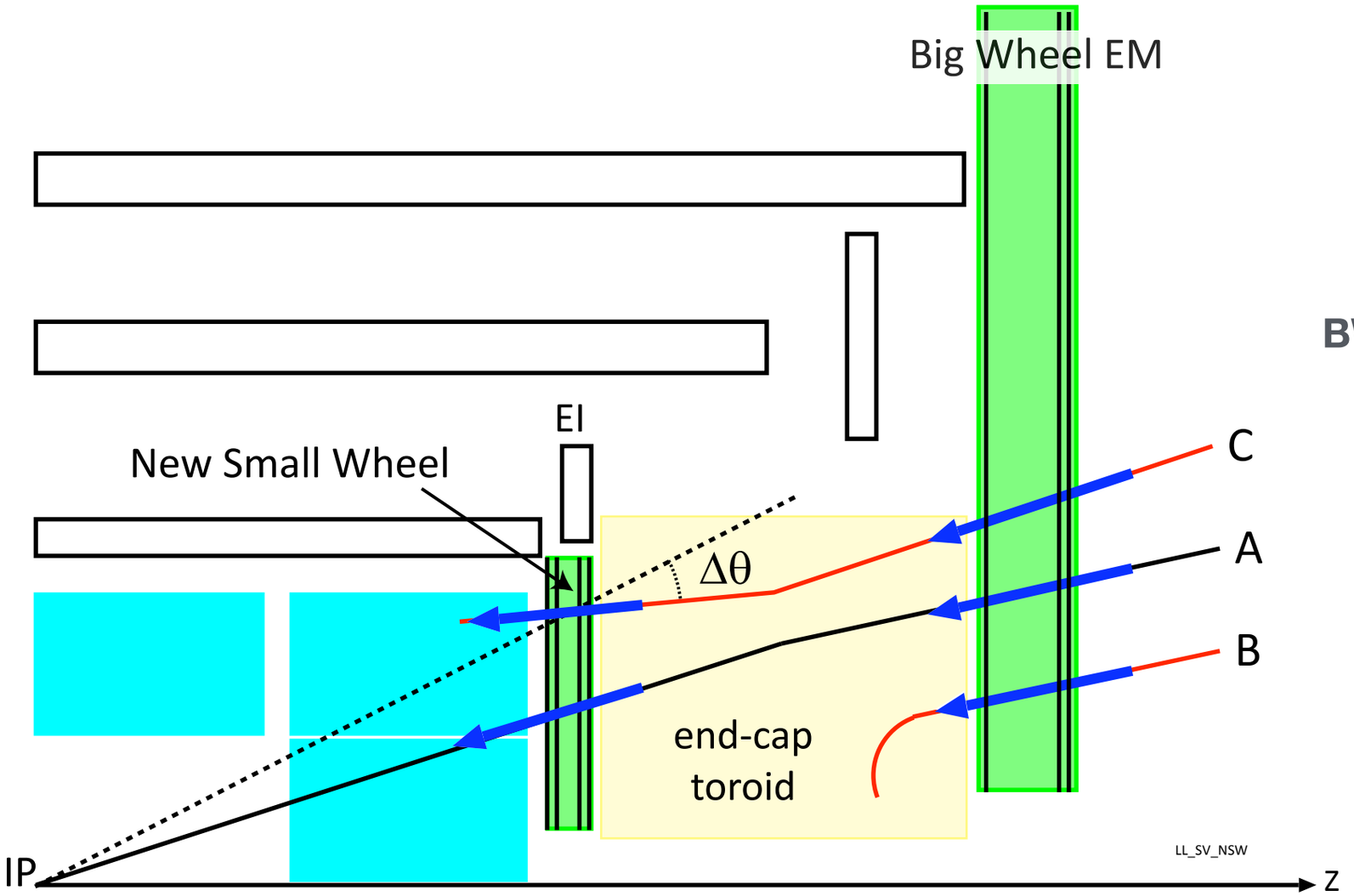
4 Trigger Processor Hardware Platforms — Joao
- 4.1 Specification Comparison
  - 4.1.1 ATCA Standard Interfaces
  - 4.1.2 Optical I/O for Detector Data and Sector Logic
  - 4.1.3 Mezzanine to mezzanine lateral communication
- 4.2 Selection Criteria

5 Testing — This talk / David / Julia
- 5.1 Initial Testing of the MM Implementation
- 5.2 Pattern Generators
  - 5.2.1 The Micromegas ART Pattern Generator
  - 5.2.2 The sTGC Pattern Generator
- 5.3 Cosmic Ray Testing
- 5.4 Vertical Slice and Test Beam

6 Phase-2 Compatibility — This talk

7 Project Organization — This talk
- 7.1 Responsibilities

NSW Trigger Overview



Current trigger:
BW track segments pointing to IP

TRIGGER

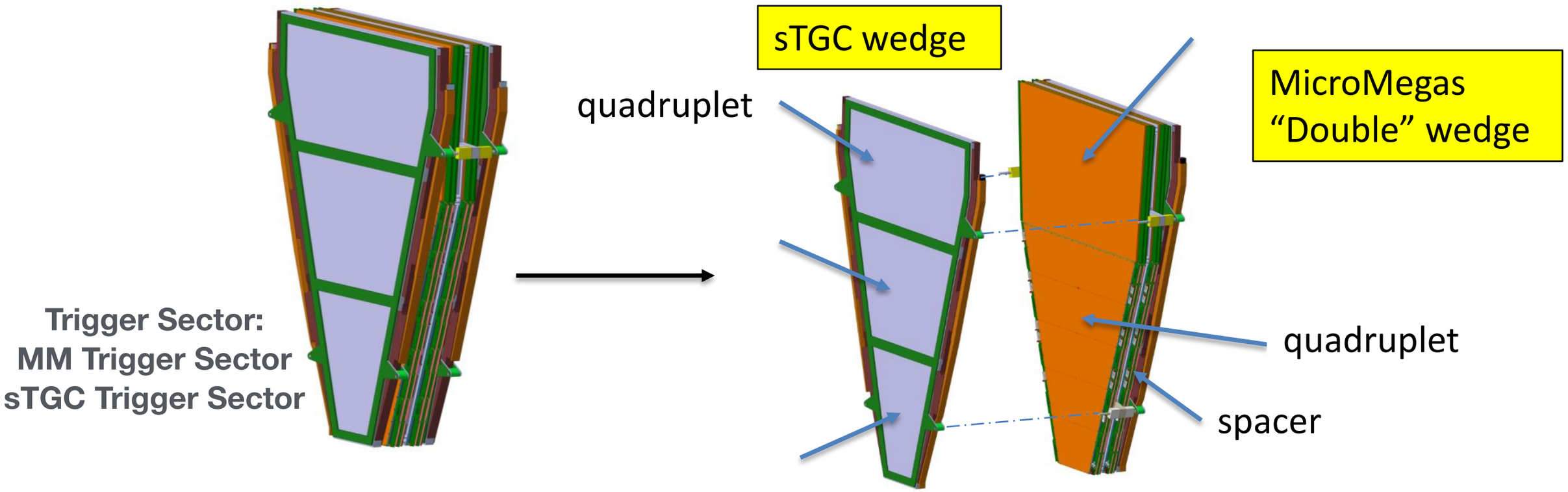
NSW
Micromegas and sTGC
Track segments
1.3 < |η| < 2.7

BW
TGC
Track segments
1.0 < |η| < 2.4

Δθ: Angle relative to 'infinite momentum track' —— resolution goal < 1 mrad

Phase I: Δθ sent to Sector Logic but not used
Phase II: BW trigger segment precision will improve
Use Δθ to cut on bending angle β

Detectors layout and granularity

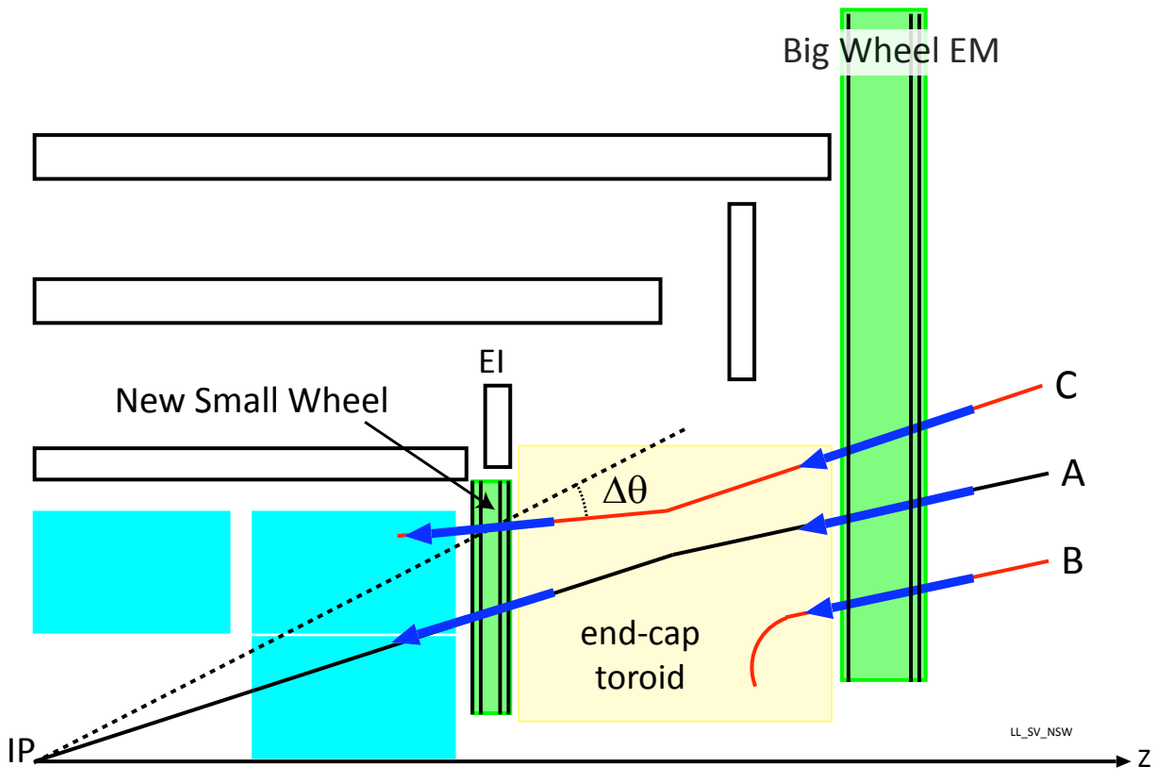


- The NSW has 2 different detector technologies: sTGC and MicroMegas (MM)
- Each NSW sector (16 per wheel/side) consists of 2 sTGC and 2 MicroMegas wedges
- Each MM wedge consists of 2 quadruplets (chambers, modules)
- Each sTGC wedge consists of 3 quadruplets (chambers, modules)
- Each MM/sTGC quadruplet comprises 4 active layers
- Micromegas rely on strips as readout elements, stereo strips for 2nd coordinate
- sTGC rely on strips (precision coord) , pads (pad trigger) and wires (2nd coord) as readout elements

sTGC larger lever arm ==> better Δθ resolution

1 MM Sector ==> 1 MM Trigger Processor (FPGA)
1 sTGC Sector ==> 1 sTGC Trigger Processor (FPGA) } **1/2 Trigger Processor ATCA Board**

Requirements and Limitations



Main requirement:

Δθ: Angle relative to 'infinite momentum track' — — resolution goal < 1 mrad (required for Phase II)

NSW trigger logic to reject track segments with Δθ > 7 - 15 mrad (to be tuned)

Reduces trigger rate to Sector Logic

BW Matching resolution requirement:

ϕ resolution : 20 mrad
η resolution: 0.005

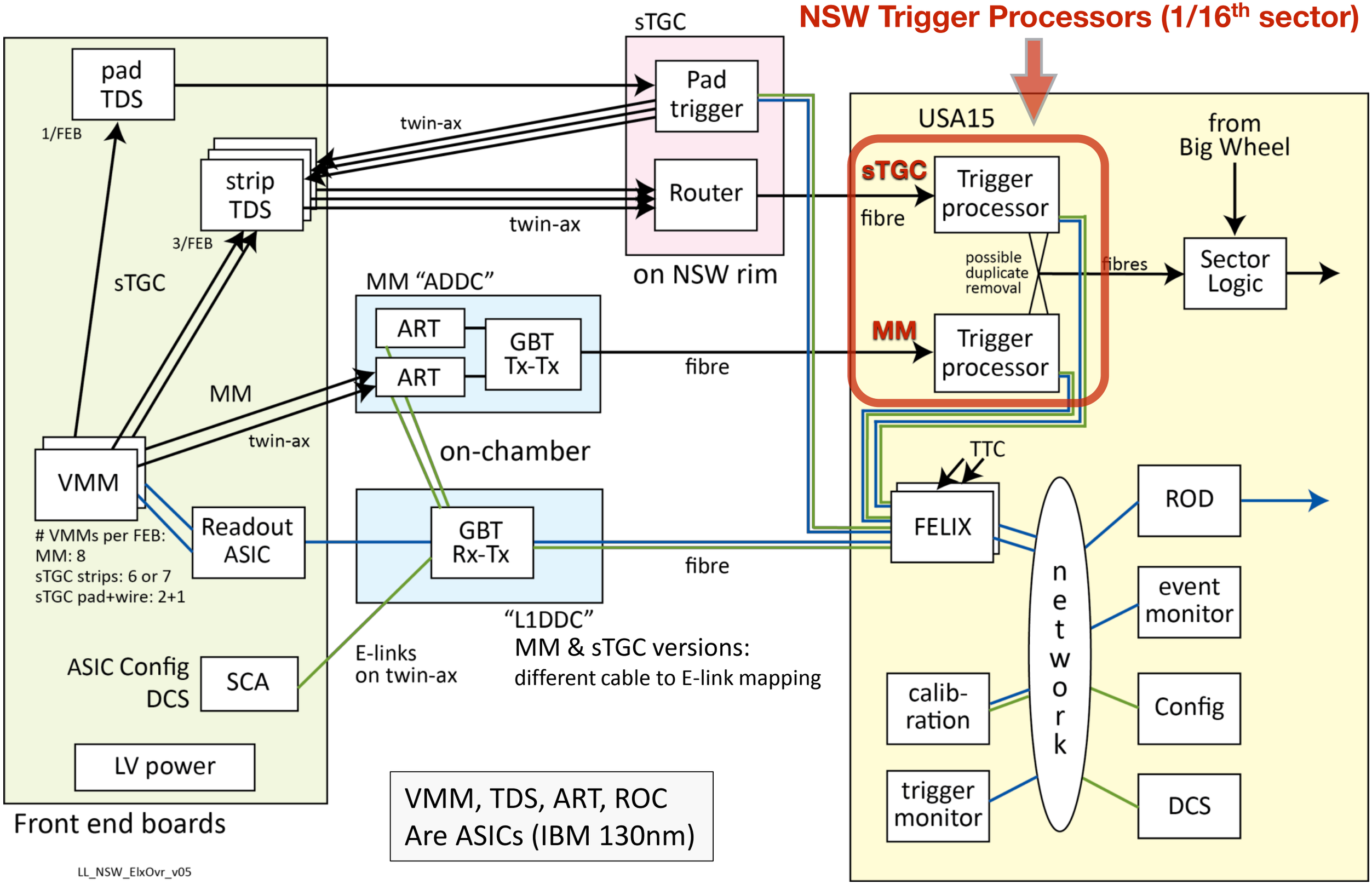
Preliminary ϕ resolution:
MM < 10 mrad
sTGC ~ 20 mrad (from pad size)

The corroboration with the BW trigger is done by projecting the 'infinite momentum track' through the R – ϕ point of the segment in the NSW onto the BW's R – ϕ array of Regions-of-Interest (RoI).

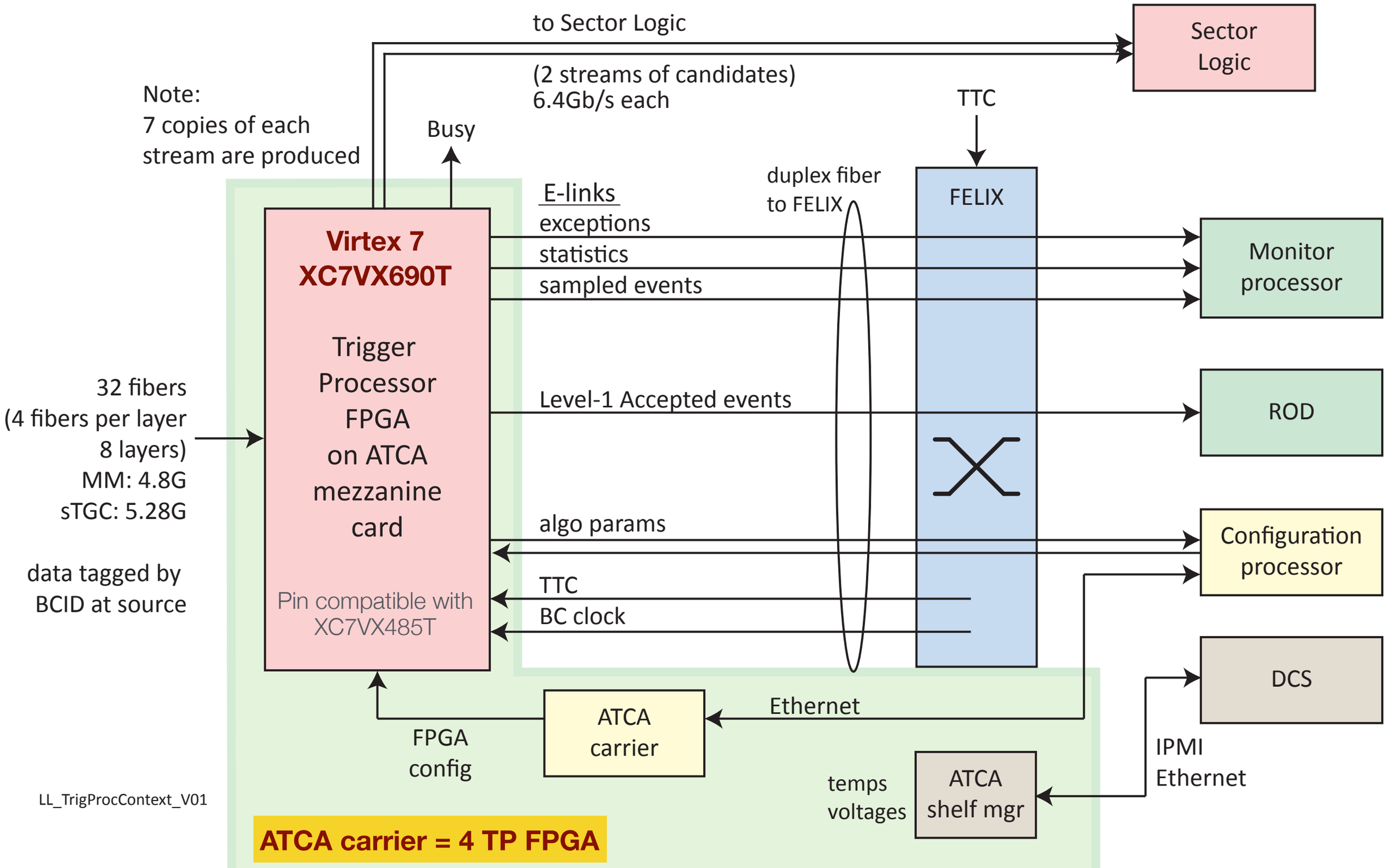
BW RoI: 0.025 x 0.030 in η - ϕ

Lacking complete trigger simulation for MM and sTGC

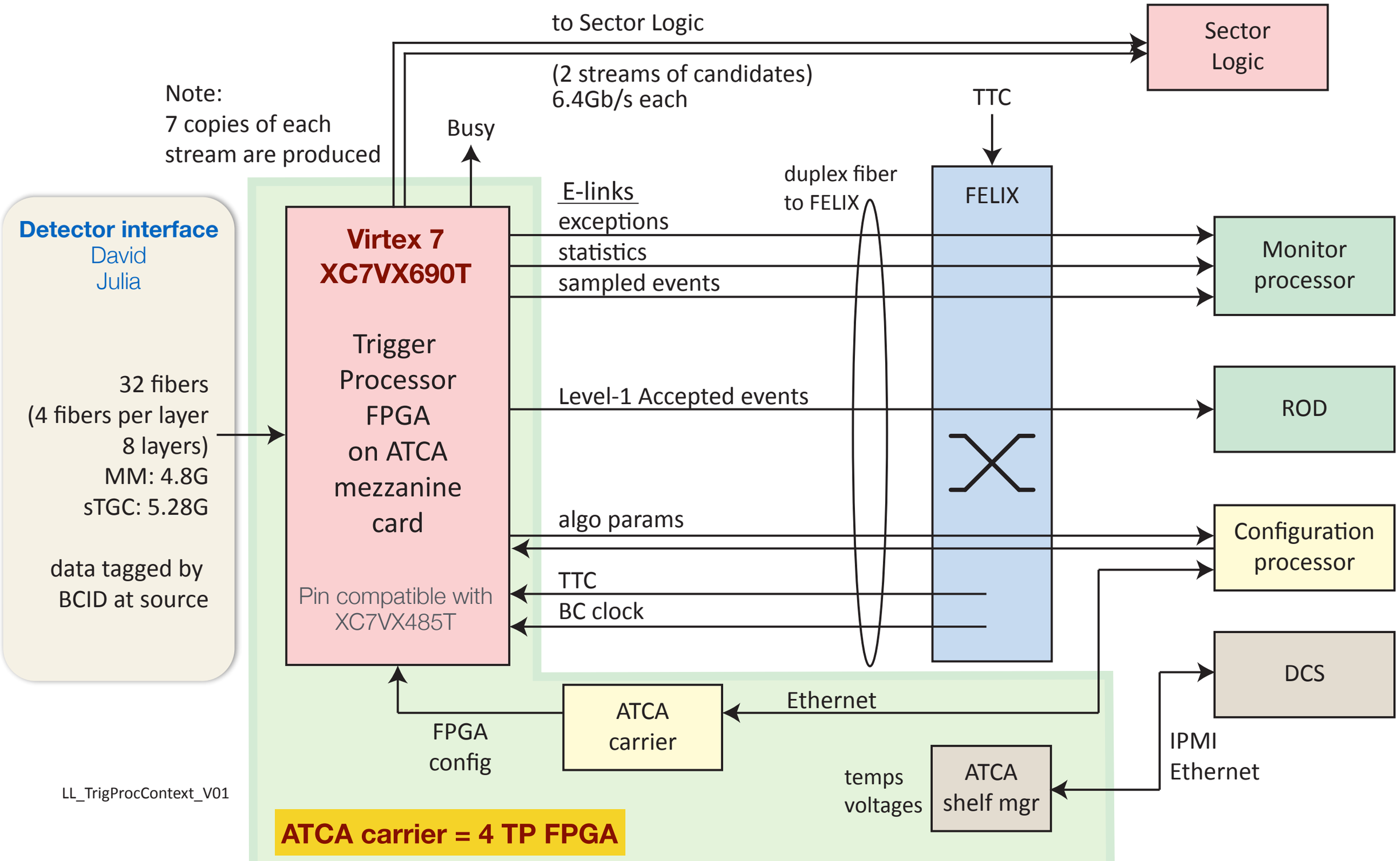
NSW Trigger and DAQ data flow



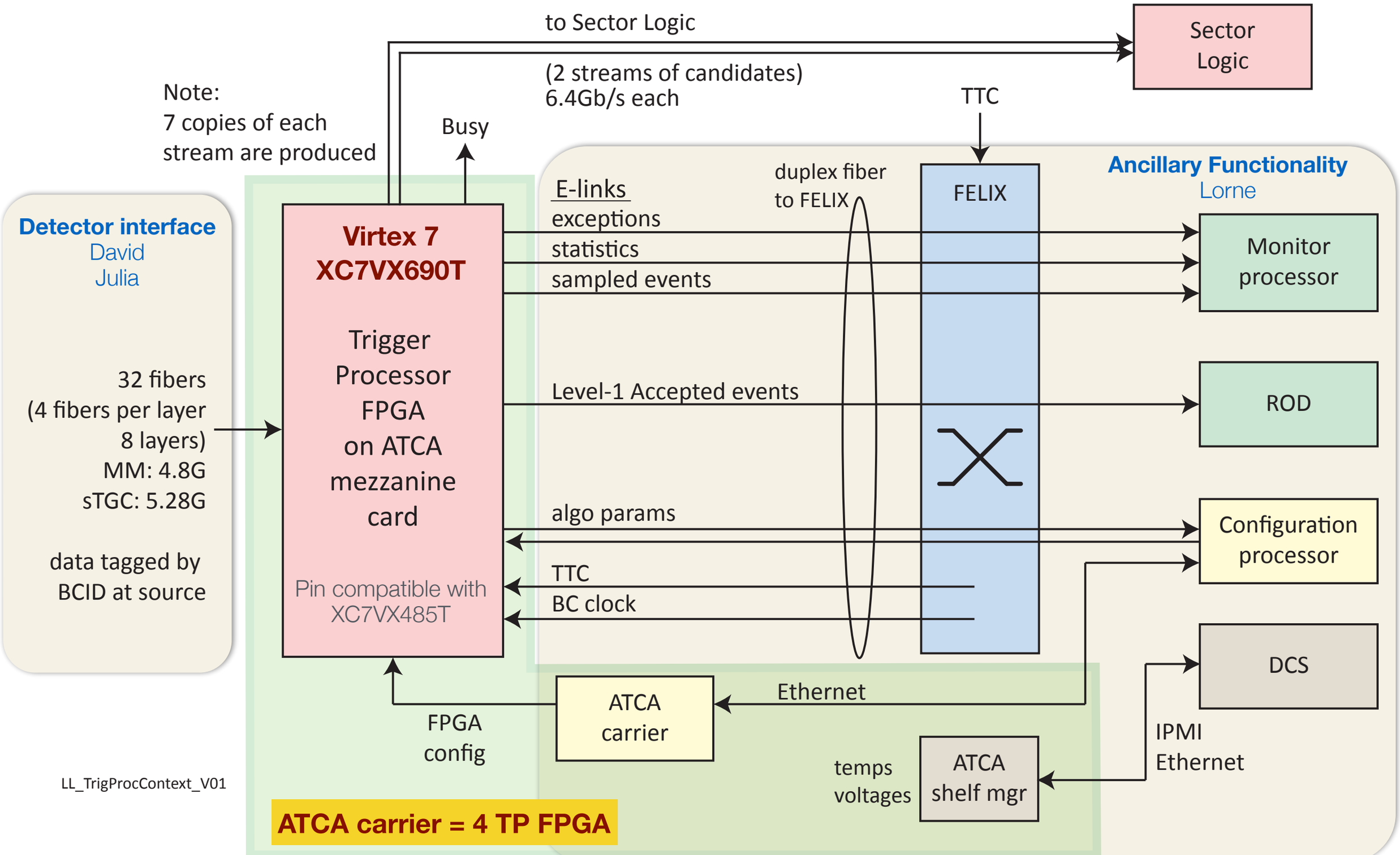
Trigger Processor Specifications



Trigger Processor Specifications



Trigger Processor Specifications



NSW Trigger Data Format

NSW track segment information

Field:	sTGC type	MM type	$\Delta\theta$ (mrad)	ϕ index	R index	spare
Num of bits:	2	2	5	6	8	1

= 24 bits

sTGC/MM Type
No segment: 00
Low quality: 01
Medium quality: 10
High quality: 11

Resolution:

Δθ: 1 mrad/bit)

ϕ index: 10 mrad/bit

R index = η: 0.005/bit

Full scale Δθ: ± 15 mrad

Still to be defined

Granularity to be common between MM and sTGC and small and large sectors

Data Format to Sector Logic

word	byte0	byte1
0	comma	comma
1	segment-1	
2		segment-2
3		
4	segment-3	
5		segment-4
6		
7	SectorID	BCID

4 bits **12 bits**

Idle code for alignment purposes in the 8b/10b encoding

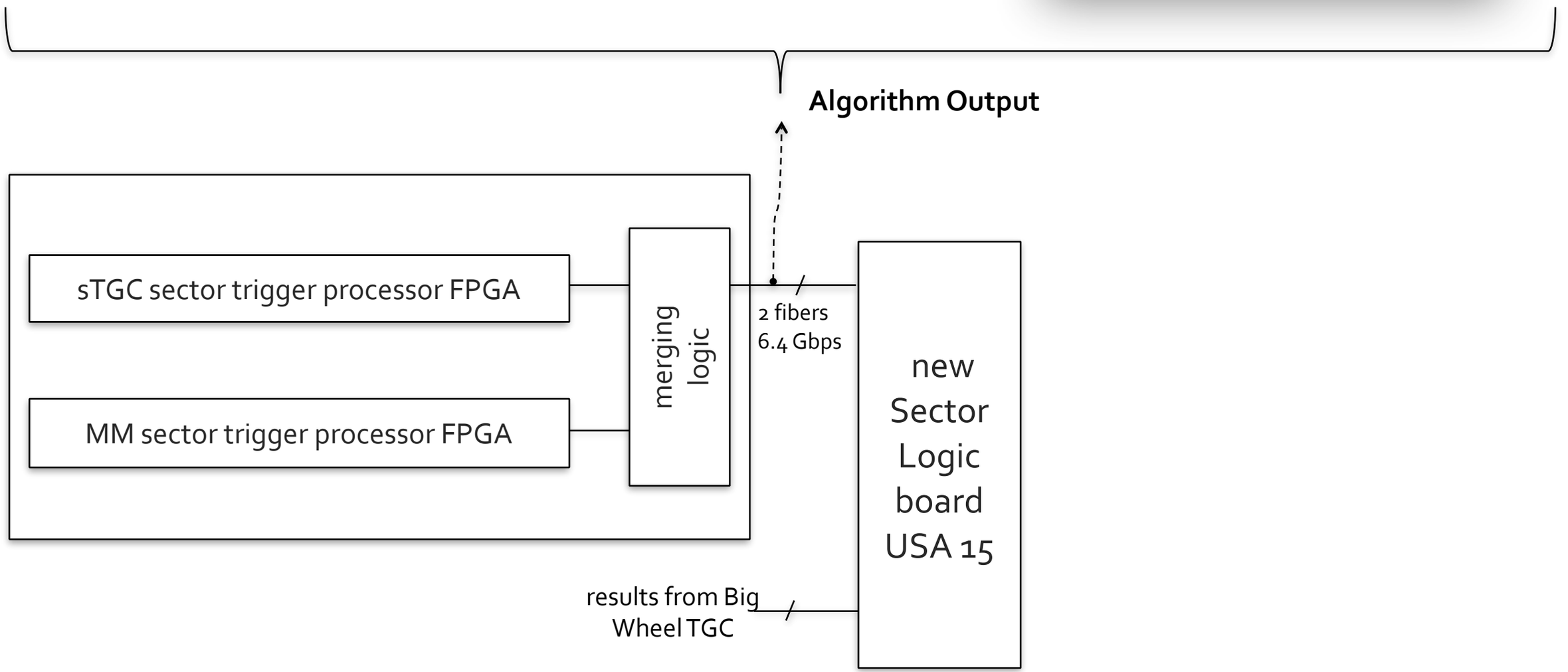
Interface to Sector Logic

Baseline:

- 2 fibers, 4 candidates per fiber (maximum 8 per BC):
  - 6.4 Gb/s, 128 bit, 8b/10b encoded.
  - One 2-byte word is transferred after 8b/10b encoding at 320 MHz

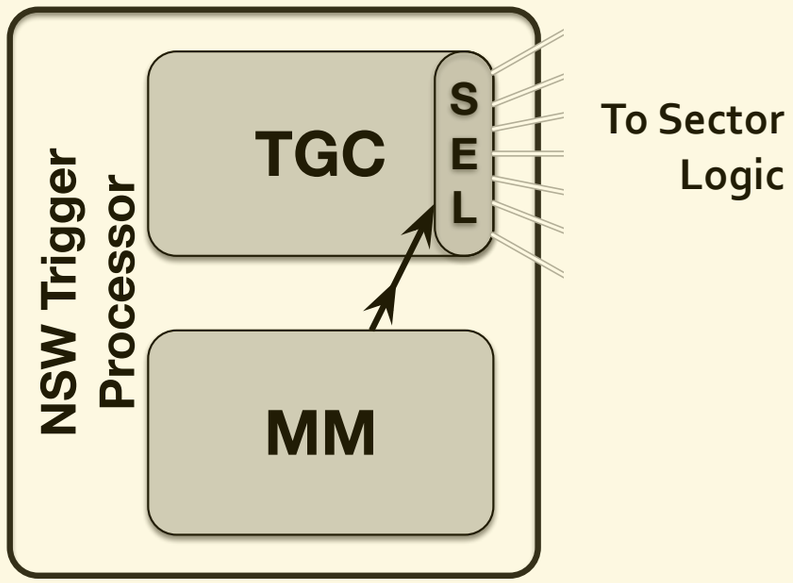
word	byte0	byte1
0	comma	comma
1	segment-1	
2		segment-2
3		
4	segment-3	
5		segment-4
6		
7	SectorID	BCID

X 2



Combination of sTGC and MM Trigger Data

Merging streams in sTGC FPGA



sTGC trigger chain slower by ~130 ns

transfer MM result to sTGC FPGA

Need fast connectivity between FPGAs

SRS hardware option: 64 LVDS high-speed connections
LAr hardware option: 8 LVDS high-speed connections

More on this later

Merging algorithm
expected to take 25-50 ns
(still to be defined)

Will reduce number of candidates to 8
(MM is not limited to 4 candidates)

Possibilities to be studied:

1. **Remove duplicates**: candidates with same R, ϕ and similar $\Delta\theta$ (condition still to be evaluated)
2. **Use quality flag**: probably based on hits on segment

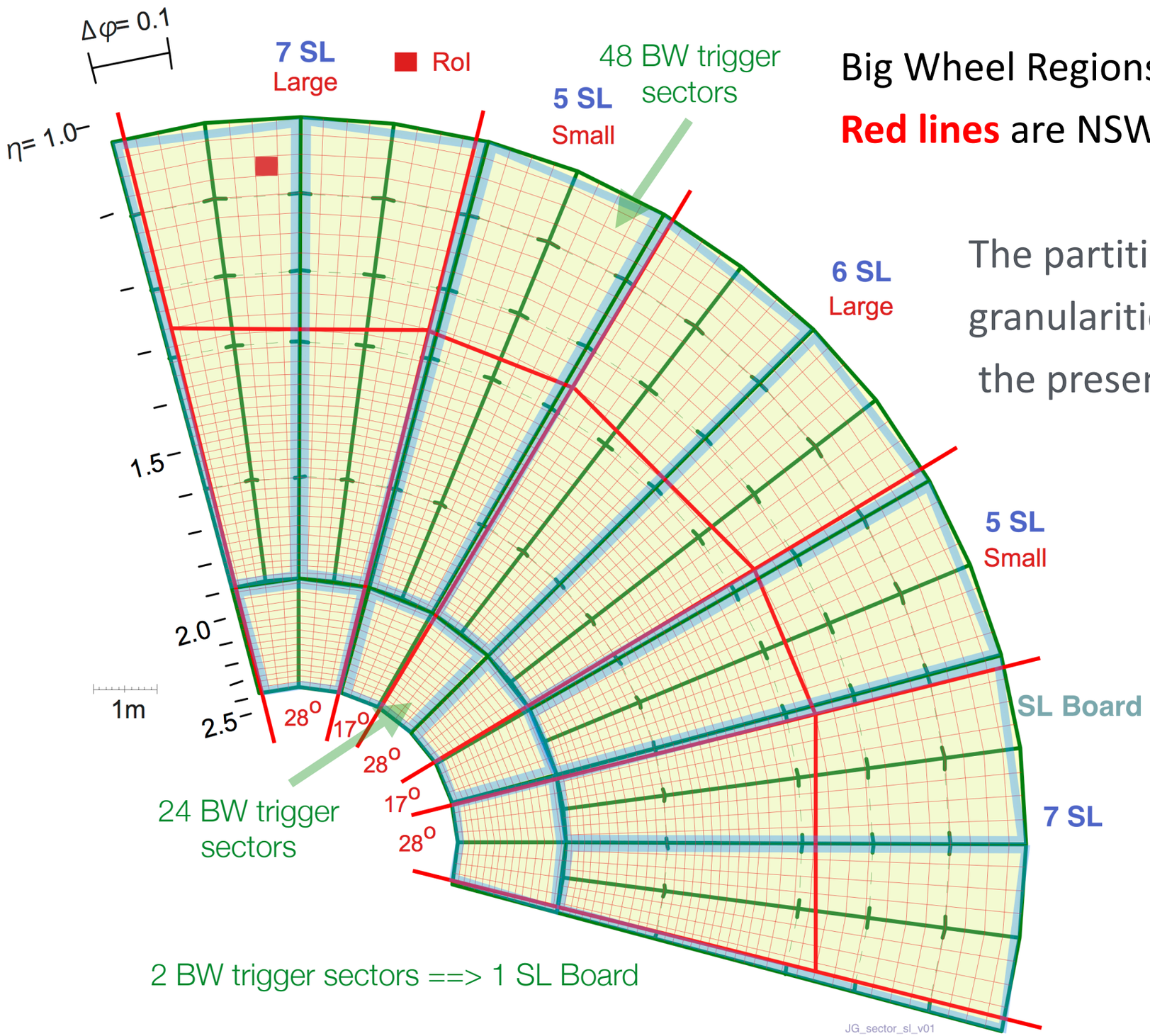
Data overflow

Field:	sTGC type	MM type	$\Delta\theta$ (mrad)	ϕ index	R index	spare
Num of bits:	2	2	5	6	8	1

- Planning to add information about data overflow
  - Set overflow bit if, for a BCID, more than 8 candidates are found
  - Possibility
    - Use reserved bit of the last track candidate word sent to SL
      - No additional bits are required
- If future simulations shows that 8 candidates are insufficient
  - Increase from 2 to 3 fibers to SL (not 100% clear if SL can handle this)
  - Transmission at 8 Gb/s — sufficient to provide 10 candidates
  - Transmission at 9.6 Gb/s — however SL Kintex GTX cannot operate at this rate

Matching to Sector Logic Boards

Track vector information from the NSW is combined with results from the current Level-1 muon trigger system (TGC-BW)

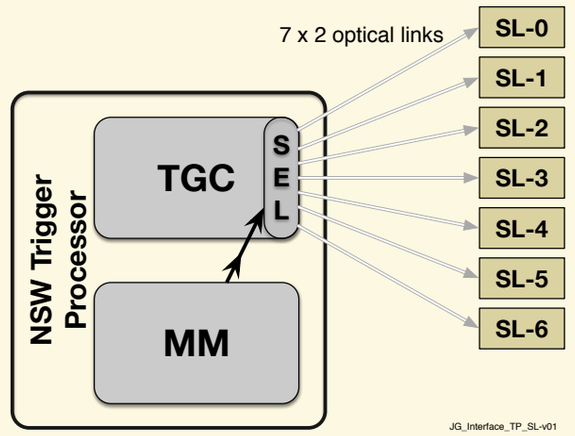


Big Wheel Regions-of-Interest to be confirmed by NSW

Red lines are NSW sector boundaries.

The partitioning of the Trigger Sectors and granularities of the RoI remain the same as in the present scheme

Mismatch of NSW and BW detector boundaries
⇒ fan-out up to **7 SL** boards



Both hardware platforms can provide these much outputs

Other fanout options (now disfavored)

- **These options have been considered until recently but the realization that hardware boards can provide enough output connections, makes the option of sending 7 copies directly to SL the most desirable**

1:7 fan-out with active fan-outs: slightly higher latency due to optical-electrical-optical conversion and additional fiber length

1:7 fan-out with passive optical splitter: rejected since signal loss is too high

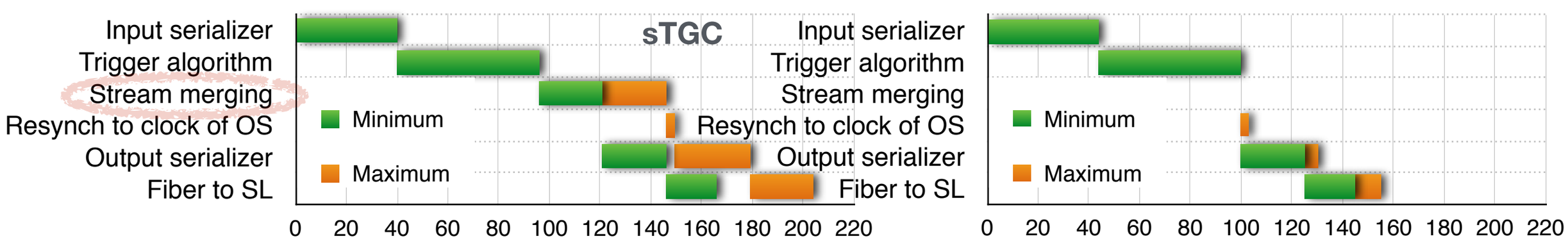
2×(1:4) passive optical splitter: perhaps possible, depending if the transmitter optical power is sufficient. Would need to be checked and/or tested.

4×(1:2) passive optical splitter: OK, but only if the trigger processor has enough outputs. Requires eight output optical links.

Trigger Processor Latency

- Trigger signal delivery to MuCTPI: 57 Bunch Crossings
- New Sector Logic requires: 16 BCs ($5_{serializer}$ + 9processing + 2_{fiber} BCs)
- Full NSW trigger chain: 43 BCs (1075 ns) — including 2 BCs to merge streams

	sTGC		MM		
	min (ns)	max (ns)	min (ns)	max (ns)	Notes
Input deserializer (Rx)	40	40	44	44	
Trigger algorithm	56	56	56	56	320 MHz clock
Stream merging algorithm	25	50	–	–	Assigned to sTGC
Re-synch to 320 MHz clock driving output serializer	0	3.1	0	3.1	45° phase chosen to best match pipeline length
Output to Sector Logic serializer (Tx only)	25	30	25	30	Deserializer on Sector Logic **MM** latency budget
Fiber to Sector Logic	20	25	20	25	4-5 m fiber @ 5 ns/m
Total	166	204.1	145	158.1	

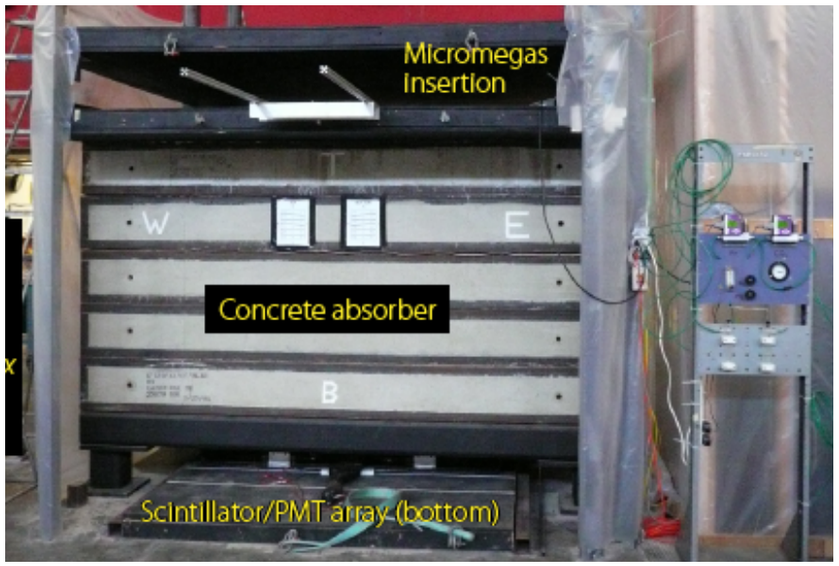


Trigger Processor Testing Plans

- **Testing with Pattern Generators**
  - Both MM and sTGC has followed this path as the main testing tool (details in the talks to follow)
- **Cosmic ray tests**
  - Advantage: Real Front-end electronics

sTGC: Weizmann

MM: Harvard



- **Vertical slice at CERN (Meyrin site)**
  - Integrate the various components of the NSW electronics
    - VMM —> Trigger Processor. Use evaluation board to capture SL input
  - Playback captured and simulated data (can test TP at 40 MHz)

Manpower

NSW Trigger Processor

Joao Guimaraes (Coordinator)

Hardware

Hardware Platform

Option A: LAr ATCA/AMC

Stony Brook
Chuck Pancake (E, 35%)
Eugene Shafto (E, 10%)
John Hobbs (P, 5%)
Dean Schamberger (P, 5%)
Boline (P, 10%)

Arizona
Kenneth Johns (P, 5%)

Option B: SRS ATCA/AMC

Bucharest
Sorin Martoiu (E, 20%)
Gabriel Stoicea (P, 10%)
Michele Renda (S, 10%)

Eicsys Gmbh, Germany
Samway Electronics, Bucharest

Fiber Plant

Weizmann
Lorne Levinson (P, 5%)

Firmware

MM Trigger Algorithm

Harvard
Nathan Felt (E, 50%)
Tomo Lazovich (S, 20%)
John Huth (P, 5%)
Joao Guimaraes (P, 5%)

Saclay
Samira Hassani (P, 5%)

sTGC Trigger Algorithm

Weizmann
Lorne Levinson (P, 5%)
Julia Narevicius (E, 10%)
Alex Roich (E, 10%)

Ancillary Functionality

Illinois
Todd Moore (E, 30%)
Verena M. Outschoorn (P, 5%)
Wooyoung Moon (S, 20%)

Weizmann
Julia Narevicius (E, 10%)
Alex Roich (E, 10%)
Lorne Levinson (P, 5%)

BNL
George Iakovidis (E, 25%)

Studies and Testing

MM Trigger

Harvard
Nathan Felt (E, 50%)
John Oliver (E, 15%)
John Huth (P, 5%)
Joao Guimaraes (P, 5%)
David Lopez Mateos (P, 10%)
Hugh Skottowe (P, 10%)
Tomo Lazovich (S, 40%)
Stephen Chan (S, 40%)
New student (S, 40%)
Brian Clark (S, 10%)

Saclay
Samira Hassani (P, 5%)

BNL
George Iakovidis (E, 50%)

Illinois
Todd Moore (E, 20%)
Verena M. Outschoorn (P, 5%)
Wooyoung Moon (S, 20%)

sTGC Trigger

Weizmann
Lorne Levinson (P, 5%)

JG_Organigram_TP-v1

Schedule

Title	Effort	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
1) Hardware Platform	97w 4d	Hardware Platform									11/2/15, 5:00 PM	
1.1) Option A: SRS	38w	Option A: SRS							8/26/15, 5:00 PM			
1.1.1) Mezzanine card	10w	Mezzanine card		4/22/15, 5:00 PM								
1.1.1.1) V1: Prototype	6w	V1: Prototype	3/25/15, 5:00 PM									
1.1.1.2) V2: Final	4w		V2: Final	4/22/15, 5:00 PM								
1.1.2) ATCA carrier board	28w	ATCA carrier board							8/26/15, 5:00 PM			
1.1.2.1) V1: Virtex 6		2/12/15, 8:00 AM										
1.1.2.2) V2: Kintex 7	28w	V2: Kintex 7							8/26/15, 5:00 PM			
1.2) Option B: LAr	59w 4d	Option B: LAr									11/2/15, 5:00 PM	
1.2.1) Mezzanine Card	22w 1d	Mezzanine Card									11/2/15, 5:00 PM	
1.2.1.1) V2: LAr OTC		2/12/15, 8:00 AM										
1.2.1.2) V3: Muon AMC	22w 1d					V3: Muon AMC					11/2/15, 5:00 PM	
1.2.1.2.1) Design	13w 4d								9/3/15, 5:00 PM			
1.2.1.2.2) Fabrication	4w									10/1/15, 5:00 PM		
1.2.1.2.3) Board Testing	4w 2d										11/2/15, 5:00 PM	
1.2.2) ATCA carrier Board	37w 3d	ATCA carrier Board									11/2/15, 5:00 PM	
1.2.2.1) V1: LAr ATCA	16w 3d	V1: LAr ATCA				6/8/15, 5:00 PM						
1.2.2.1.1) Design	2w 3d		3/2/15, 5:00 PM									
1.2.2.1.2) Fabrication	6w			4/13/15, 5:00 PM								
1.2.2.1.3) Board Testing	8w				6/8/15, 5:00 PM							
1.2.2.2) V2: Muon+LAr board	21w					V2: Muon+LAr board					11/2/15, 5:00 PM	
1.2.2.2.1) Design	10w							8/17/15, 5:00 PM				
1.2.2.2.2) Fabrication	6w								9/28/15, 5:00 PM			
1.2.2.2.3) Board Testing	5w									11/2/15, 5:00 PM		
2) Firmware	190w											
2.1) Ancillary Functions	128w 2d											
2.1.1) Basic	16w					6/3/15, 5:00 PM						
2.1.2) Enhanced	112w 2d											
2.2) sTGC Trigger Algorithm	28w	sTGC Trigger Algorithm						7/29/15, 5:00 PM				
2.3) MM Trigger Algorithm	21w 3d	MM Trigger Algorithm				6/3/15, 5:00 PM						
2.4) sTGC+MM Merging	12w				5/6/15, 5:00 PM							
3) Testing	0h				Testing						12/1/15, 8:00 AM	
3.1) Vertical Slice Start											12/1/15, 8:00 AM	
3.2) Cosmic Ray Tests Start									9/1/15, 8:00 AM			
3.3) MSW Start					5/1/15, 8:00 AM							
4) External factors	1d							External factors	9/1/15, 8:00 AM			
4.1) VMM2 Chip Ready	1d	2/12/15, 5:00 PM										
4.2) VMM3 Chip Ready									9/1/15, 8:00 AM			

Conclusions

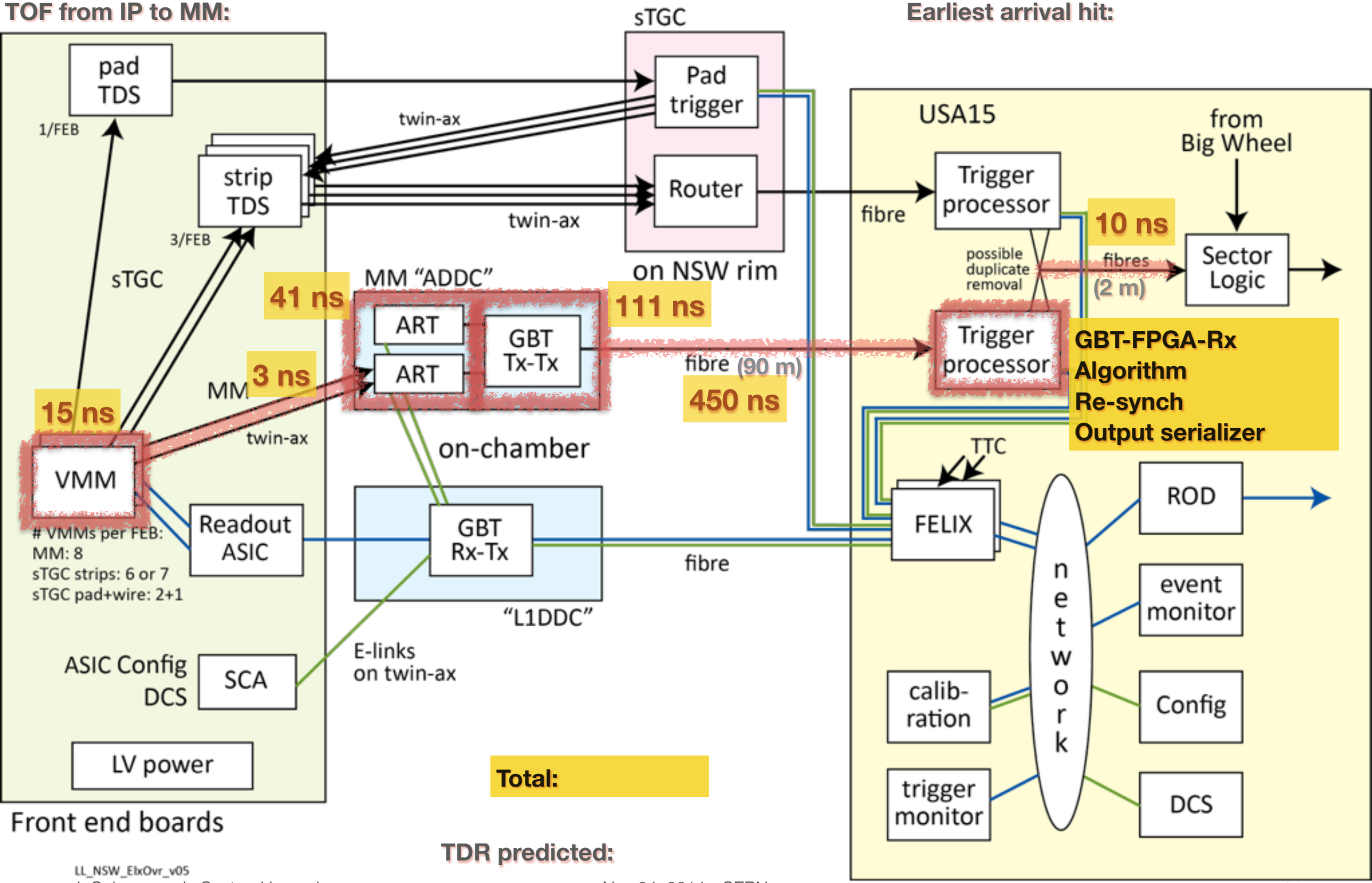
- Work on Trigger Processor is rather advanced already
- Lack of proper simulation is limiting estimations of rates, efficiencies and resolutions
  - More on this later
- Tests on real data (cosmic rays and test beams) limited by availability of FE boards with VMM2
  - Most studies of the trigger algorithms can be made in evaluation boards. No urgent need for ATCA boards to be available.
- Two hardware platforms to choose from
  - Both seem adequate for the job (so, a good problem to have)
  - Will discuss this in the afternoon
- Compatibility with Phase II
  - Trigger hardware and algorithms should be compatible with Phase II requirements
  - However, one should not exclude the possibility of using the larger latency to improve the algorithms (e.g. use information of both MM and sTGC)
    - This would likely require new FPGA's, mezzanine cards and possibly ATCA boards

Backup Slides

MM Latency

TOF from IP to MM:

Earliest arrival hit:



Total:

TDR predicted:

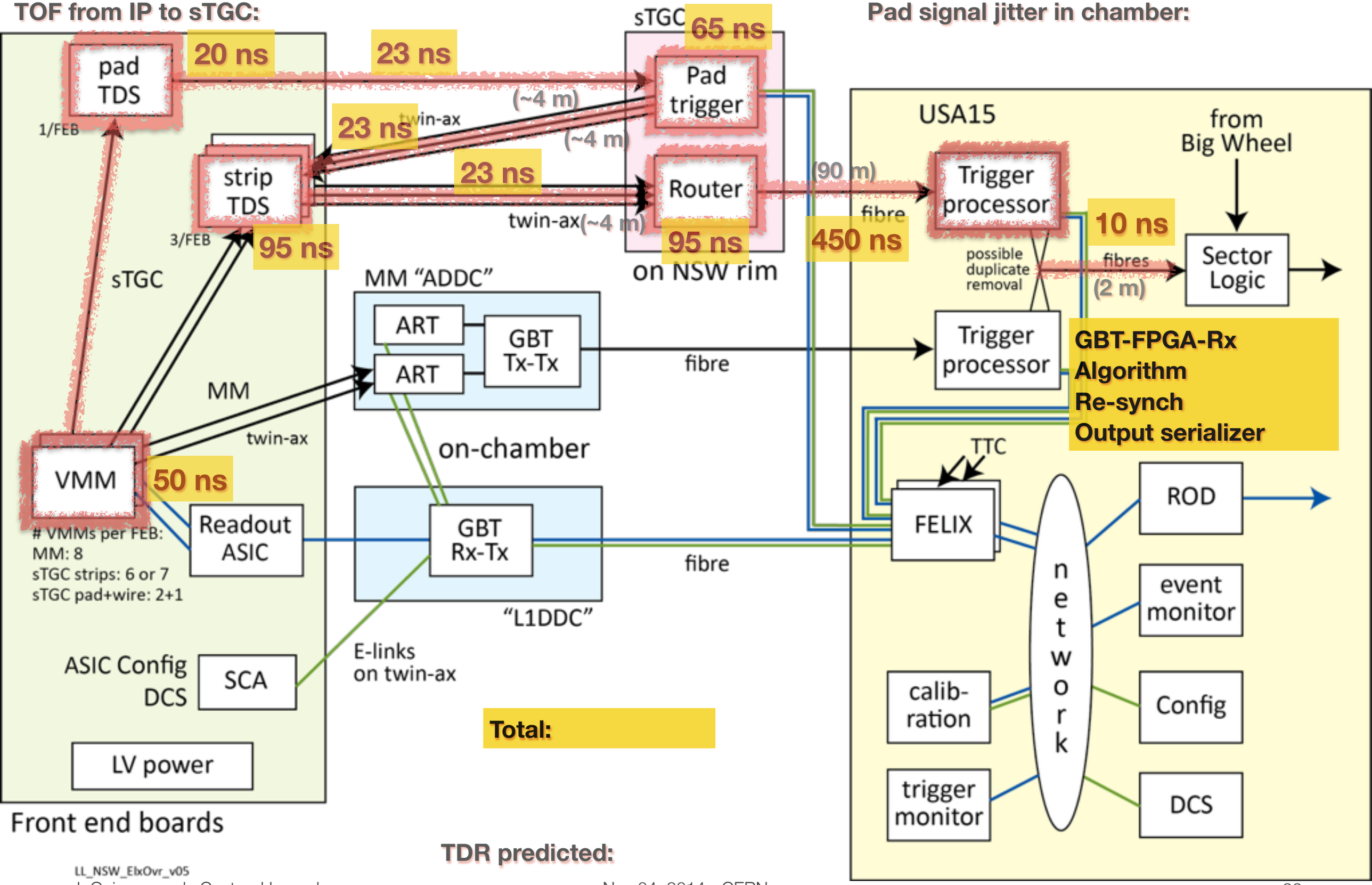
MM Latency

	min (ns)	max (ns)	Notes
TOF from interaction point to MM (z=7.744 m)	30.2	30.2	To periphery of MM @R=4.618m + 5 cm IP
Earliest arrival hit	50	75	Depends onsite of rolling window (2 or 3 BC)
VMM2 chip latency	10	15	ART at threshold crossing instead of peak
FEB to Trigger Driver cable	3	3	Twin-ax cable 0.5 m @ 5 ns/m
Trigger driver latency	41	41	ART encoding (companion chip): from VMM to until first data bunch is output to GBT
Uplink GBT latency (Tx)	99	111	GBTx measured Mar 2014
Fiber to Trigger Processor card in USA15 (80-90 m)	400	**450**	5 ns/m (fiber length might be reduceable)
Uplink GBT latency (Rx)	44	44	GBT-FPGA (optimized) - includes GTX-TX (Kai Chen)
Trigger Algorithm	56.25	56.25	320 MHz clock
Re-synch to 320 MHz clock driving output serializer	0	3.1	45° phase chosen to best match pipeline length
Output to Sector Logic serializer (Tx only)	25	30	Deserializer on Sector Logic latency budget
Fiber to Sector Logic	5	10	1-2 m fiber @ 5ns/m
Total	**763**	**869**	TDR was 785-920 ns

sTGC Latency

TOF from IP to sTGC:

Pad signal jitter in chamber:



Total:

TDR predicted:

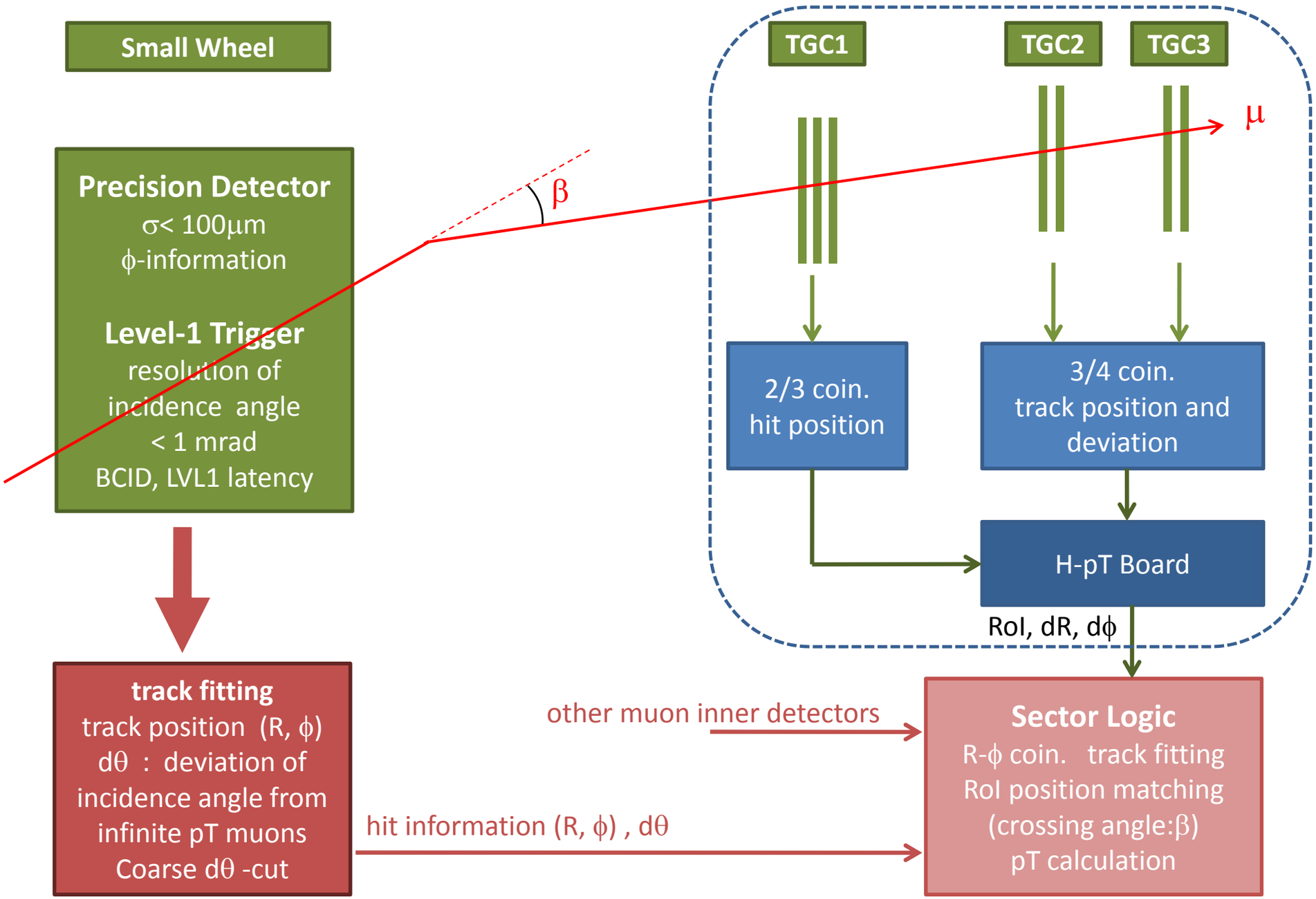
LL_NSW_ElxOvr_v05

sTGC Latency

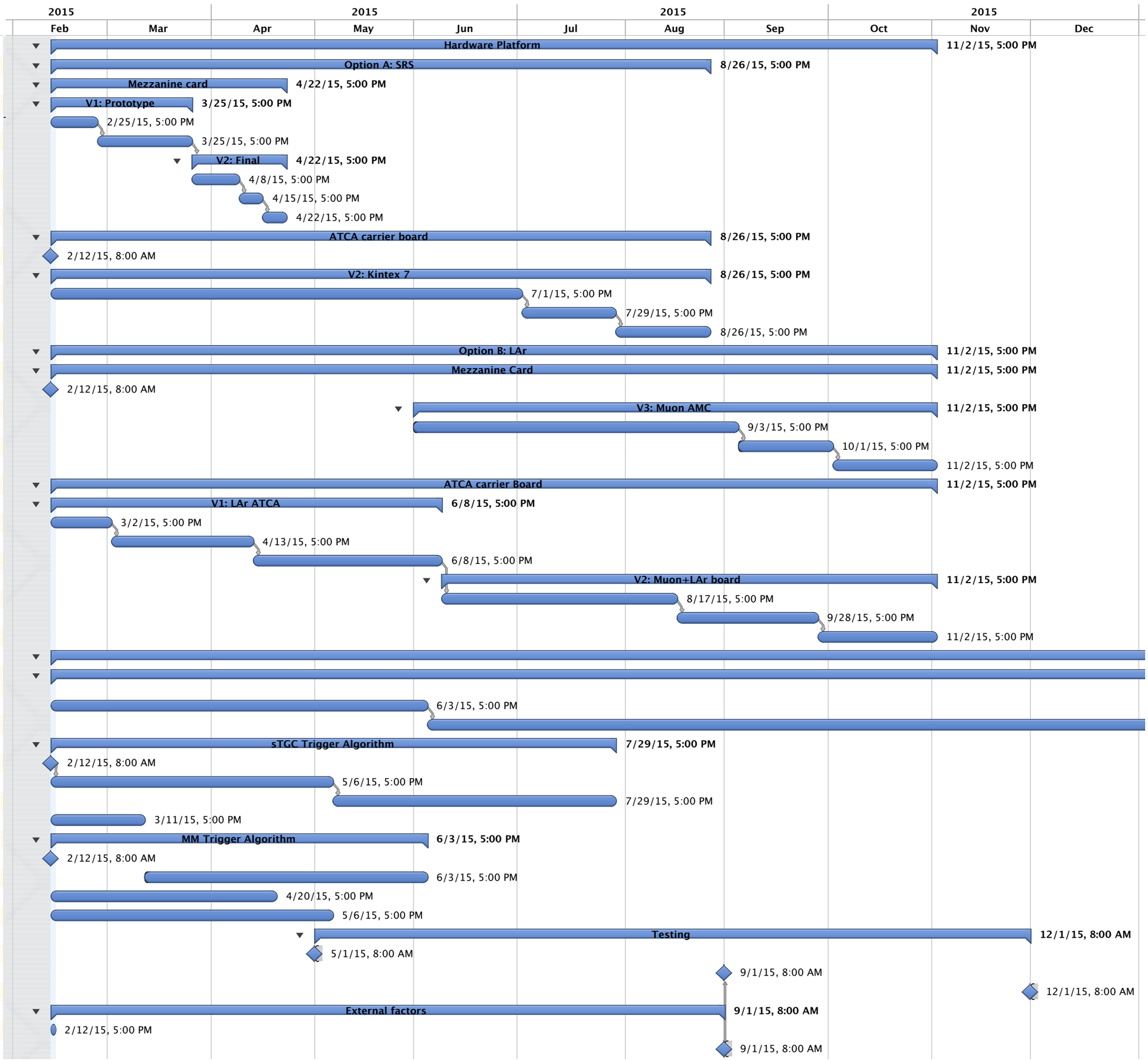
	min (ns)	max (ns)	Notes
TOF from interaction point to NSW (z=7.8 m)	29	31	To periphery of NSW @R=5m
Pad signal jitter in chamber	5	10	Worst case due to tracks midway between wires (late signals due to long drift time)
Pad ASD (VMM)	40	50	ASD latency + time-to-peak
Serialize 32 pads @5 Gbps	16	20	
TDS to pad triger on rim, max 4 m	18	23	Twin-ax cable delta R = 3-4 m + delta Z = 0.5 m @ 5 ns/m
Deserialize 32 pads	30	40	On Pad Trigger
Pad trigger (incl deskew)	15	25	Strips are pipelined until pad trigger arrives
Serializer of Pad Trigger output	0	0	25 ns for 32 bits @ 1.28 Gbits/sec (simultaneous with deserializer)
Pad trigger to on-chamber TDS ASIC	18	23	Twin-ax cable delta R = 3-4 m + delta Z = 0.5 m @ 5 ns/m
TDS: Trigger Data Serializer	**95**	**95**	(Strip data transferred while waiting for pad trigger)
On chamber cabling (up to 3-4m) to Router	18	23	Twin-ax cable delta R = 3-4 m + delta Z = 0.5 m @ 5 ns/m
Router	**85**	**95**	Include deserialization, switch (10 ns), serialization
Fiber to Centroid card in USA15 (80-90m)	400	**450**	5 ns/m (fiber length might be reduceable)
Trigger processor input deserializer	40	40	
sTGC trigger algorithm	56	56	8 layers done in parallel, measured to be 13 clocks + 5 estimated
Re-synch to 320 MHz clock driving output serializer	0	3.1	45° phase chosen to best match pipeline length
Centroid to Sector Logic serializer (Tx only)	25	30	Deserializer on Sector Logic latency budget
Fiber to Sector Logic	5	10	
Total	**890**	**1024**	TDR was 780-896 ns

Sector Logic for the NSW

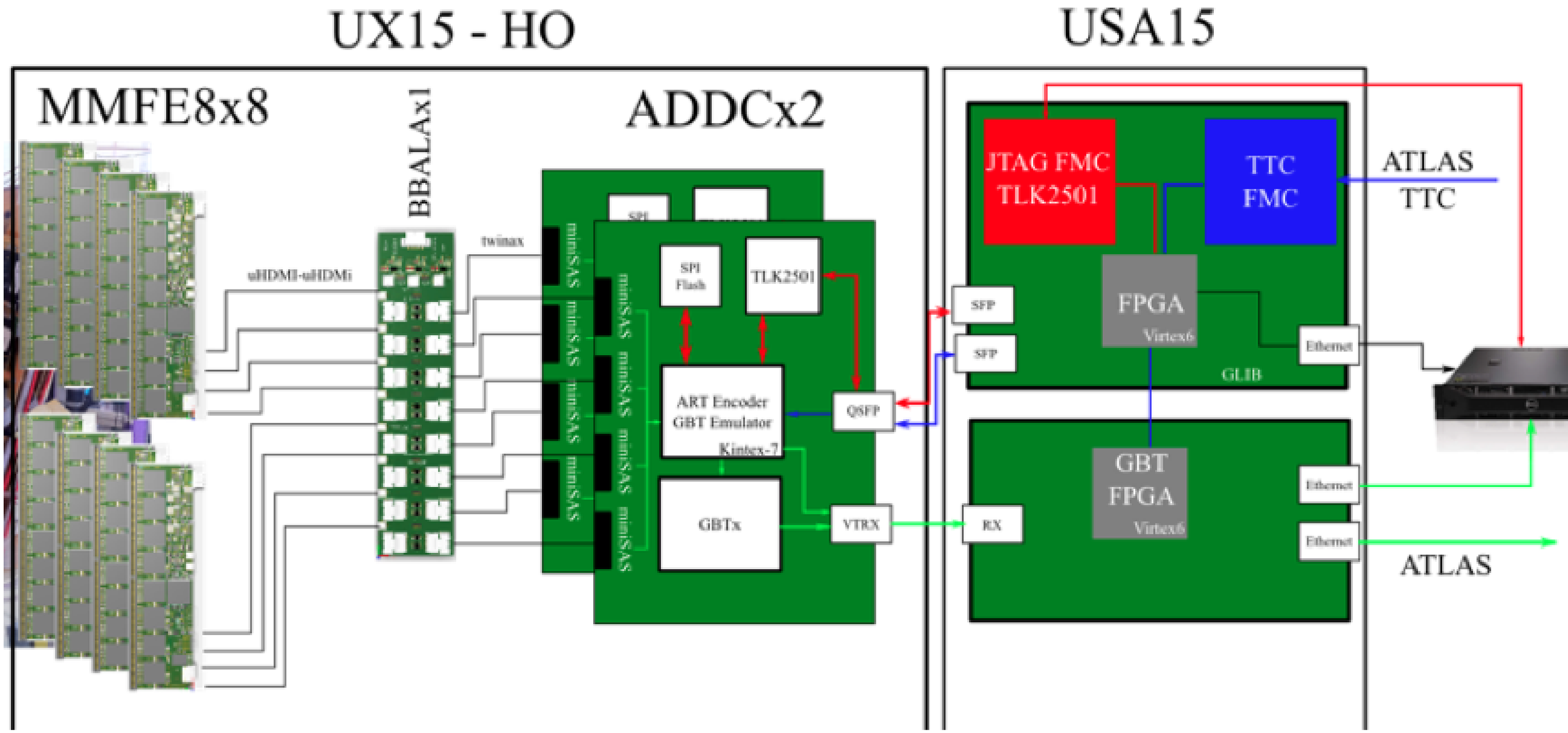
Track vector information from the NSW is combined with results from the current Level-1 muon trigger system (BW-TGC)

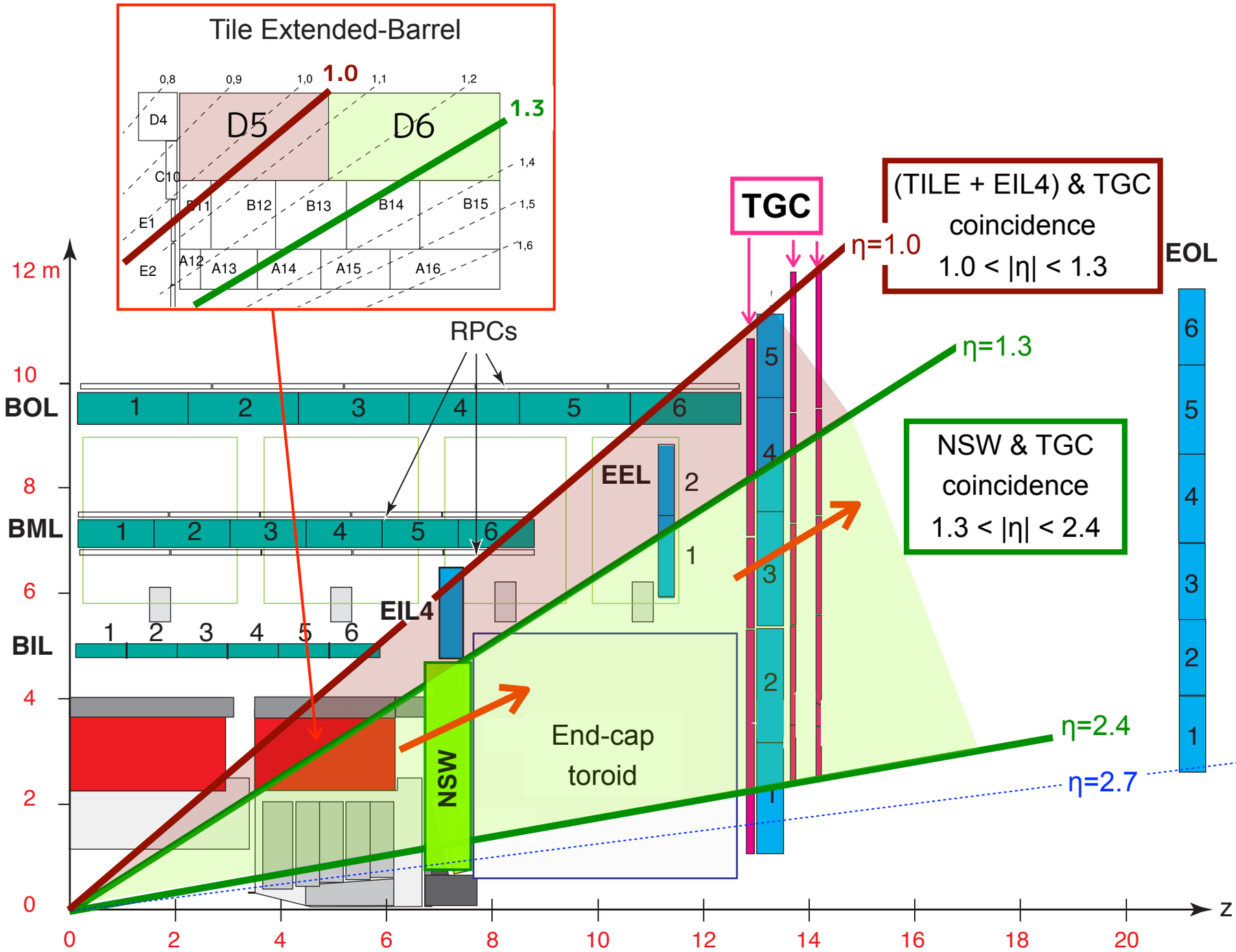


Title	Effort
1) Hardware Platform	97w 4d
1.1) Option A: SRS	38w
1.1.1) Mezzanine card	10w
1.1.1.1) V1: Prototype	6w
1.1.1.1.1) Fabrication	2w
1.1.1.1.2) Board Testing	4w
1.1.1.2) V2: Final	4w
1.1.1.2.1) Design	2w
1.1.1.2.2) Fabrication	1w
1.1.1.2.3) Board Testing	1w
1.1.2) ATCA carrier board	28w
1.1.2.1) V1: Virtex 6	
1.1.2.2) V2: Kintex 7	28w
1.1.2.2.1) Design	20w
1.1.2.2.2) Fabrication	4w
1.1.2.2.3) Board Testing	4w
1.2) Option B: LAr	59w 4d
1.2.1) Mezzanine Card	22w 1d
1.2.1.1) V2: LAr OTC	
1.2.1.2) V3: Muon AMC	22w 1d
1.2.1.2.1) Design	13w 4d
1.2.1.2.2) Fabrication	4w
1.2.1.2.3) Board Testing	4w 2d
1.2.2) ATCA carrier Board	37w 3d
1.2.2.1) V1: LAr ATCA	16w 3d
1.2.2.1.1) Design	2w 3d
1.2.2.1.2) Fabrication	6w
1.2.2.1.3) Board Testing	8w
1.2.2.2) V2: Muon+LAr board	21w
1.2.2.2.1) Design	10w
1.2.2.2.2) Fabrication	6w
1.2.2.2.3) Board Testing	5w
2) Firmware	190w
2.1) Ancillary Functions	128w 2d
2.1.1) Basic	16w
2.1.2) Enhanced	112w 2d
2.2) sTGC Trigger Algorithm	28w
2.2.1) Main algorithm	
2.2.2) Alignment corrections	12w
2.2.3) Single quadruplet algorithm	12w
2.2.4) sTGC Emulator VMM2	4w
2.3) MM Trigger Algorithm	21w 3d
2.3.1) Main algorithm	
2.3.2) Alignment corrections	12w
2.3.3) ART Pattern Generator	9w 3d
2.4) sTGC+MM Merging	12w
3) Testing	0h
3.1) MSW Start	
3.2) Cosmic Ray Tests Start	
3.3) Vertical Slice Start	
4) External factors	1d
4.1) VMM2 Chip Ready	1d
4.2) VMM3 Chip Ready	



MSW in ATLAS Cavern




Tile Extended-Barrel
0,8
0,9
1,0
1,1
1,2
1.0
1.3
D4
D5
D6
C10
E1
E2
B11
B12
B13
B14
B15
A12
A13
A14
A15
A16
1,4
1,5
1,6
12 m
10
8
6
4
2
0
BOL
BML
BIL
1 2 3 4 5 6
RPCs
EEL
EIL4
NSW
End-cap
toroid
TGC
η=1.0
(TILE + EIL4) & TGC
coincidence
1.0 < |η| < 1.3
EOL
η=1.3
NSW & TGC
coincidence
1.3 < |η| < 2.4
η=2.4
η=2.7
z
0
2
4
6
8
10
12
14
16
18
20