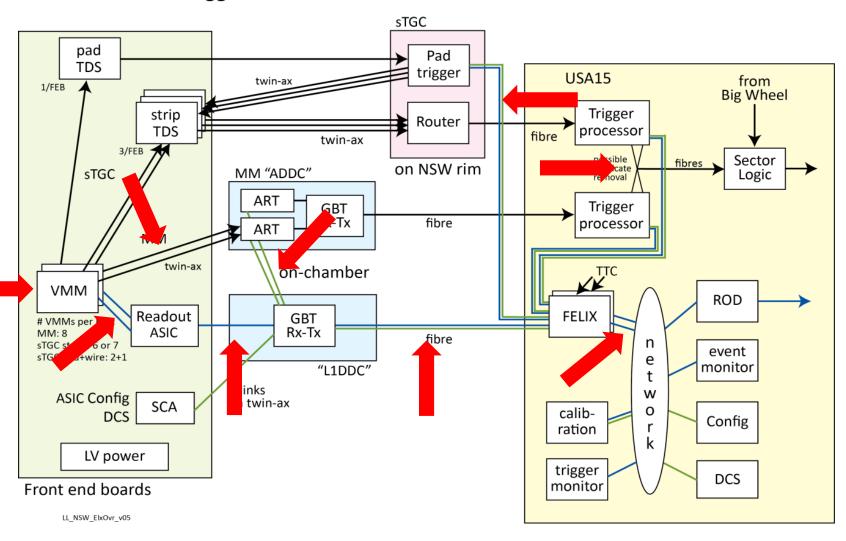
#### **NSW Estimates of Data Rates**

Daniel Lellouch
Weizmann Institute

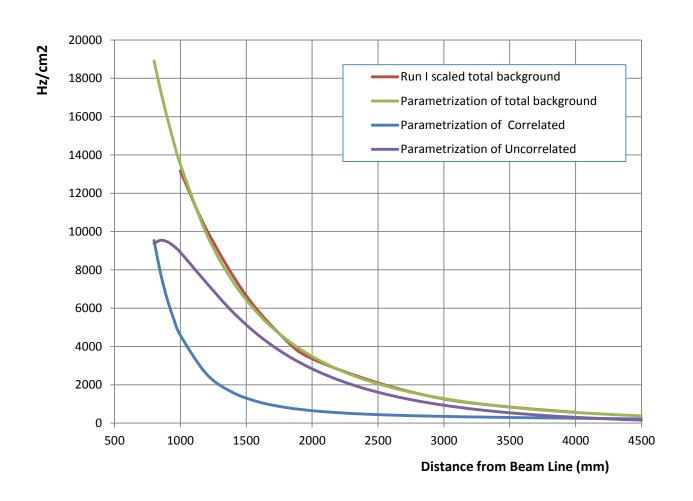
#### NSW Electronics Trigger & DAQ dataflow



## Main Assumptions

- Luminosity:  $7 \times 10^{34}$
- Correlated and uncorrelated backgrounds: scale from RUN-1
  - Increase in energy, new beam pipe & shielding: ~30% reduction
  - Will have a thinner JD → background increase
  - Assume overall compensation of effects
- Strips per μ:
  - sTGC: 4.7 for sTGC
  - MM: 4 to 9 depending on angle and mag field. Take a conservative 10 until detailed Monte Carlo provides a better parametrization.
- Read out 3 BC's for sTGC, 5 for MM

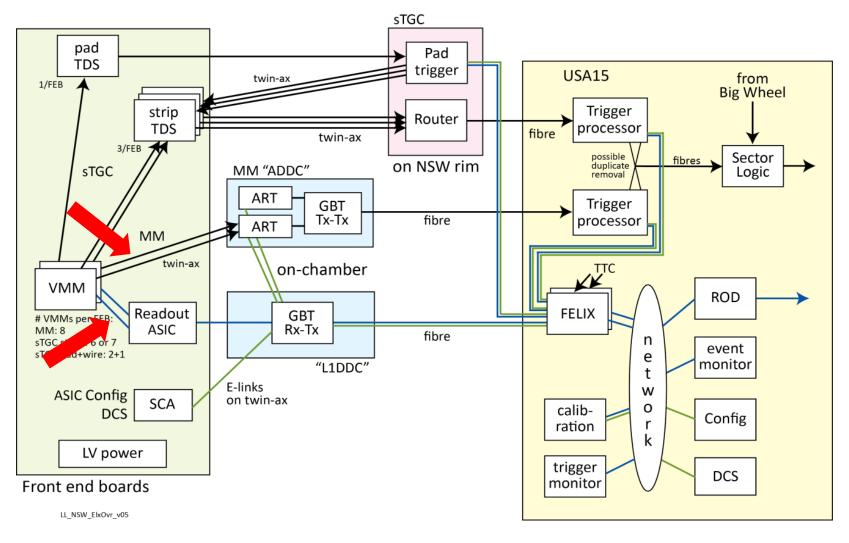
# Background parametrization



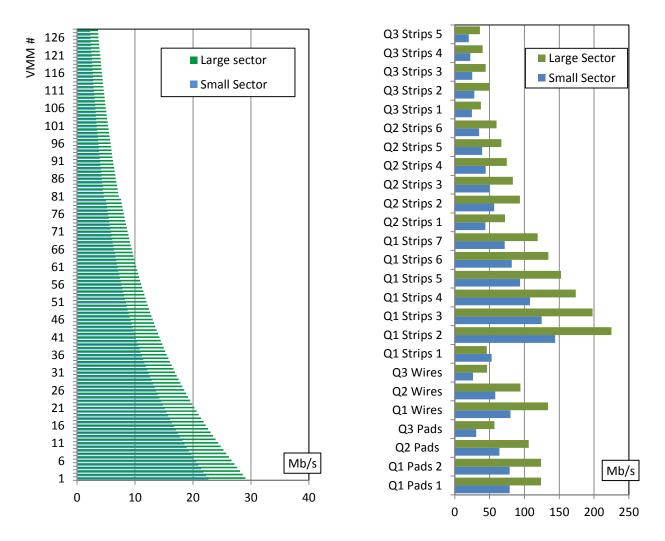
Actual parametrization in  $\Delta \eta \bullet \Delta \varphi$  (matches geometry)

# Data rates from VMM chips

NSW Electronics Trigger & DAQ dataflow



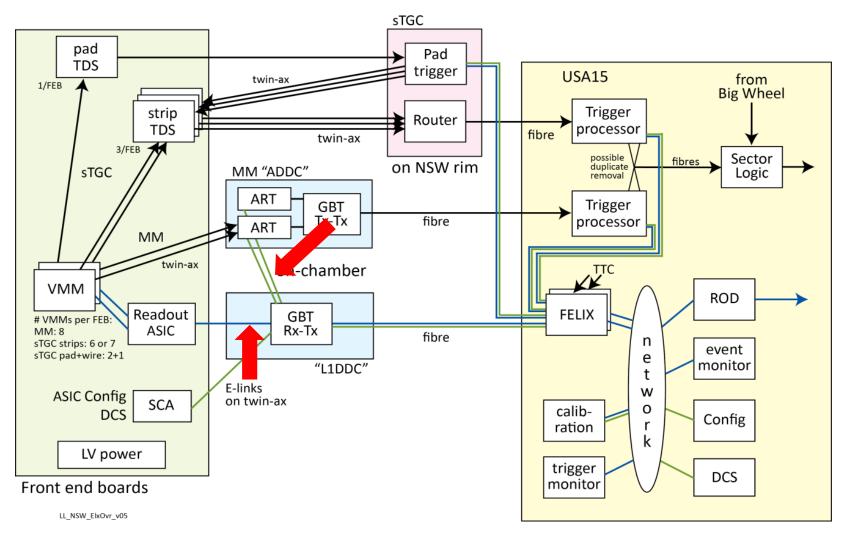
Goal: verify that rates are well below 640 Mb/s



- ~8 times more VMM chips for MM (left) than sTGC (right) since strip widths are ~.4 resp 3.2 mm
- Rates scale accordingly
- Well in busyness

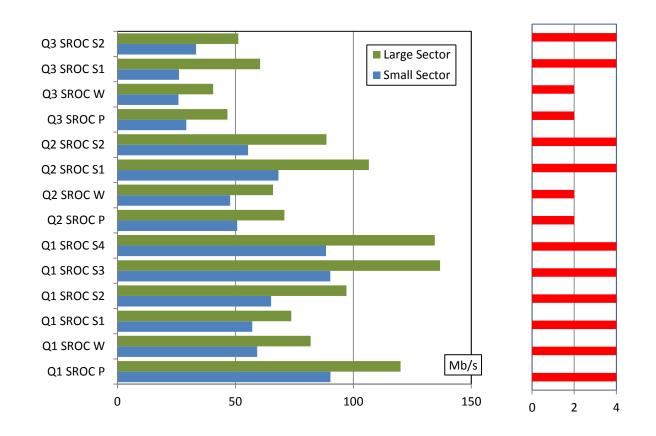
#### Data rates on E-links to GBT

NSW Electronics Trigger & DAQ dataflow



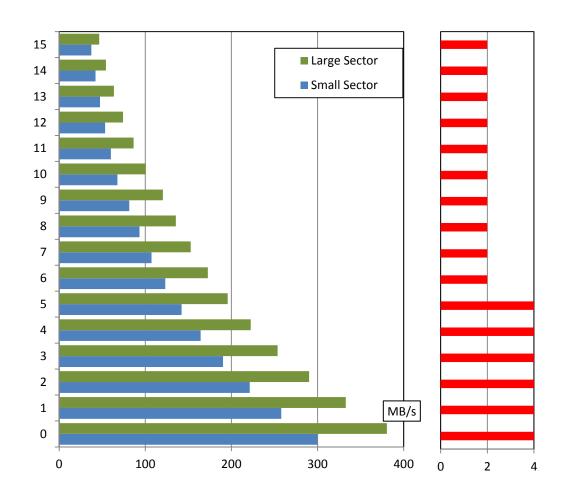
Goal: verify that rates are well below 160 or 320 Mb/s, depending on configuration

## sTGC rates over (S)ROC to GBT E-links



- Rates have been balanced by ad-hoc mapping of VMM to SROC
- Flexibility in n/w configuration, but no more than 8 inputs per GBT
- Worst case: ~47% of available bandwidth

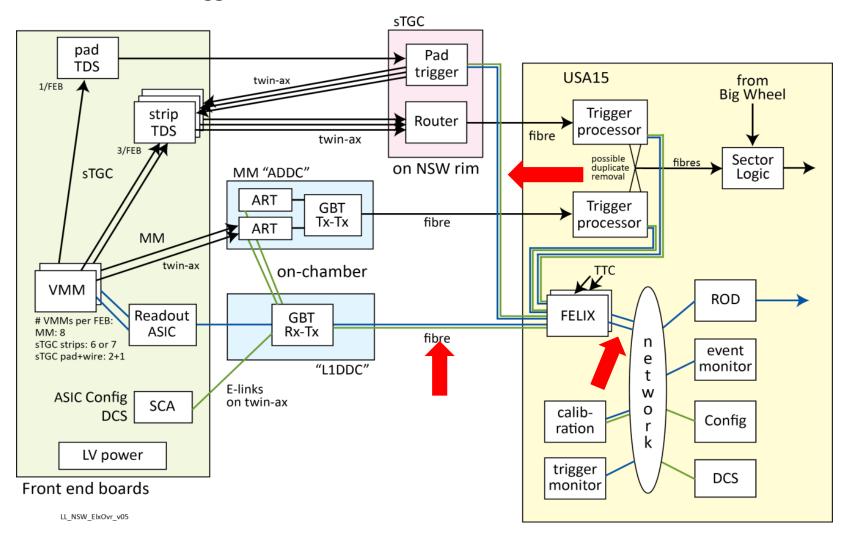
### MM rates over ROC to GBT E-links



- No contingency (actually negative!)
- Wait for a more detailed simulation; if needed, extra links can be added

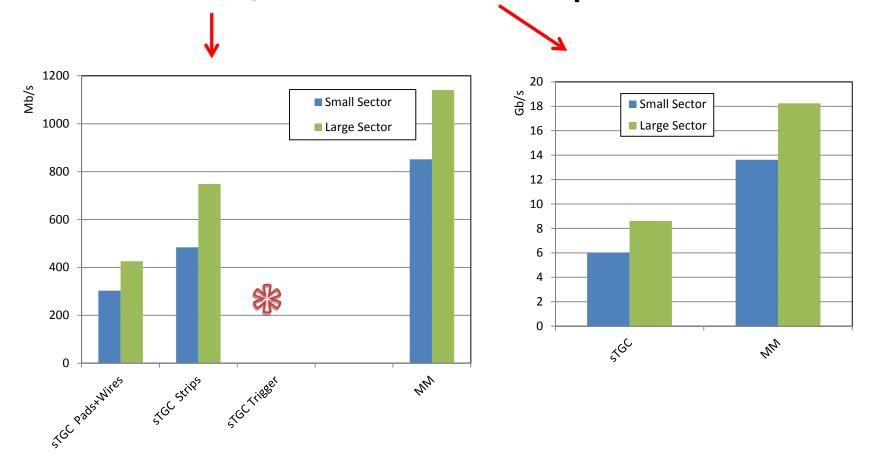
## Data rates of GBT outputs

NSW Electronics Trigger & DAQ dataflow



Goal: verify that GBT rates are below 3.2 Gb/s and FELIX below 40Gb/s

## GBT to FELIX, and FELIX output data rates

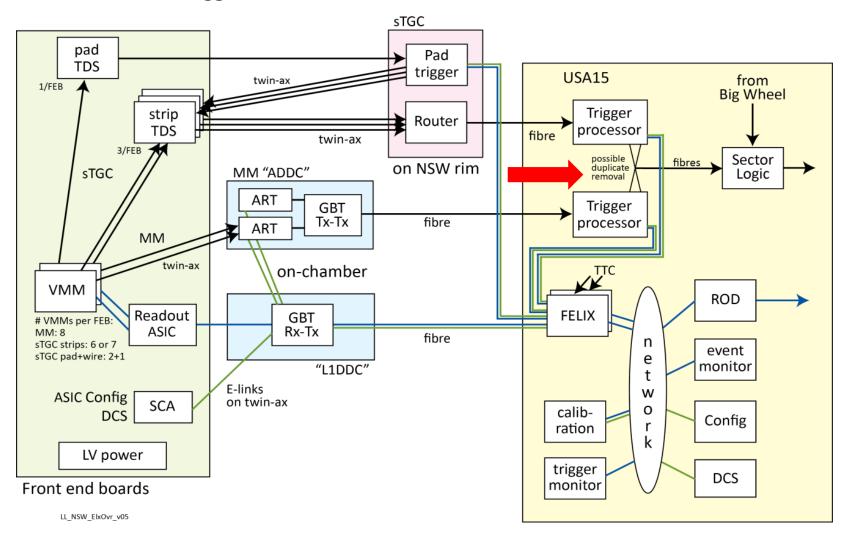


Copious contingency!

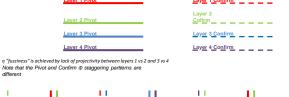
= not yet calculated but very small

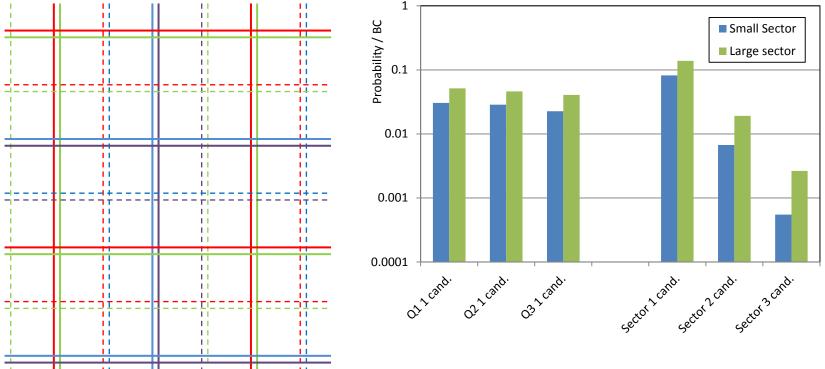
# Trigger processor(s) occupancy

NSW Electronics Trigger & DAQ dataflow



Goal: estimate fraction of trigger candidates lost by processor occupancy





- Estimate probability of 1,2,3 or more sTGC trigger candidates per sector
- Need sophisticated simulation of pad trigger and reliable estimate of angle of tracklets due to correlated background.
  - Waiting for it, assume that at most 30% of corr. background tracks do produce a pad trigger (very preliminary simulation gave 10%)
- The result is: ~10<sup>-3</sup> trigger inefficiency. However, depends on 3<sup>rd</sup> power of rate!

#### Conclusion

No show-stopper identified

 However, some estimates need to be refined by a better simulation

If needed, ad-hoc solutions can be implemented