Preliminary Design Review (PDR) for NSW Electronics

Tuesday 10 February 2015

Tuesday 10 February: On-detector Electronics - 60/6-015 - Room Georges Charpak (Room F) (09:00 - 19:00)

time	[id] title	presenter
09:00	[14] sTGC Router	HU, Xueye
10:00	[15] sTGC pad trigger	VARI, Riccardo
10:45	Coffee	
11:00	[13] L1DDC Card	ALEXOPOULOS, Theodoros
12:00	Lunch	
13:15	[12] MM ADDC Card	YAO, Lin
14:15	[16] LV Power	AMIDEI, Dante
15:30	Coffee	
15:45	[17] VMM3 Readout and ROC ASIC Requirements/Specs	LEVINSON, Lorne MARTOIU, Sorin
17:15	[18] Reviewers' Closed Session	