VETRA – off-line analysis and monitoring software platform for the LHCb VELO

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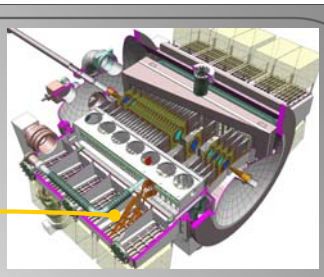
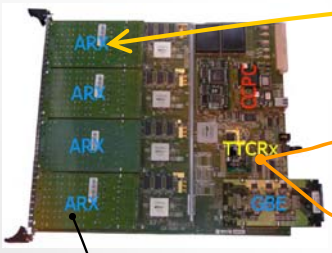
(On behalf of the LHCB VELO group)

→ The two proton beams of the Large Hadron Collider (LHC) will produce copious amounts of B-mesons. This will allow the precise measurement of CP violation. The B-mesons travel on average about 7 mm before decaying into more stable secondary particles. The LHCb VErtex LOcator has been designed to perform accurate reconstruction of the decay position (secondary vertex) of the B-mesons.

→ VELO consists of a row of silicon detectors (21 stations, 82 silicon sensors). The VELO sensors are only 7mm from the LHC beam. They are separated from the primary LHC vacuum only by a thin (300 μm) foil. During beam injection the VELO has to be retracted by 30 mm from the beam.

→ The total number of read-out channels is about 180,000. The RAW data is transported off the detector using 60 m cables to the TELL1 FPGA based acquisition boards where hit reconstruction is performed.





→ The TELL1 read-out board receives the analogue front-end signals from the VELO. The main tasks of this off-detector electronics acquisition board are data synchronization, buffering and zero suppression. The zero suppression (TELL1 processing) procedure, that runs after the digitization, consists of several algorithms implemented within FPGA processors. This allows to suppress the noise in the system and reconstruct clusters. Each board processes data coming from one sensor (2048 channels).

Zero Suppressed RAW BANK

The standard output of the TELL1 board in physics operation are clusters stored in the zero-suppressed (ZS) bank. The clusters objects are then used for track reconstruction.

Non-Zero Suppressed RAW BANK

Unprocessed digitised data can also be readout of the TELL1 board at a low rate. This type of data is critical for VELO commissioning and debugging. The NZS data are necessary to understand the noise measured in the read-out channels, identify noisy or broken channels, perform the detector time alignment and many more applications. In particular this data is needed to tune the TELL1 processing algorithm parameter for optimal cluster reconstruction.

Noise data, test pulse data or physics data

NZS Data

Conversion, Preparation, Decoding

First part of the software processing.

· **Conversion** – raw file transformation from the persistent to transient form (RawEvent object)

· **Preparation** – unscrambling data sectors – the data fragments are bind together randomly by the TELL1 for the performance reason

· **Decoding** – essentially unpacking 10 bit ADC samples that were read out from each channel

NZS Data

The main input stream for the emulation – format identical with the one that is used by the TELL1

VETRA

· Complete Emulation of the complex processing performed in the TELL1 board

· Seven algorithms that require **10^6 parameters** to operate properly

· Input data formatting identical to this used by the TELL1 hardware

· Integrated into official experiment software framework

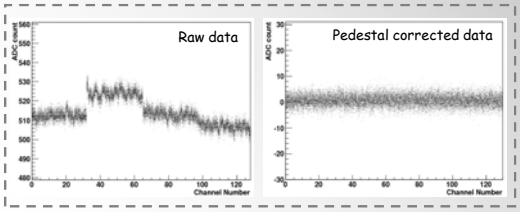
TELL1 Emulation

- Pedestal Following Process
- Front-End chip cross-talk correction
- Cable cross-talk correction
- Common mode subtracion
- Channel Reordering
- Common mode subtraction
- Clusterization

Processing Para Computers

Processing Para Monitoring

Detailed monitoring of the emulation available for each processing step. This gives us the unique possibility of checking the performance of each algorithm in the FPGAs



In the **normal mode** of operation the emulator performs the bit perfect processing of the input NZS data and produces the ZS data bank. These can be passed to the tracking software.

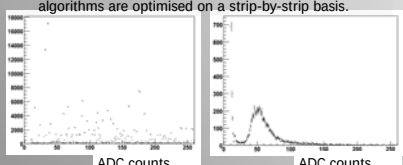
VELOCOND DB

VELOCOND Data Base contains the processing parameters needed to configure and initialize the TELL1 algorithms

Params Retrieving and Processing

A set of dedicated python modules takes care of communicating with Computer Algorithms, retrieving the calculated parameters and updating the VELOCOND DB

Processing **parameter training** is a special mode of the emulator operation. In this case a collection of Computer Algorithms work in combination with the standard TELL1 algorithms. During this phase the parameters for the FPGA algorithms are optimised on a strip-by-strip basis.



Optimising the parameters is critical to the detector performance. The figures show the sum of the charge for reconstructed clusters for a sample of data taken during the 2007 test beam. The left hand side plot has been obtained without tuning the algorithm parameters, the right hand side plot shows the same data after parameter optimisation.

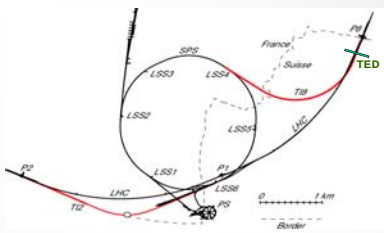
The processing parameters are critical for the VELO operation!

Emulated ZS BANK

The main output stream of the emulator. The emulated ZS bank is identical to the one produced by the TELL1 board for the **BIT PERFECT** Emulation

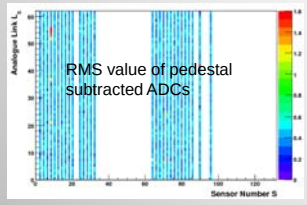
LHC BEAM INDUCED TRACKS SEEN BY THE VELO

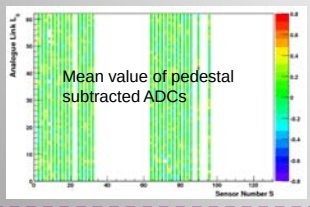
LHC beam synchronisation tests were conducted in August and September 2008. The proton beam was collided with a beam absorber (TED) in the LHC injection line 300m from LHCb. This caused a number of secondary long lived particles to be produced. The tracks were reconstructed by the VELO



First real data tracks reconstructed and displayed by the LHCb software

Detailed monitoring of the processing is performed. A number of dedicated monitoring algorithms checks the performance of the algorithms on the data using the bit-perfect emulation of the FPGA algorithms





Once the processing parameter monitoring confirms their quality the parameters can be uploaded into the TELL1 memory

VELOCOND DB

XML2PVSS