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The GigaFitter: Performances at CDF and Perspectives for Future Applications

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The Silicon-Vertex-Trigger (SVT) is a processor developed at CDF experiment to perform online fast and precise track reconstruction. SVT is made of two pipelined processors, the Associative Memory, finding low precision tracks, and the Track Fitter, refining the track quality with high precision fits. We will describe the architecture and the performances of a next generation track fitter, the GigaFitter, developed to reduce the degradation of the SVT efficiency due to the increasing instantaneous luminosity. The GigaFitter reduces the track parameter reconstruction to a few clock cycles and can perform many fits in parallel, thus allowing high resolution tracking at very high rate.

The core of the GigaFitter is implemented in a modern Xilinx Virtex-5 FPGA chip, rich of powerful DSP arrays. The FPGA is housed on a mezzanine board which receives the data from a subset of the tracking detector and transfers the fitted tracks to a Pulsar motherboard for the final corrections. Instead of the current 12 boards, one per each sector of the detector, the final system will be much more compact, consisting of a single GigaFitter Pulsar board equipped with four mezzanine cards receiving the data from the entire tracking detector. Moreover, the GigaFitter modular structure is adequate to scale for much better performances and is general enough to be easily adapted to future High Energy Physics (HEP) experiments and applications outside HEP.

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