Development of DAQ-Middleware

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- Performance of DAQ-Middleware
- DAQ-Middleware activity at J-PARC
- Conclusions

Feature of DAQ-Middleware

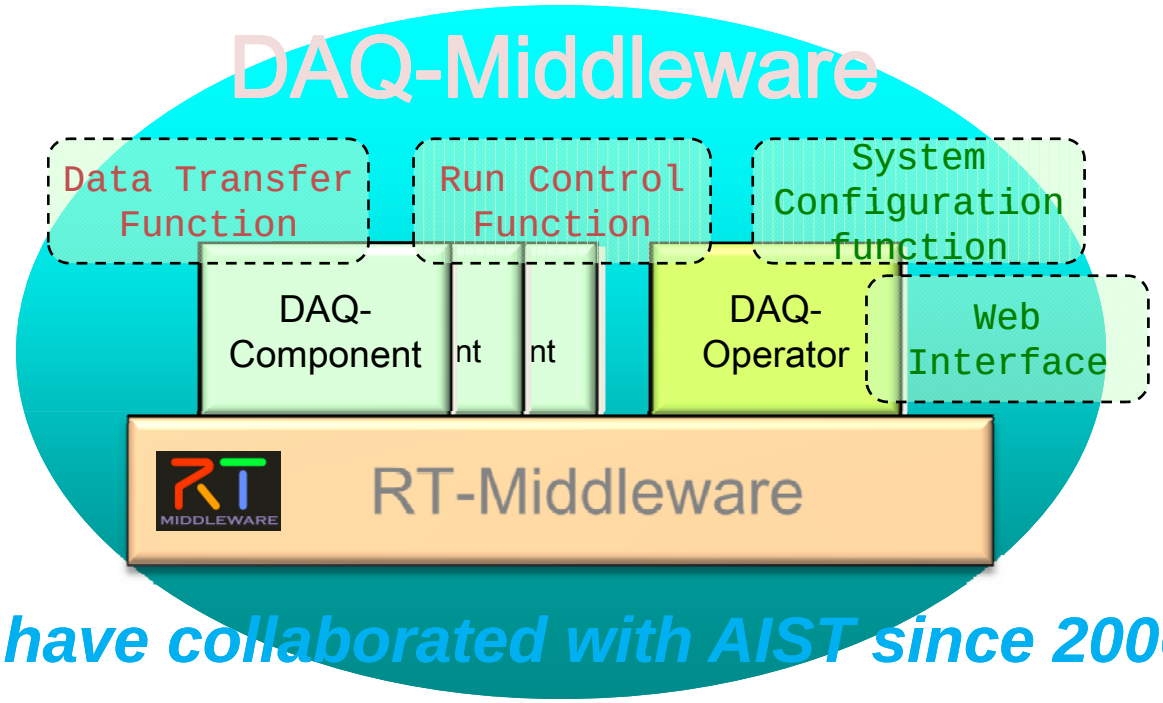
DAQ-Middleware based on RT-Middleware

- DAQ-Middleware is a software framework of network-distributed DAQ system based on Robot Technology (RT) Middleware
- RT-Middleware is an international standard of Object Management Group (OMG) not only for Robotics but also embedded system
- The software package of RT-Middleware was developed by National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba, Japan

DAQ-Middleware based on RT-Middleware (Cont.)

- "The Robot Technology Component Specification "@OMG specifies;
  - Platform-Independent Model (PIM) expressed in UML and Platform-Specific Models (PSMs) expressed in OMG IDL. PIM does not depend on programming languages, operating systems and communication media& protocol. PSM is still independent of programming languages and operating systems.
  - In the OpenRTM-aist implementation of AIST we use, C++ and Python as programming language and CORBA as communication protocol were adopted.
- RT-Middleware will be expected to stop "scrap and building" cycles and make software infrastructure of robotics and embedded system.

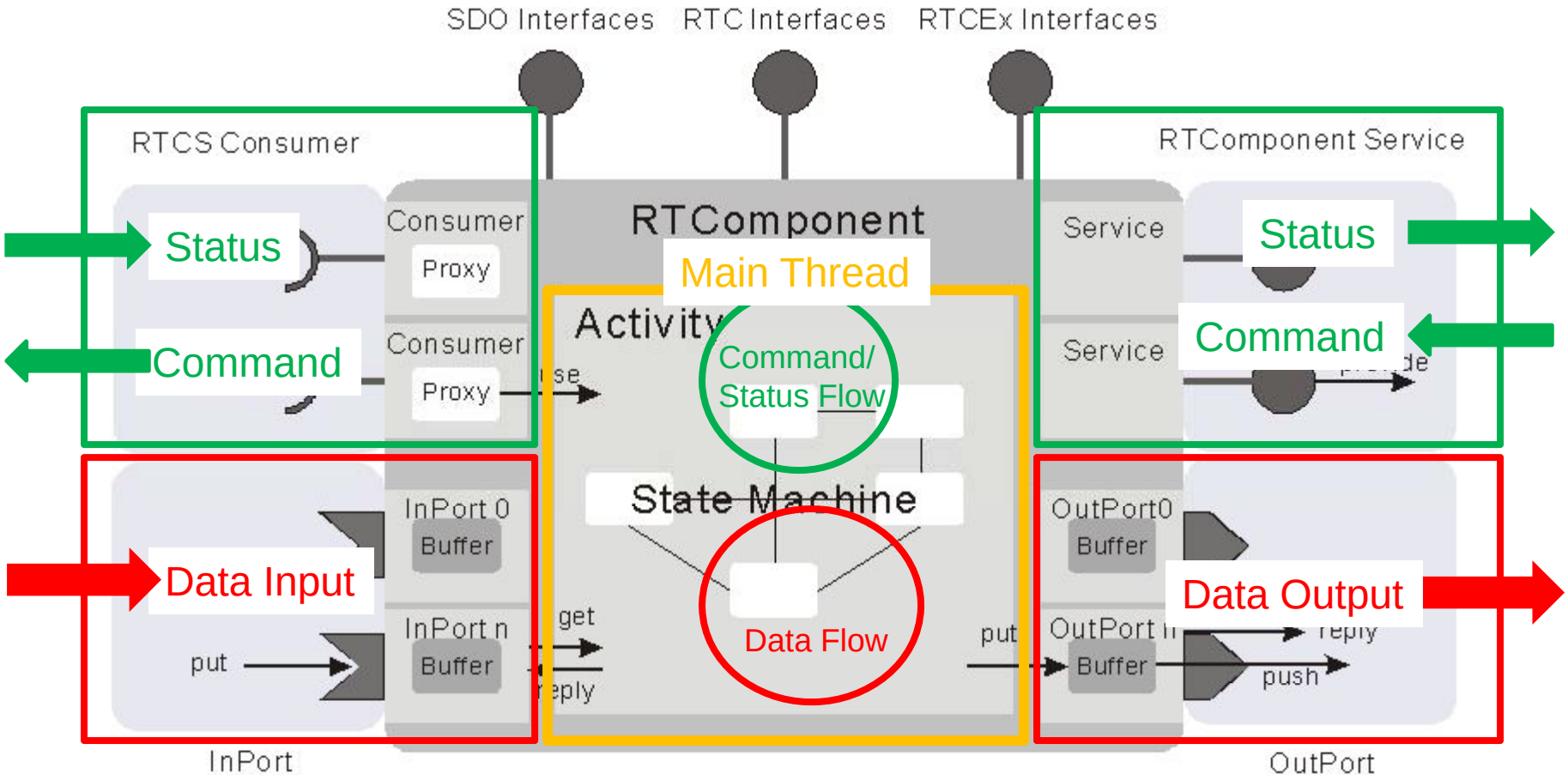
Introduction of DAQ-Middleware



We have collaborated with AIST since 2006.

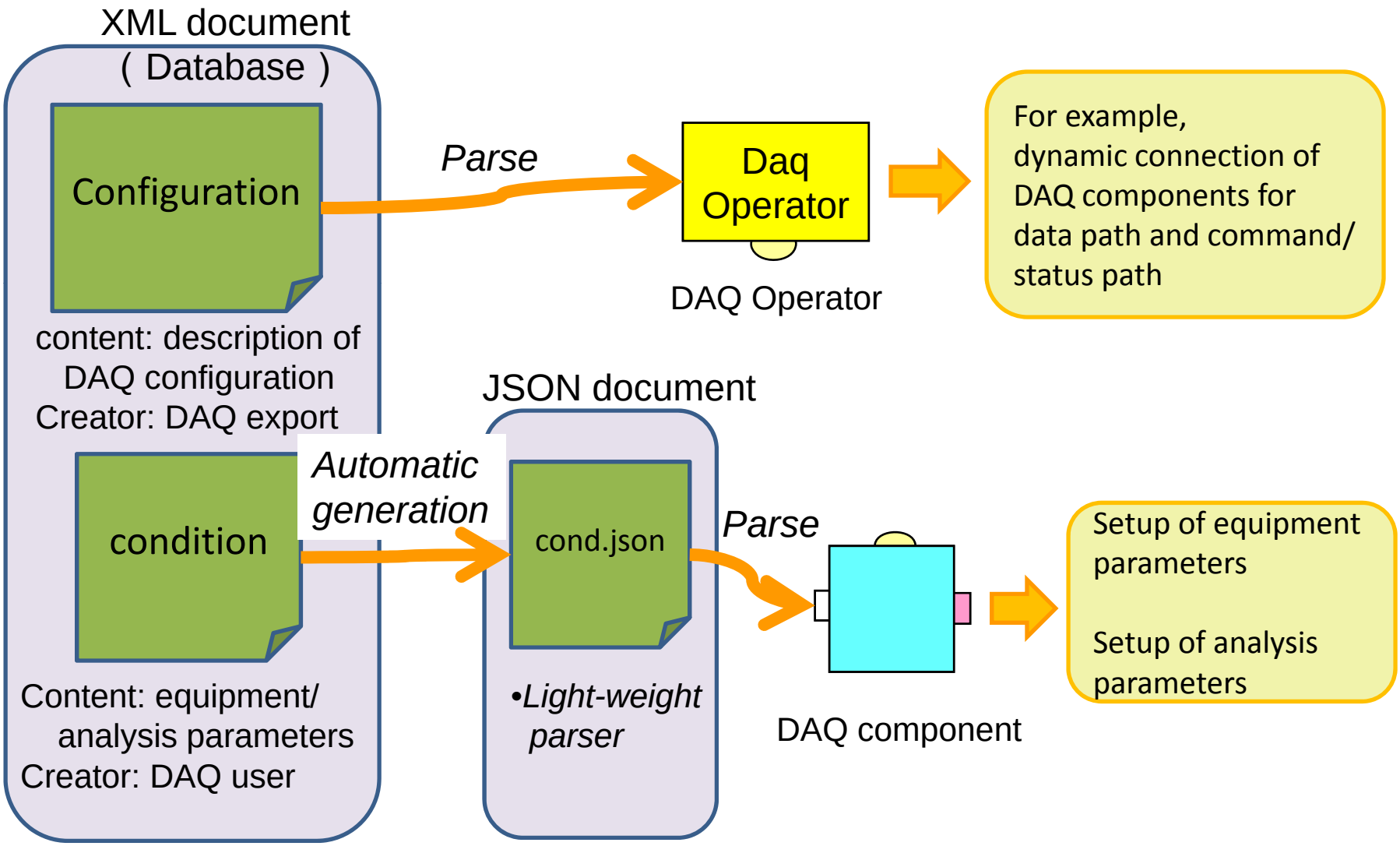
- DAQ-Component is a software unit used to build an integrated DAQ system
- DAQ-Operator is a special DAQ-Component which controls other DAQ-Components
- The databases for system configuration (configuration database) and equipment parameters (condition database)
- Web interface(XML/HTTP protocol) as system interface to external world
- Booting mechanism of DAQ-Components over network

Autonomous component model

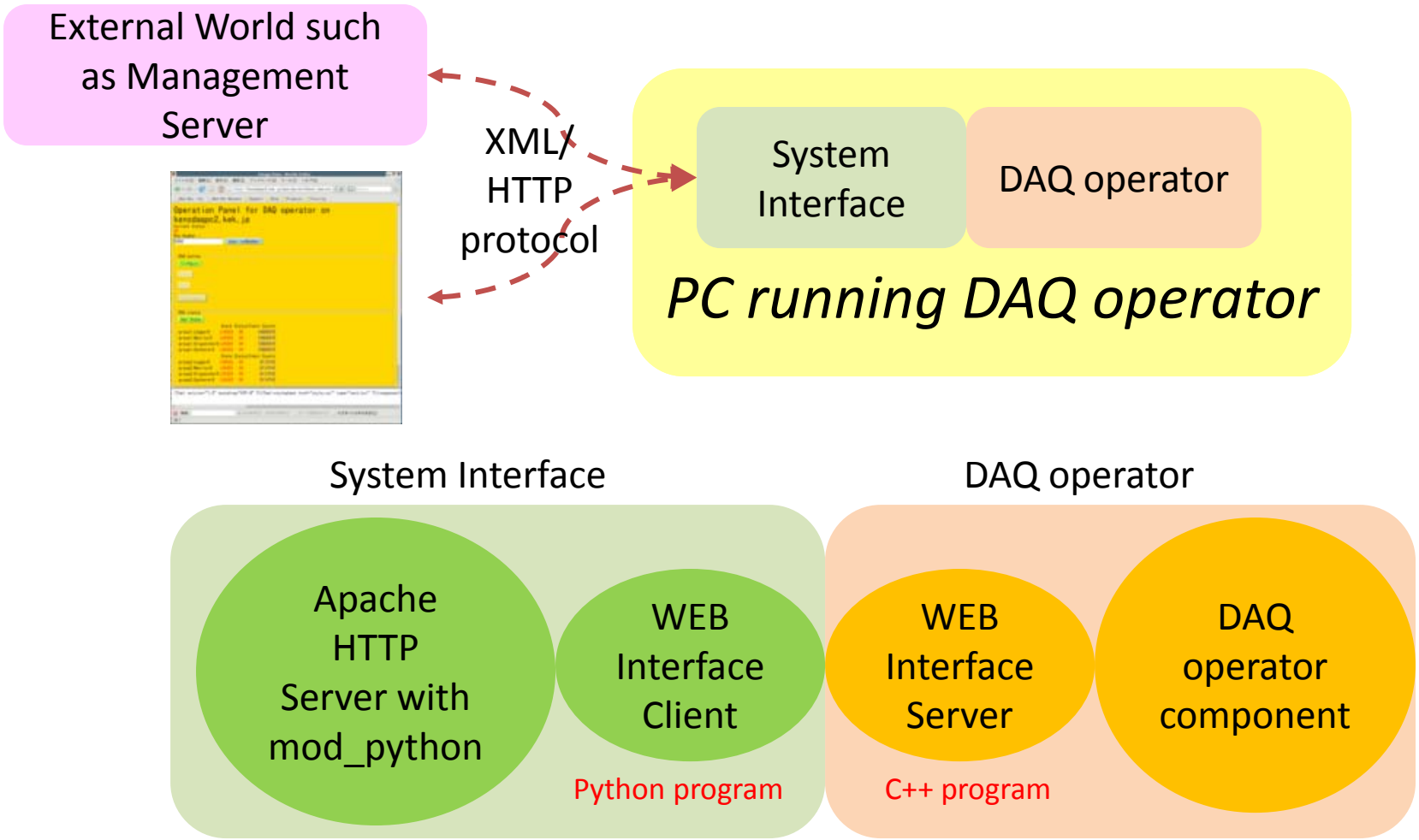


- Data Port and Service Port are used for Data path and command/status path, respectively
- Autonomous main thread is used for core logic

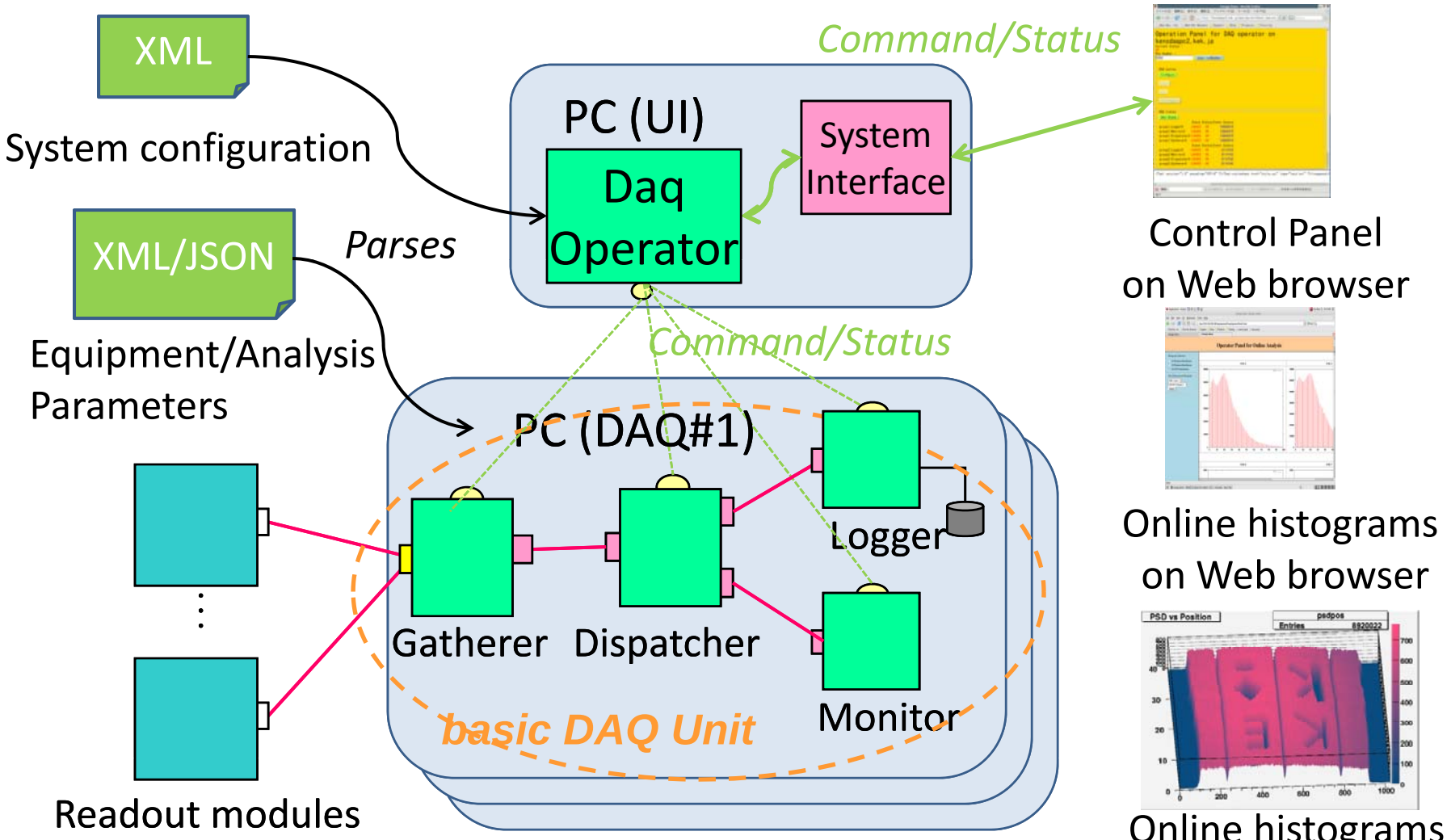
Configuration/condition database



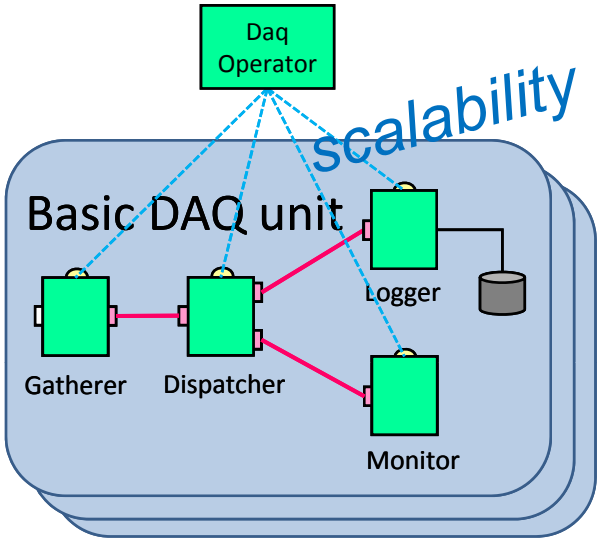
System interface

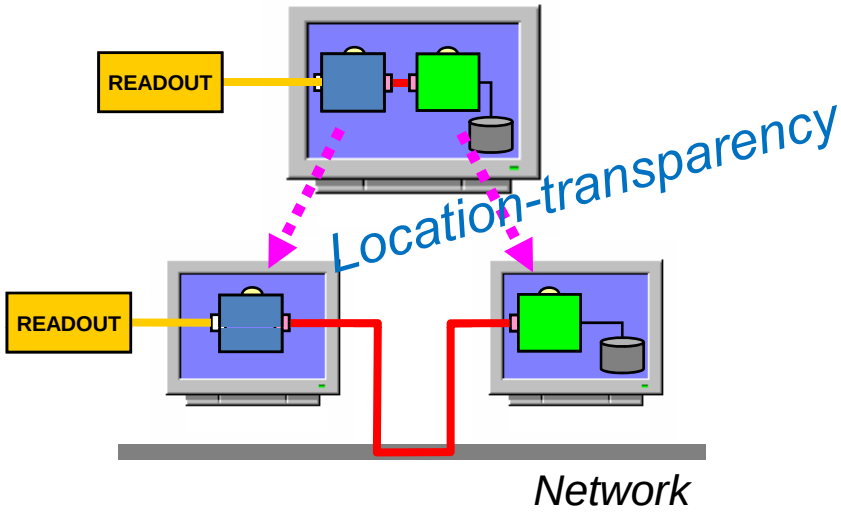


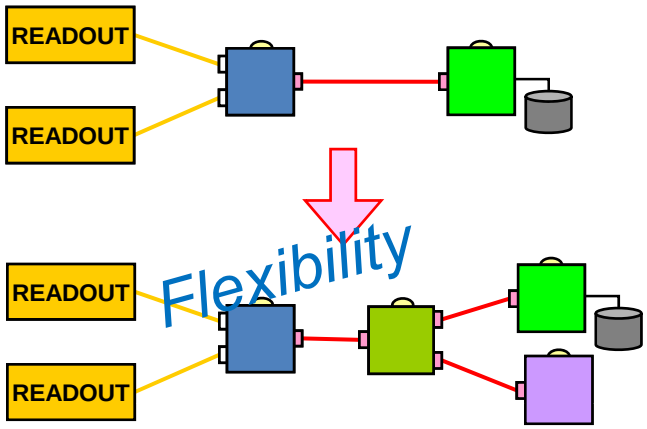
An architecture of DAQ-Middleware based system

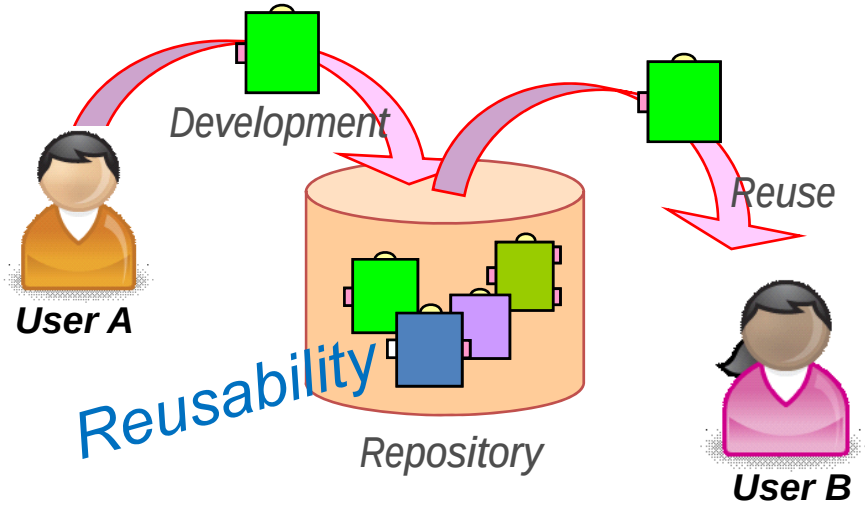


Summary of features









Performance of DAQ-Middleware

Purpose of measurement

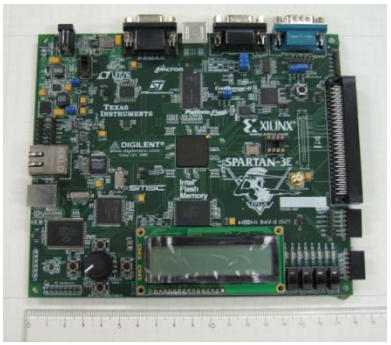
- To measure the total throughput of a basic DAQ unit of DAQ-Middleware for MLF's requirements (first target experiments)

Requirements:
1. Basic DAQ unit
-Gatherer, Dispatcher, Logger and Monitor components on a PC
-A readout PC governs a VME crate (20 modules)
-Max. throughput on the module is 1.28MB/s
-A module has 8 channels of Position Sensitive Detector(PSD)
-Max. event rate of a PSD: ~20kcounts/s (160kB/s)
2. Total throughput(average) is about 30MB/s on multiple DAQ units
3. Acquired data are stored into files in unit of the module

Equipment for readout used by measurement

- Typical detector for MLF/neutron experiments is PSD
- NEUNET is the readout module with SiTCP
  - SiTCP: a hardware-based TCP processor
- NENUET emulator with traffic shaper is really used for the measurement

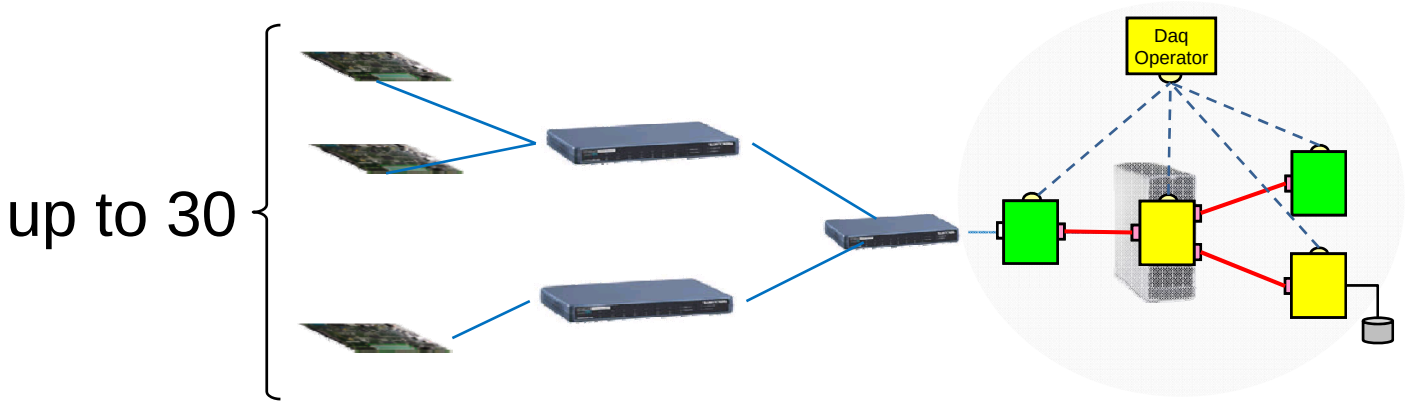

NEUNET and PSD



NEUNET emulator

Testbed and Setup

- NEUNET emulator
  - Xilinx Starter Kit x 30
- Network switch
  - Cisco Catalyst 2960G-24TC-L x 2
  - Cisco Catalyst 2960G-8TC-L x 1
- PC(HP xw8600)
  - CPU: Quad-Core Xeon x 2



The parameters

PC: HP xw8600

CPU: Quad-Core Xeon E5420(2.5GHz/12MB x2)

Intel 5400 Chipset(1333MHz/1600MHz FSB)

memory: 16GB

Disks: HITACHI HDS721010KLA330

1TB/32MB Cache/7200rpm/SATA 3GB/s) x 4

OS: Red Hat Enterprise Linux Client release 5.3

kernel: 2.6.18-128.1.1.el5PAE

gcc: gcc version 4.1.2 20080704 (Red Hat 4.1.2-44)

File System: Ext3

I/O Scheduler: Anticipatory

Kernel Parameters

/proc/sys/net/ipv4/tcp_rmem 4096 4194304 4194304
/proc/sys/net/ipv4/tcp_wmem 4096 65536 4194304

For Network

/proc/sys/vm/dirty_background_ratio 1 or 10(default)
/proc/sys/vm/dirty_expire_centisecs 2999
/proc/sys/vm/dirty_ratio 40

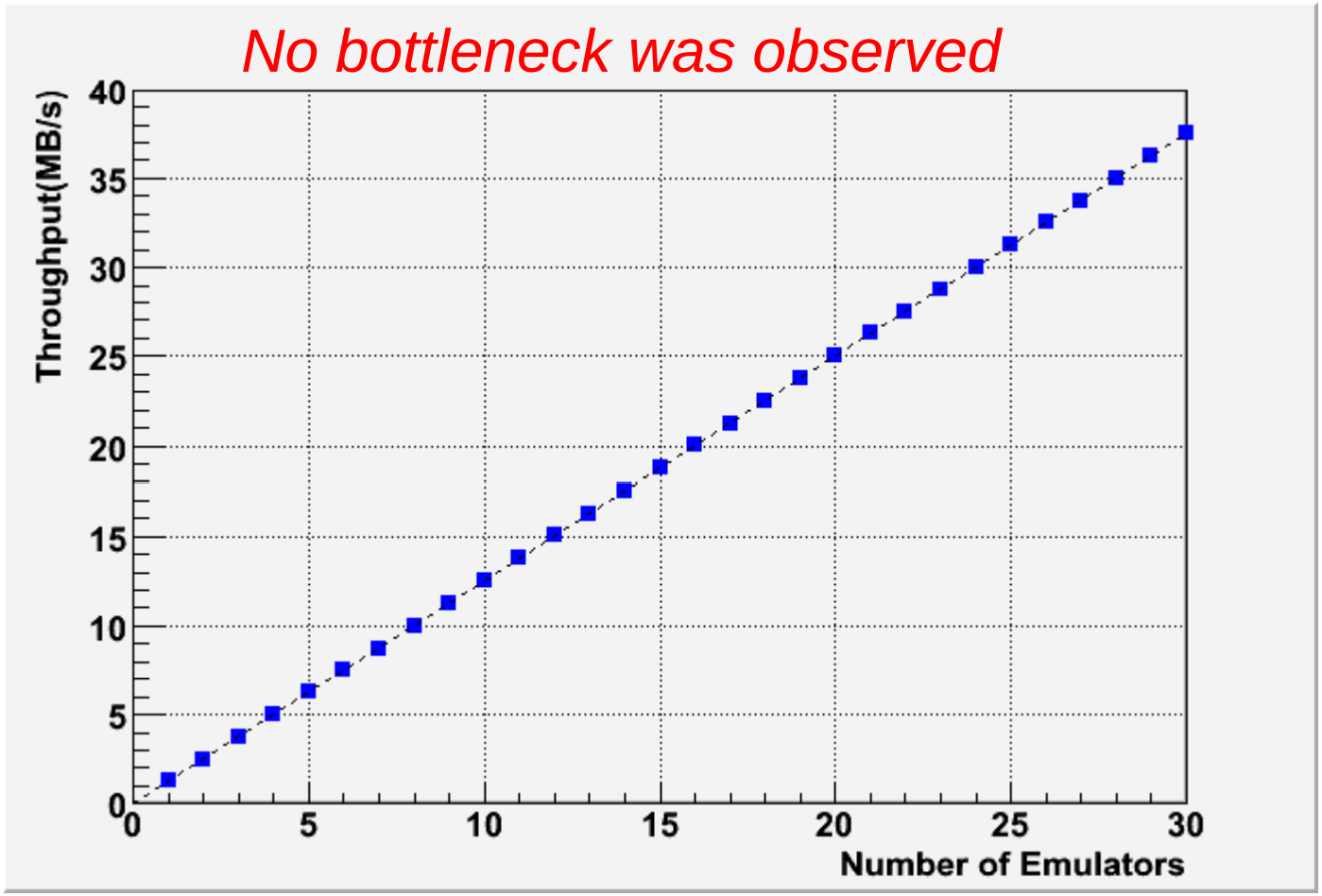
For Disk I/O

The conditions

- Three data logging conditions:
  - No logging
  - Logging with single disk
  - Logging with striping disks (four disks)
- Changing a kernel parameter
  - vm.dirty_background_ratio: 1, 10(default)
- The emulators used from 1 to 30
  - data rate at an emulator is 1.28MB/s

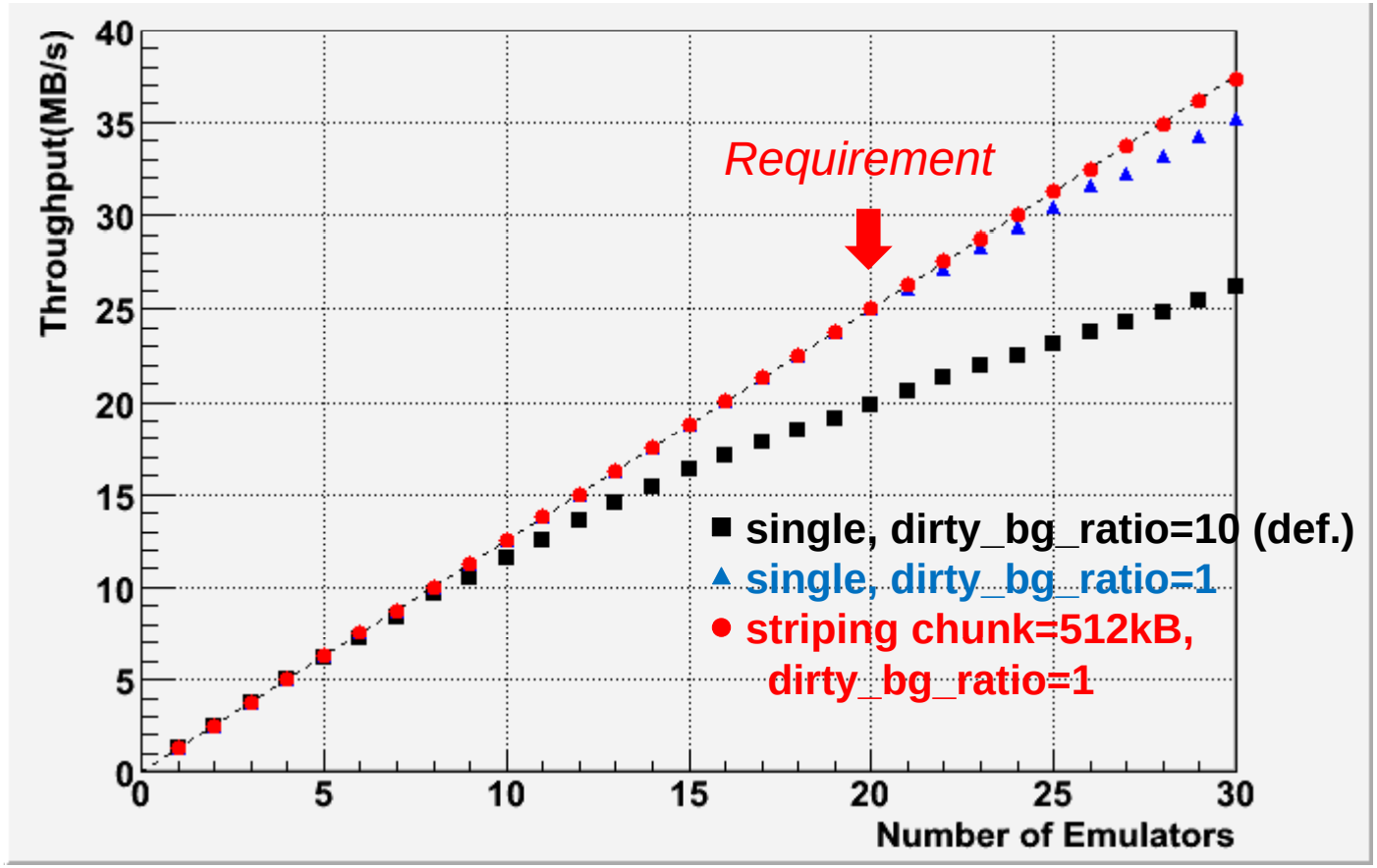
dirty_background_ratio means:
a percentage of total system memory, the number of pages at which the pdflush background writeback daemon will start writing out dirty data.

Total throughput w/o data logging



Total throughput w/ data logging

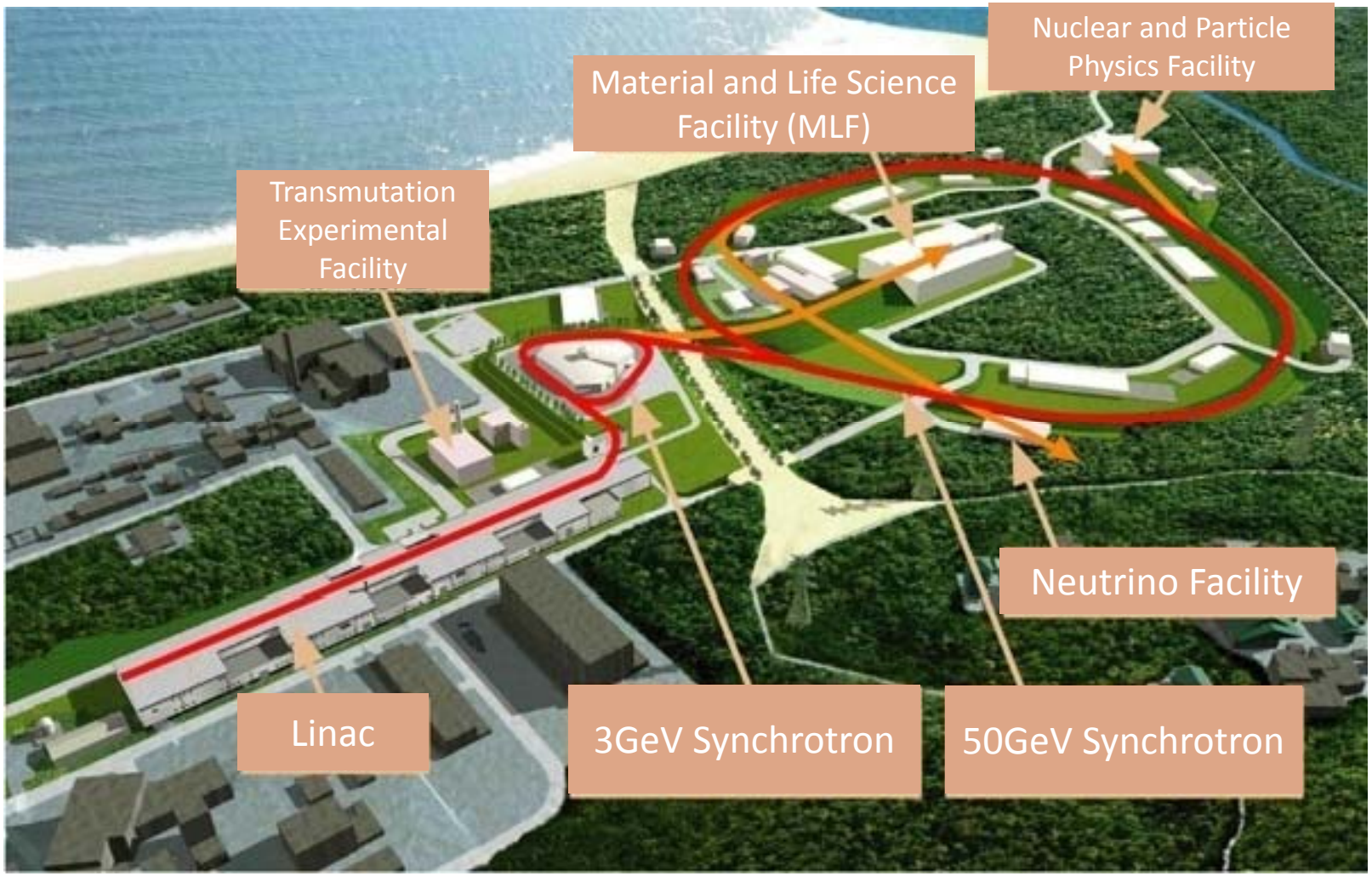
The result could satisfy the requirement from MLF



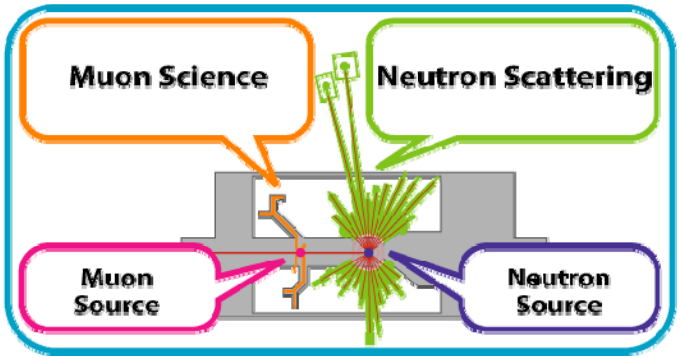
DAQ-Middleware activity at J-PARC

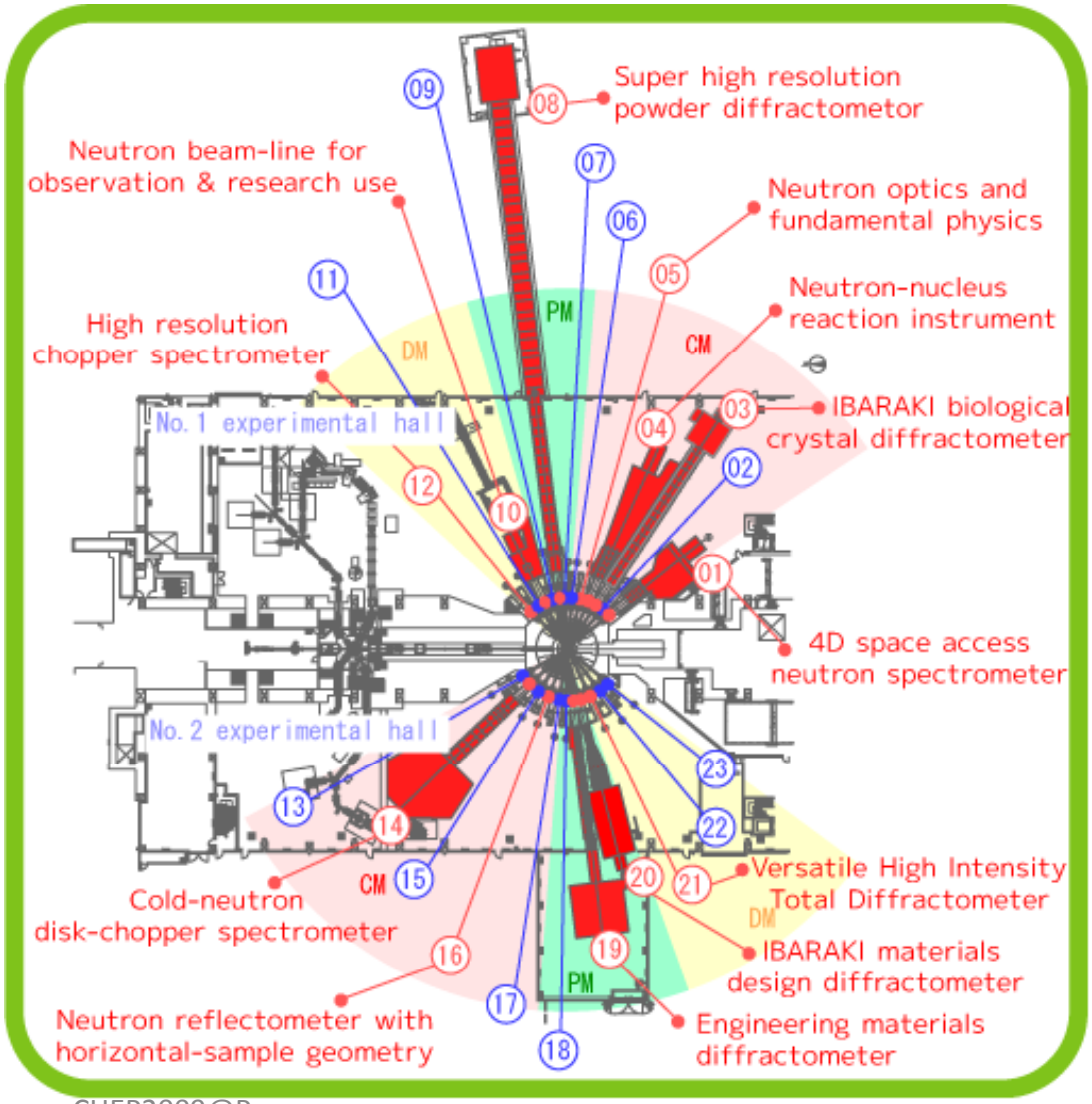
J-PARC

Japan Proton Accelerator Research Complex



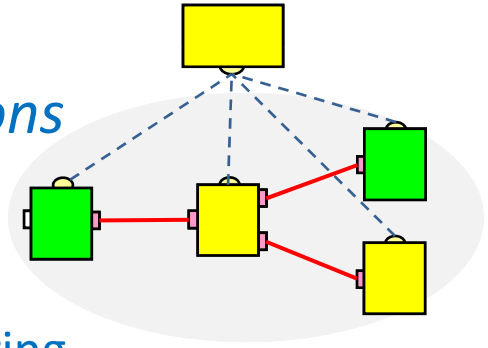
Material and Life Science Facility(MLF)



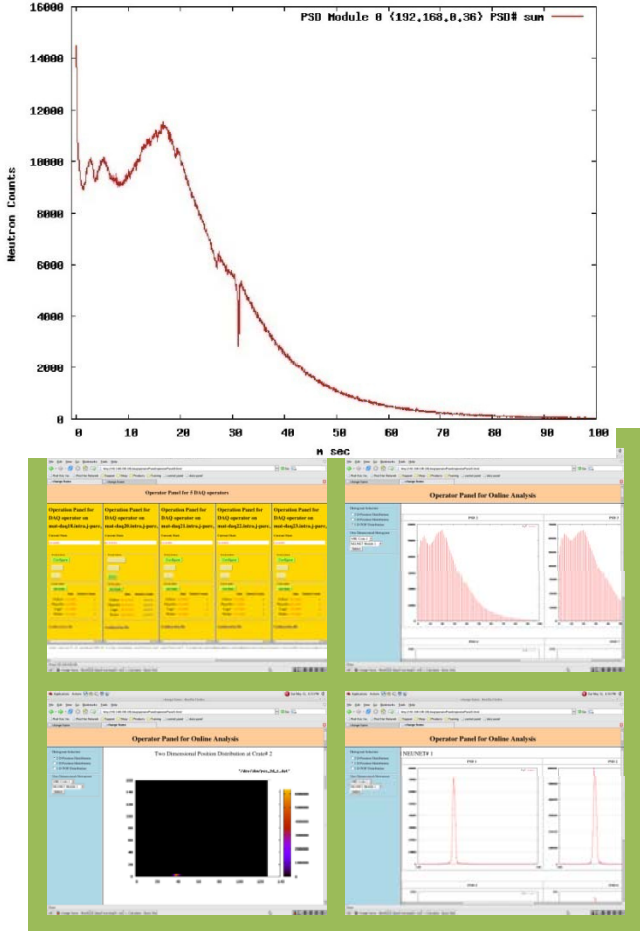


Commissioning on Neutron Beamline

- Commissioning was carried out following items at iMATERIA (IBARAKI material design diffractometer), Beam Line 20 (BL20) on MAY 2008, First beam of Neutron
  - Electronics
  - DAQ-Middleware
  - Software Framework(called Working Desktop)
  - Offline analysis
- *DAQ-Middleware functions*
  - data readout/storage
  - Web-enabled run control
  - Web-enabled Online monitoring
    - (2-d histogram, TOF, position)



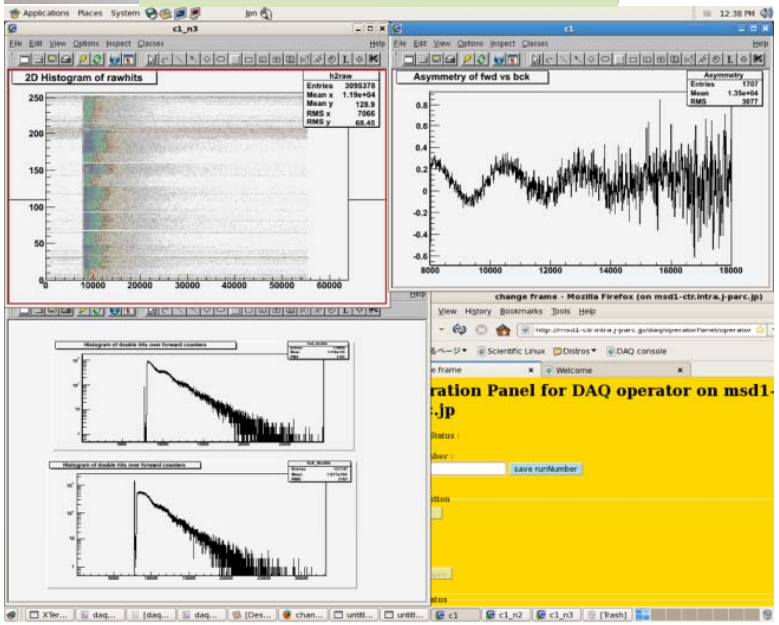
a basic DAQ unit

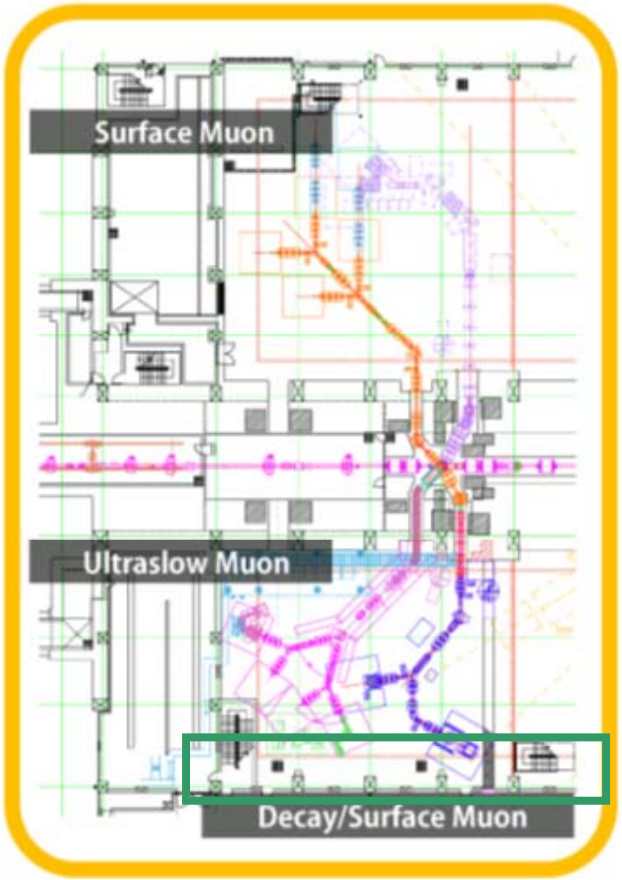


Commissioning on Muon beamline

First beam of muon (2008/ 9) :Data Taking with DAQ-Middleware

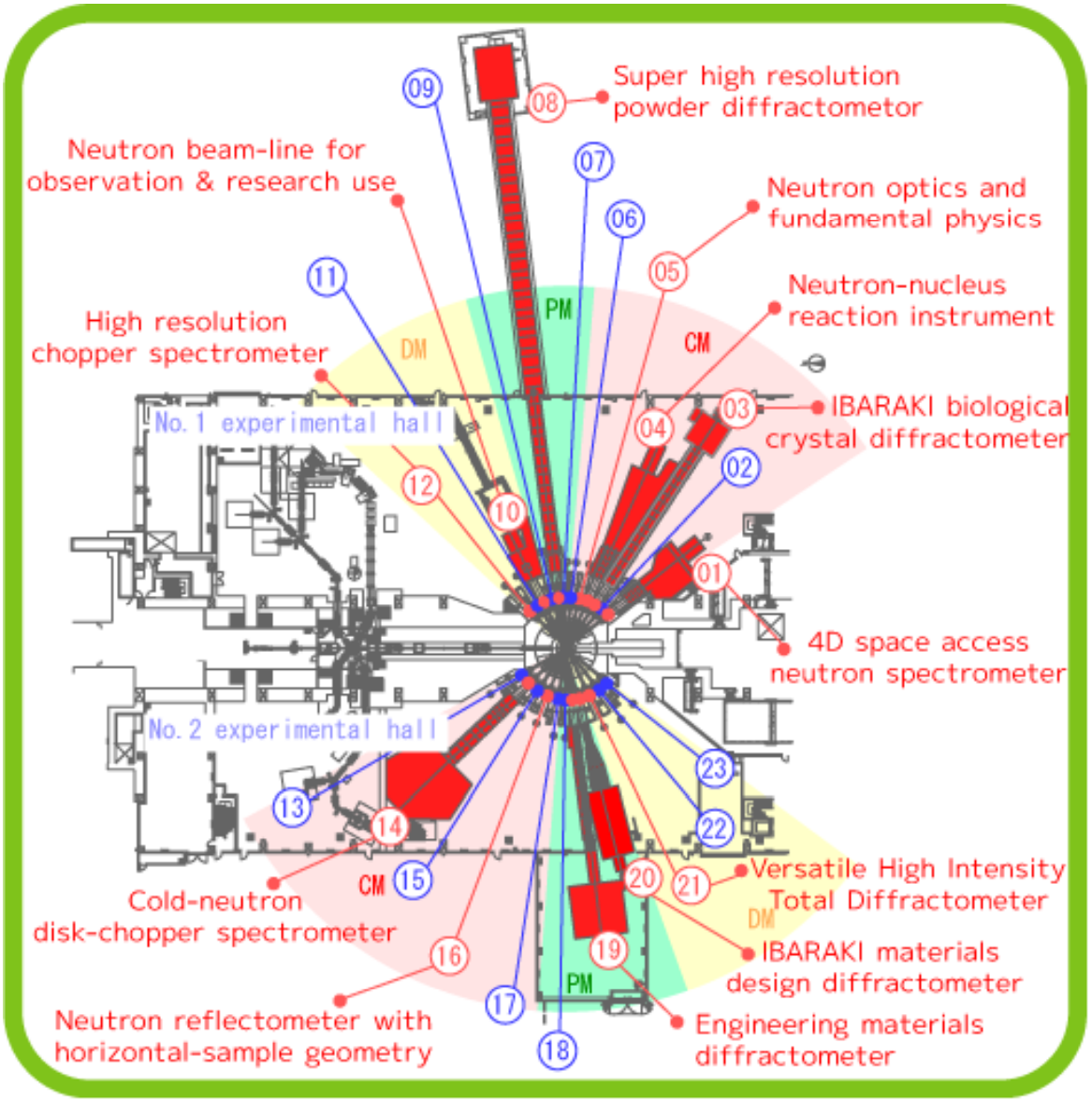
Detector:256ch
Scintillators/PMTs





DAQ : DAQ-Middleware
Analysis tool: ROOT

Current status of MLF/Neutron(Mar. 2009)



Groups in DAQ-Middleware operating / ready phase : 5 groups

- ***BL01***
- ***BL03***
- ***BL19***
- ***BL20***
- ***BL21***

Groups in DAQ-Middleware preparatory phase : 7 groups

- ***BL02***
- ***BL08***
- ***BL11***
- ***BL12***
- ***BL14***
- ***BL15***
- ***BL16***

conclusions

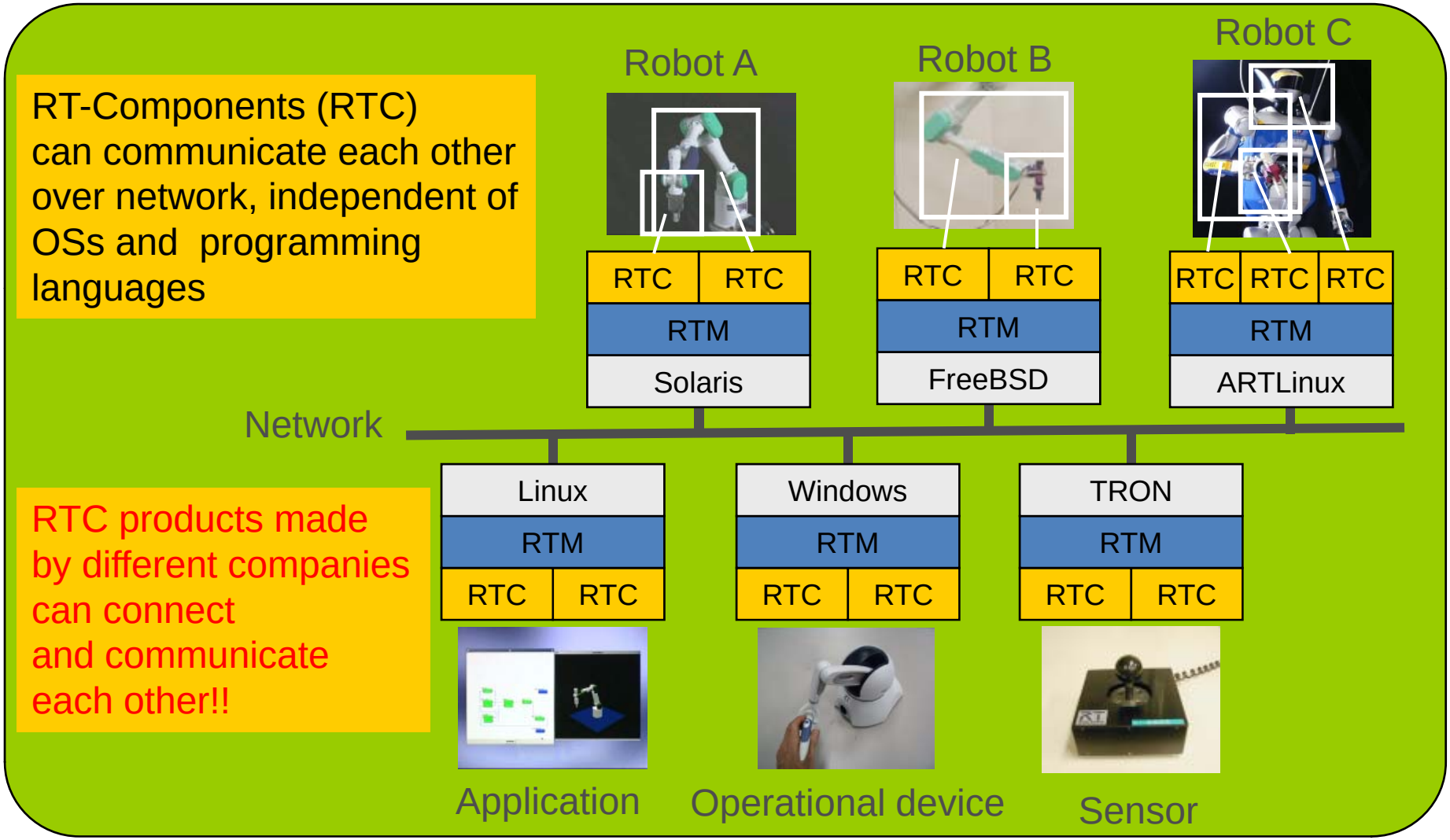
- We have developed DAQ-Middleware which could be applied to real experiments.
- We have applied experiments of MLF and have met the requirement.

Acknowledgements

- We wish to thank Prof. J. Haba at KEK for his support of this project. This work was performed in next generation DAQ sub-group of the KEK Detector Technology Project at KEK.
- We also thank staff of experimental groups at MLF and KEK electronics system group for their help.

backup

A system based on RT-Middleware



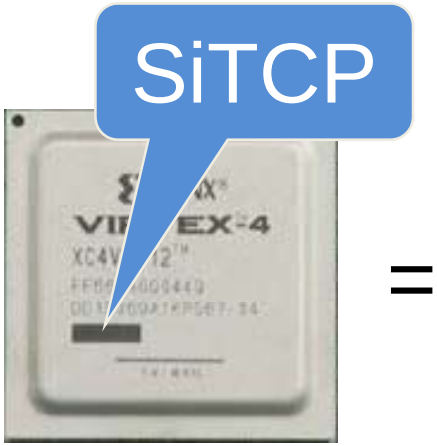
Introduction of SiTCP

Technology connecting to small device such as front end with high speed!

Ethernet PHY device

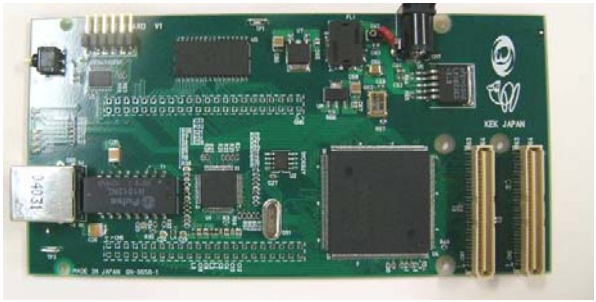
10Mbps, 100Mbps, Gigabit

+



FPGA

=



Small board

without CPU

Capability of communication with TCP/IP on Ethernet

Feature of SiTCP