Overview of BeamCal ASIC

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Hardware WG meeting

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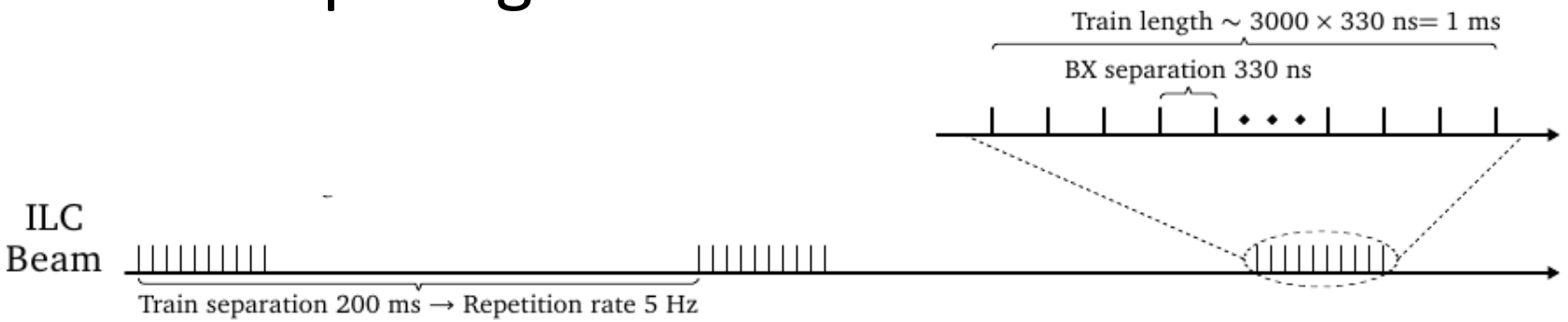
Outline

- Beamcal specs
- What has been done
- What we are working on
- Next steps

BeamCal general specs

- Radiation-hard detector
- Segmentation: ongoing work (Sergej, Lucia)
- Input cap: up to ~20pF (detector) + ~20pF (wire)
- Bunch spacing: 330ns
- Train length: ~3000 pulses (1ms)
- Train spacing: 200ms



BeamCal old specifications (2010)

Physics mode

- 10-bit resolution front-end
- Linear ADC
- Max input charge: 40pC
- Occupancy: 100%
- 10-bit Fast-feedback output
- Electronics calibration option

Calibration mode

- 10-bit resolution front-end
- Max input charge 900fC
- Occupancy: 100%
- Electronics calibration option

BeamCal new specifications

Physics mode

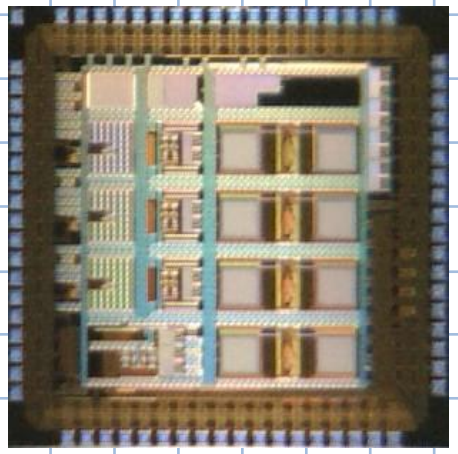
- **13-bit** resolution front-end
- **Nonlinear ADC (9 bits)**
- Max input charge 40pC for 500GeV option
- Occupancy: 100%
- 10-bit (?) Fast-feedback output
- Electronics calibration option

Calibration mode

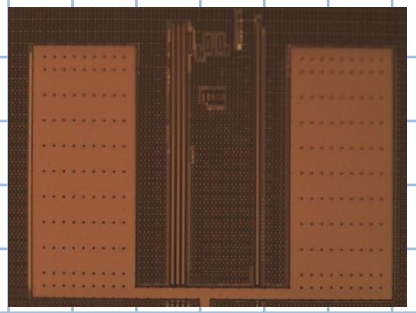
- 6-bit (?) resolution front-end
- Max input charge 4.3fC (?)
- Occupancy: TBD **(this is critical)**
- Electronics calibration option

What has been done (1/2)

- 2010: The Bean 1.0 (3 channels)
  - 180nm mixed-signal CMOS process
  - Meets most old specs
    - Exception: SNR in calibration mode
  - Starting point for future designs

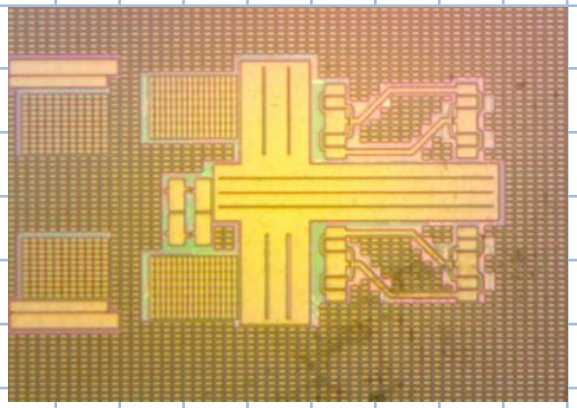


- 2012: Test ADC
  - Another 180nm mixed-signal CMOS process
  - Proof-of-concept for ADC nonlinearity control



What has been done (2/2)

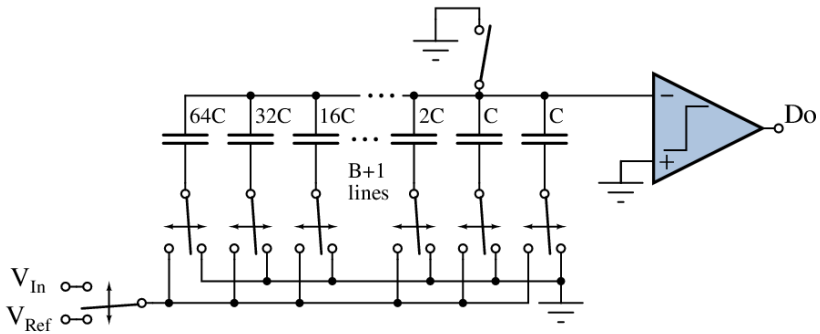
- 2012-2013: development of multiple sampling noise calculation
  - Interesting theory, still some room for more work
- 2014: The Bean 2.0
  - Yet another 180nm process
  - Stripped-down version
    - Only 1 channel
    - Lacks ADCs
  - Arbitrary weighting function generation
    - Multiple sampling concept
  - Currently under test

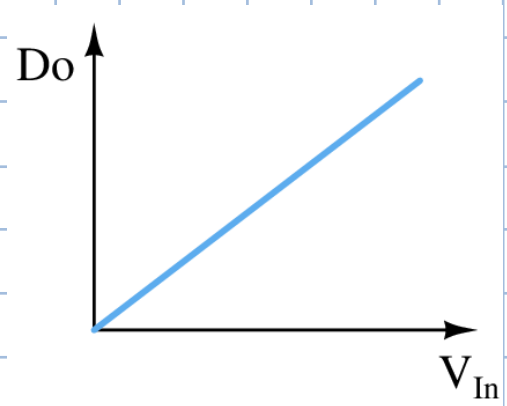


What we are working on

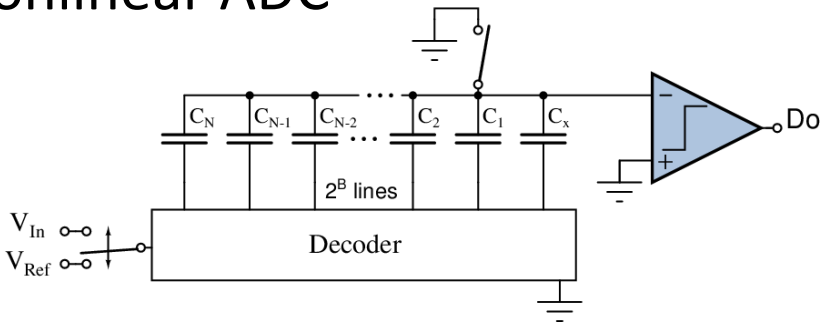
Intentionally nonlinear ADC design

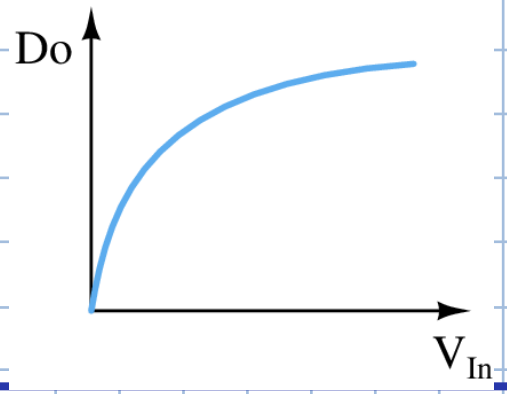
Linear ADC





Nonlinear ADC





Next steps

- Develop nonlinear ADC concept
  - Publish results
- **Converge to a common FCAL fab process**
- Design chip to test nonlinear ADC concept (2015)
- Design new front-end (2015-2016?)
  - Stringent noise specs
- Have a working, 8-channel Bean ASIC prototype (2017?)
  - Designed for new set of specifications

Thank you for your attention