AGH University of Science and Technology

Overview of readout ASICs for LumiCal detector

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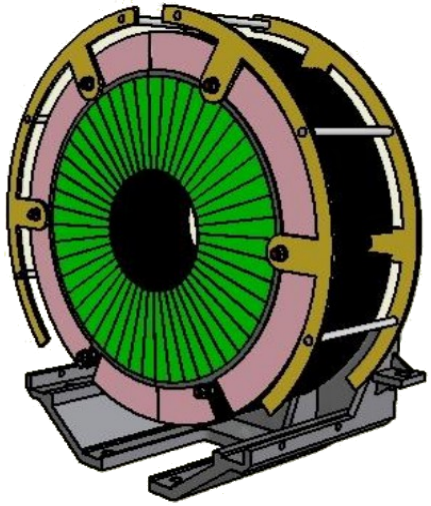
Outline

- The Goal
  - What we want to do...
- A bit of history
  - What has been done and where we are...
- Ongoing works and Future
  - What we are doing now, our plans...
- Summary

The Goal



Our Goal is to develop dedicated readout ASICs detecting and processing signals from ~200 000 channels of LumiCal calorimeter at future Linear Collider.

LumiCal design sets requirements/constraints on:

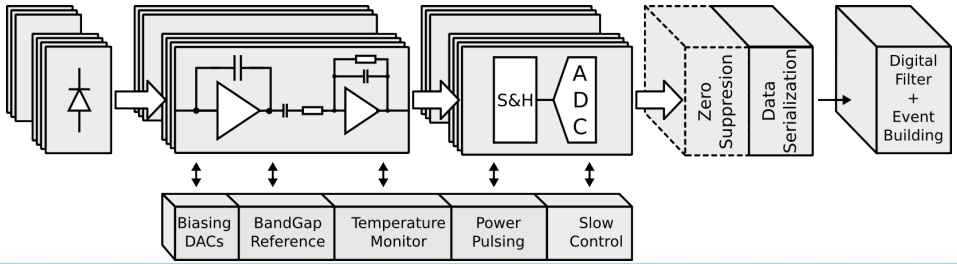
- ASIC architecture: System on Chip (SoC), with all possible functionalities inside, in order to eliminate external components and fascilitate the design of COMPACT Calorimeter
- Signal amplitude: $10^0 \div 10^5$ fC
- Sensor capacitance: 5 ÷ 35pF
- Speed: Impuls contained in ~ 350 ns (ILC)
- Average power dissipation: $<10^2$ W/barrel ?
- Noise: Signal-to-Noise > 10 for MIP

The Present Goals for LumiCal ASICs Architecture and Specification

Present goals are rather related to test-beam and ILC requirements. They do not need to be exactly the final ones. I assume that the architecture is the final one, while the specification/implementation of certain blocks, may still evaluate...

Architecture

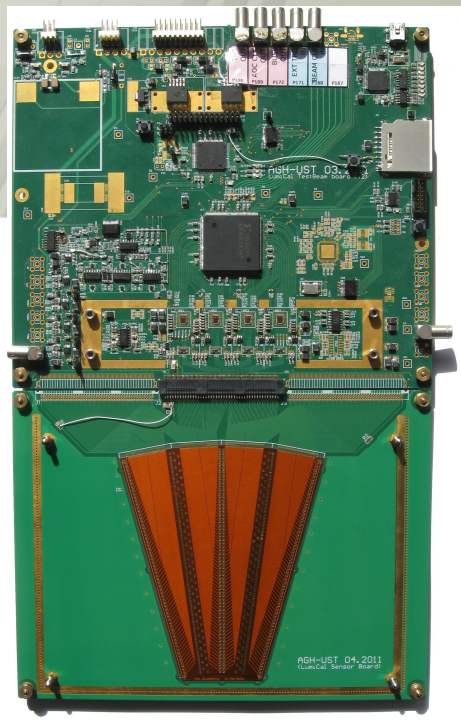
- Multichannel ASIC
- SoC type ASIC comprising signal processing blocks, plus all needed interfaces and peripheral blocks
- Analog front-end and ADC conversion in each channel
- DSP (in the future?) plus serialization and fast signal transmission



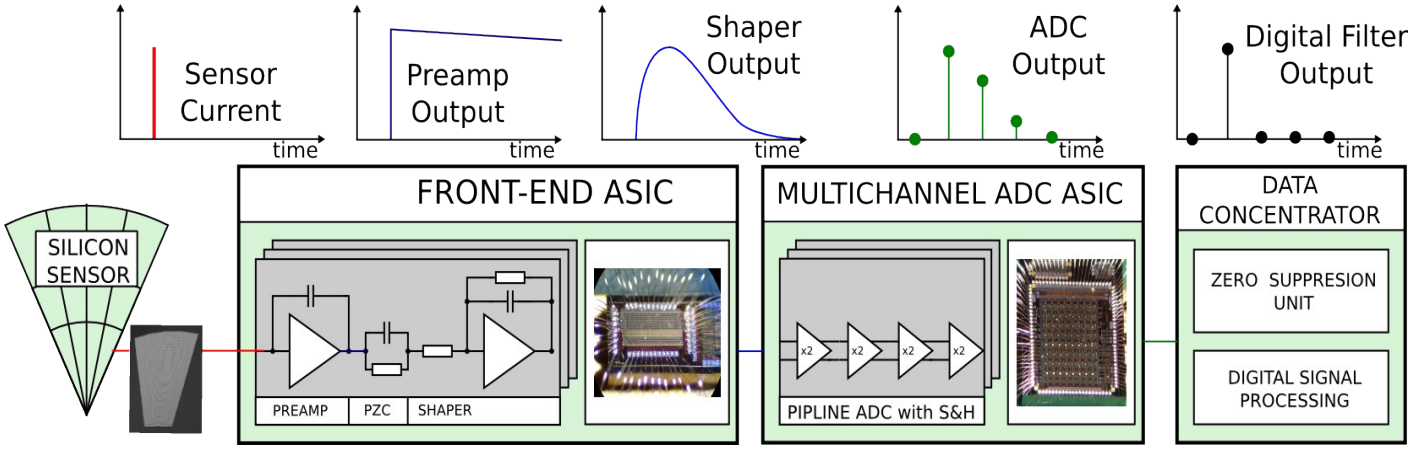
Specifications

- CMOS 130 nm technology
- 8-64 channels ?
- Sensor capacitance $C_{det} \approx 5 \div 35pF$
- Variable gain:
  - calibration mode: MIP sensitivity
  - physics mode: input charge up to ~6 pC
- CR-RC shaping with $T_{peak} \approx 50$ ns
- 10-bit signal resolution
- Fast ADC (~20MHz) for asynchronous operation and possibility of deconvolution
- Peak power cons. few mW/channel
- Power pulsing, avr. power <100uW/chn.
- Noise: ENC ~ 1000e^- @10pF

A bit of history and present status
Present LumiCal readout chain



We have developed at AGH-UST a first version of readout based on the proposed architecture. The ASICs are fabricated in rather old AMS 0.35um CMOS technology



A 32 channel LumiCal detector module was built. Readout comprises:

- 8 channel front-end ASIC with preamp & CR-RC shaper Tpeak~60ns, ~9mW
- 8 channel pipeline ADC ASIC, Tsmp<=25MS/s, ~1.2mW/MHz
- FPGA based data concentrator and further readout

Existing LumiCal readout module was used on several test-beams with LumiCal and BeamCal sensors. For last test-beam we managed to integrate and run four LumiCal planes. We are eagerly waiting for the results of analyses !!!

A bit of history and present status
Where we are ?

Detector Module:

- The existing module was good enough for FCAL first test-beams, but its design does not allow to make a COMPACT calorimeter prototype, which is the main FCAL Goal!
  - Design of Detector Module is not COMPACT,
  - ASICs need too many external components (e.g. biasing) to make the readout compact.
- Both, ASICs and Detector Module, need to be improved!

ASICs:

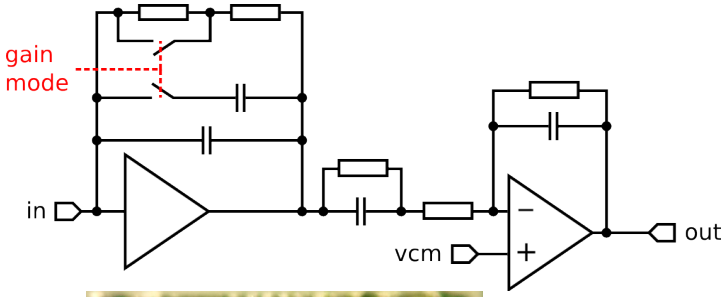
- We consider the existing readout ASICs to be the end of development based on AMS0.35um,
  - The main reason to develop ASICs in AMS0.35um was limited amount of money. Choosing AMS0.35um we were conscious about its limitations (e.g. regarding power consumption or radiation hardness),
- Two years ago we have started an ASIC R&D with new, hopefully FINAL, CMOS 130 nm technology for LumiCal readout,
- Few years ago the development of dedicated BeamCal ASIC has also started within FCAL, initiated by Angel group,
- We have been discussing with Angel that, for various reasons, the best solution for FCAL would be to use the same technology, and even more, to share some of electronic blocks.

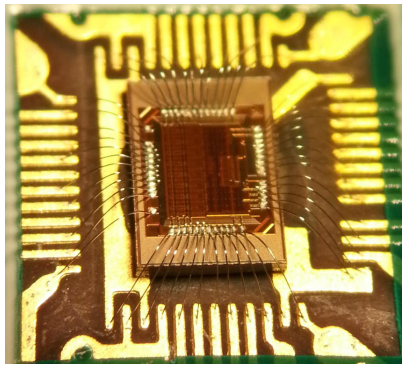
Conclusion:

It is right time now to think about FINAL ASICs and NEW Detector Module, which would allow us to build COMPACT BeamCal/LumiCal prototype

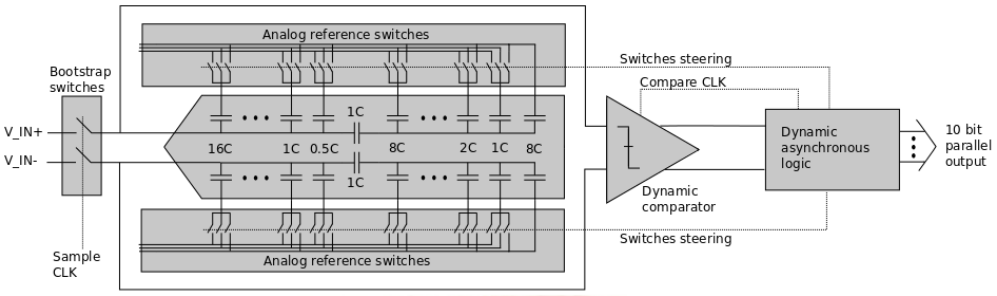
Ongoing works
Prototype ASICs designed in IBM 130 nm CMOS

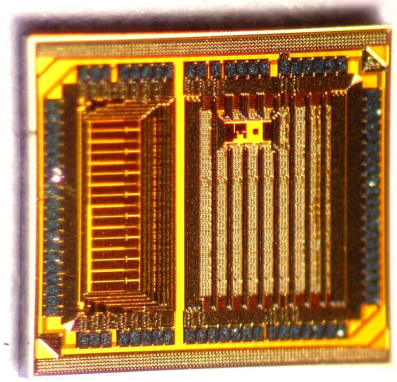
Preamplifier&Shaper





10-bit SAR ADC





- First prototypes of analog front-end (Preamplifier&Shaper) and 10-bit SAR ADC were developed in IBM 130 nm CMOS. Measurement results show that prototypes work well, although some improvements could be still done.
- In principle we were ready to start the design of multichannel ASICs for LumiCal readout, but...

Ongoing works and future
Moving from IBM to TSMC technology...

- The main reason of choosing IBM 130 nm CMOS was the fact it was considered by CERN the mainstream technology for future detector readouts
  - Being smaller institution, it is always good to follow the big ones, in order to have better support, possibility of collaboration etc....
  - So we started at AGH-UST with IBM 130 nm
- Unfortunately (maybe fortunately ?), due to some turbulances, things have changed and TSMC 130 nm is taking the pole position
  - A contract was signed between TSMC and CERN (and other groups designing for HEP applications), in order to fascilitate HEP groups collaboration and design sharing. AGH-UST signed it too.
- We have already started first designs in TSMC 130 nm (not yet for LumiCal but for LHCb related project). We would like to submit LumiCal ASICs sometime in 2015...
- For TSMC 130 nm we want to use much more aggressive schedule. Already in first submission we would like to send multichannel front-end and ADC ASICs ready for integration on COMPACT LumiCal module. Of course, in case of failure, at least one more submission would be needed...

Summary and Plans

- The old (AMS0.35um) ASIC phase has been completed.
  - Data taken with old readout still need to be analyzed. Eventually, one more test-beam with existing readout may be done.
- We have started the design in new (hopefully FINAL) CMOS 130 nm process. After first prototyping stage in IBM 130 nm we are moving now to TSMC 130 nm.
  - a positive result of this decision is the fact that for Angel it should be much simpler to get access to TSMC than to IBM. Maybe there is a chance to converge to the same technology for BemCal&LumiCal...
- We hope to submit in 2015 the multichannel readout ASICs in TSMC 130 nm. This time we would like to proceed in "large jumps" and to get ASICs ready for LumiCal readout in One(or Two) submission(s)
- I was not taking about money, but ASICs need money... (submissions are expensive), success of AIDA2020 application would be very helpful.

Thank you for attention