SRS+Timepix readout

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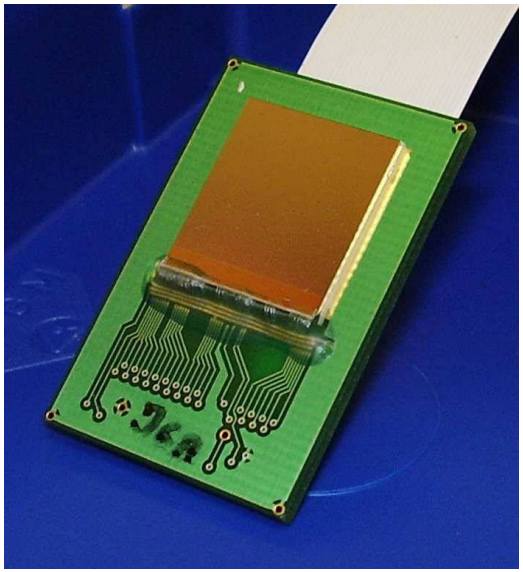
Outline

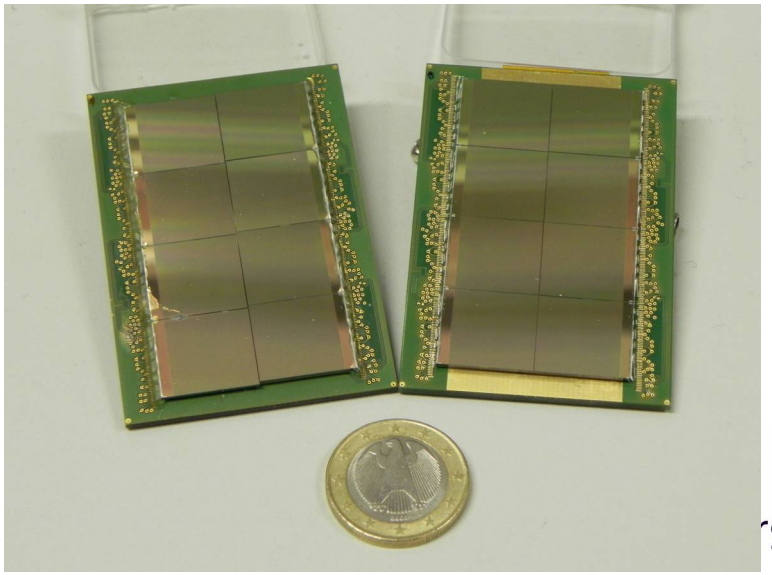
- Timepix Chip
- Small system
- Medium system
- What to do with it
- FEC6 experience

Timepix chip

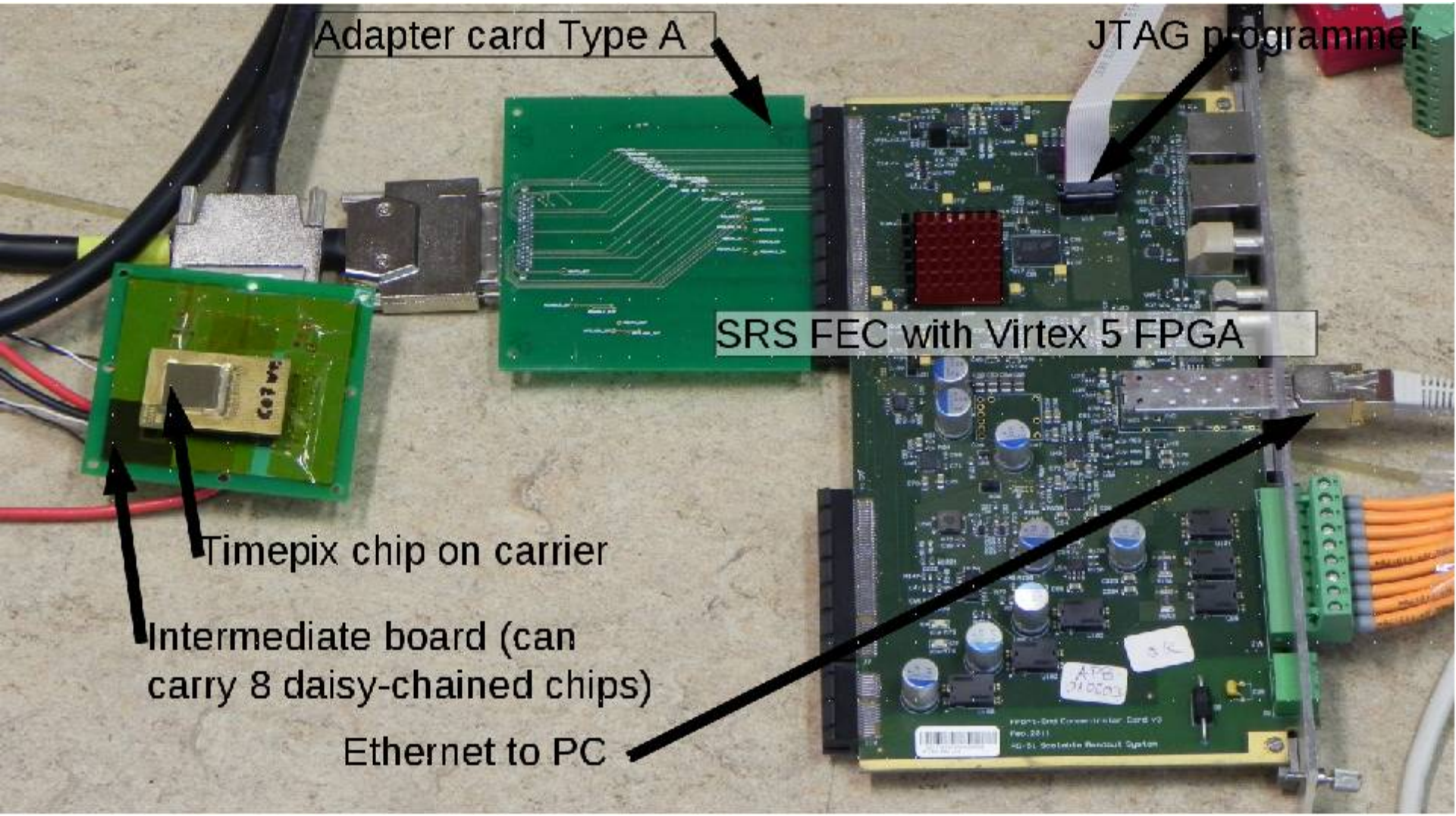
Properties:

- active surface: 1.4 x 1.4 cm²
- pixel size 55 x 55 µm²
- 256 x 256 pixel array
- 14 bit counter in each pixel (ToA or ToT)
- Noise threshold ~500e^- (ENC ≈ 90e^-)



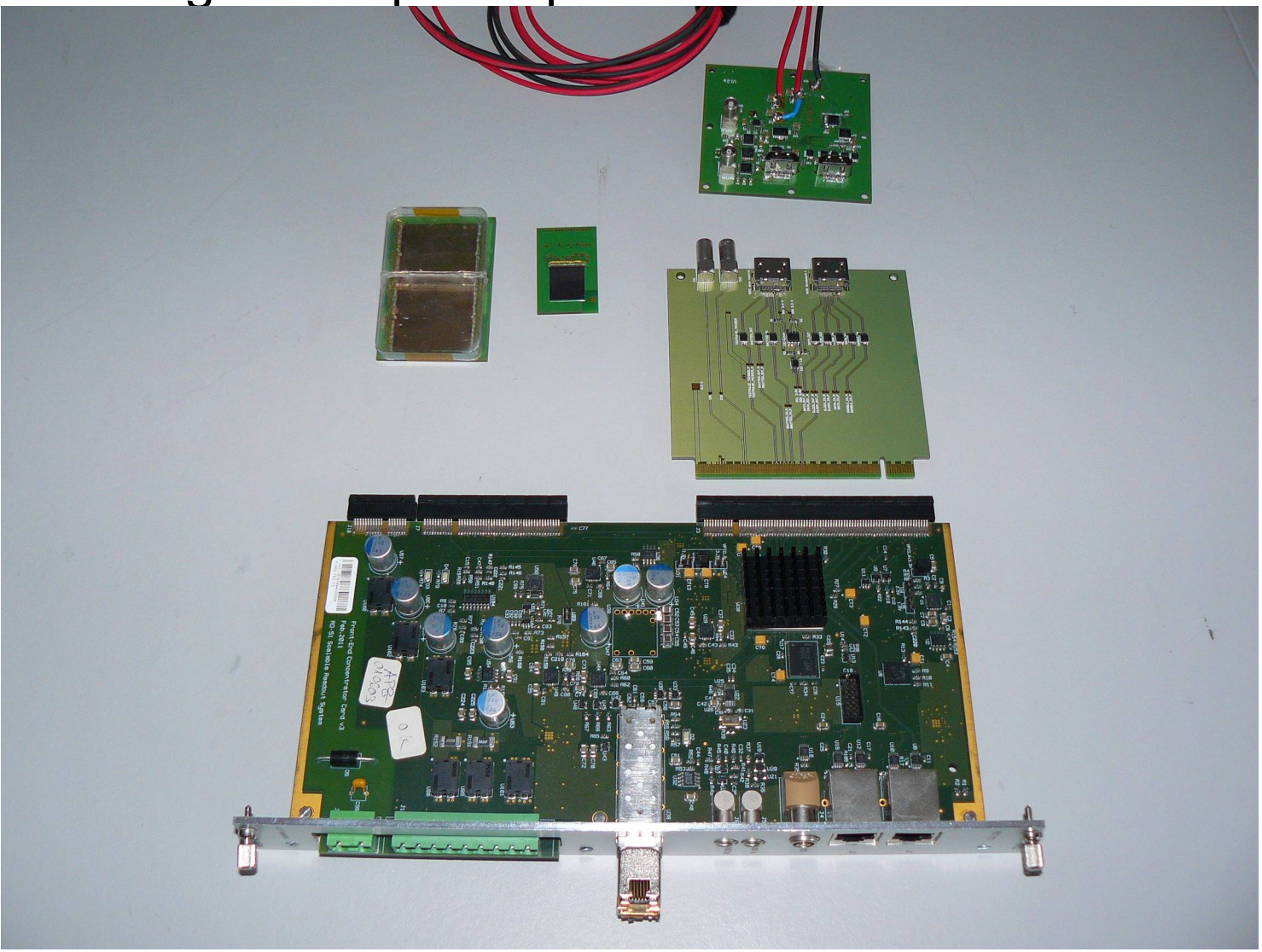


SRS+Timepix: chain



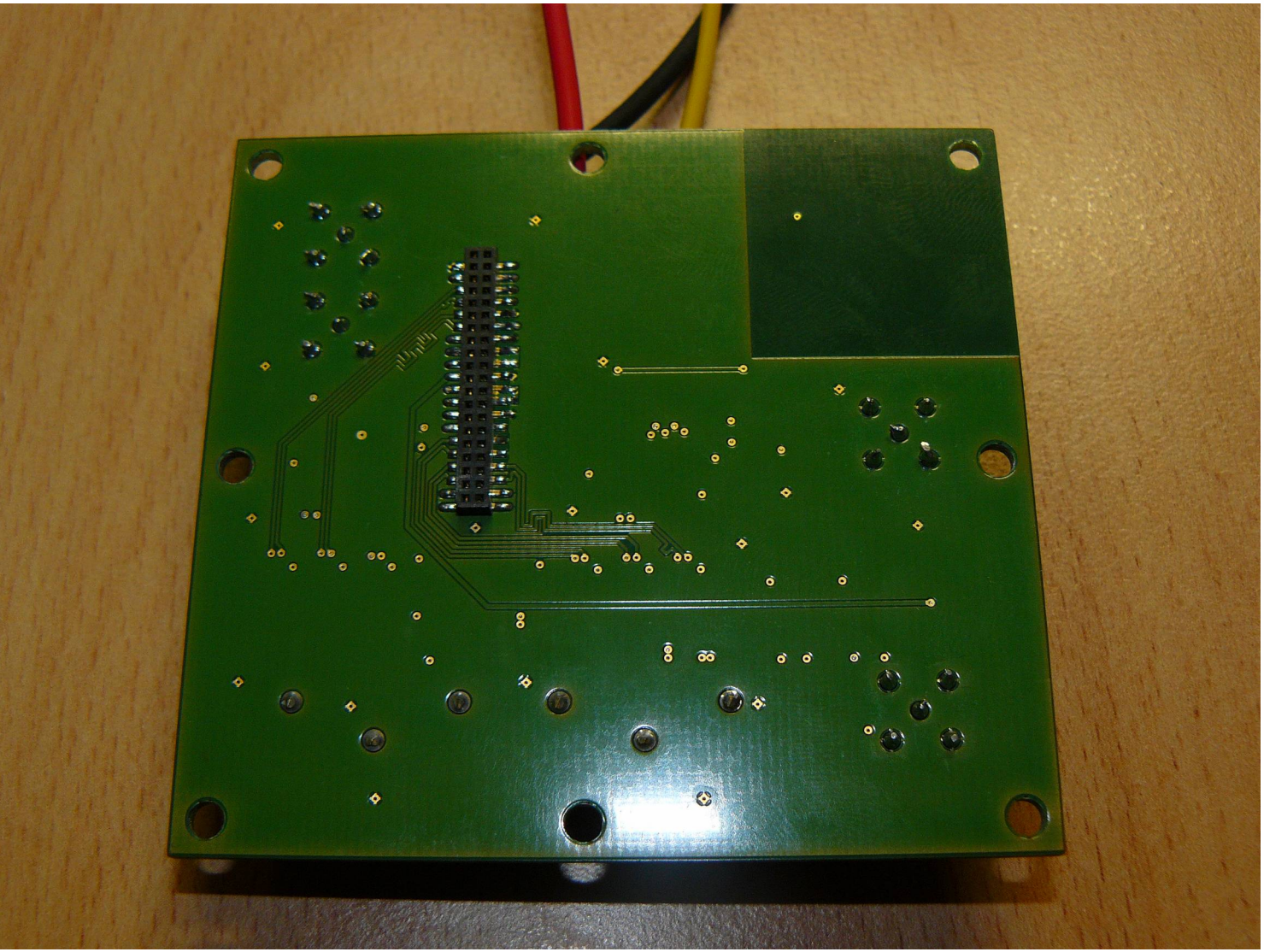
Small system

Single Timepix chip or octoboard



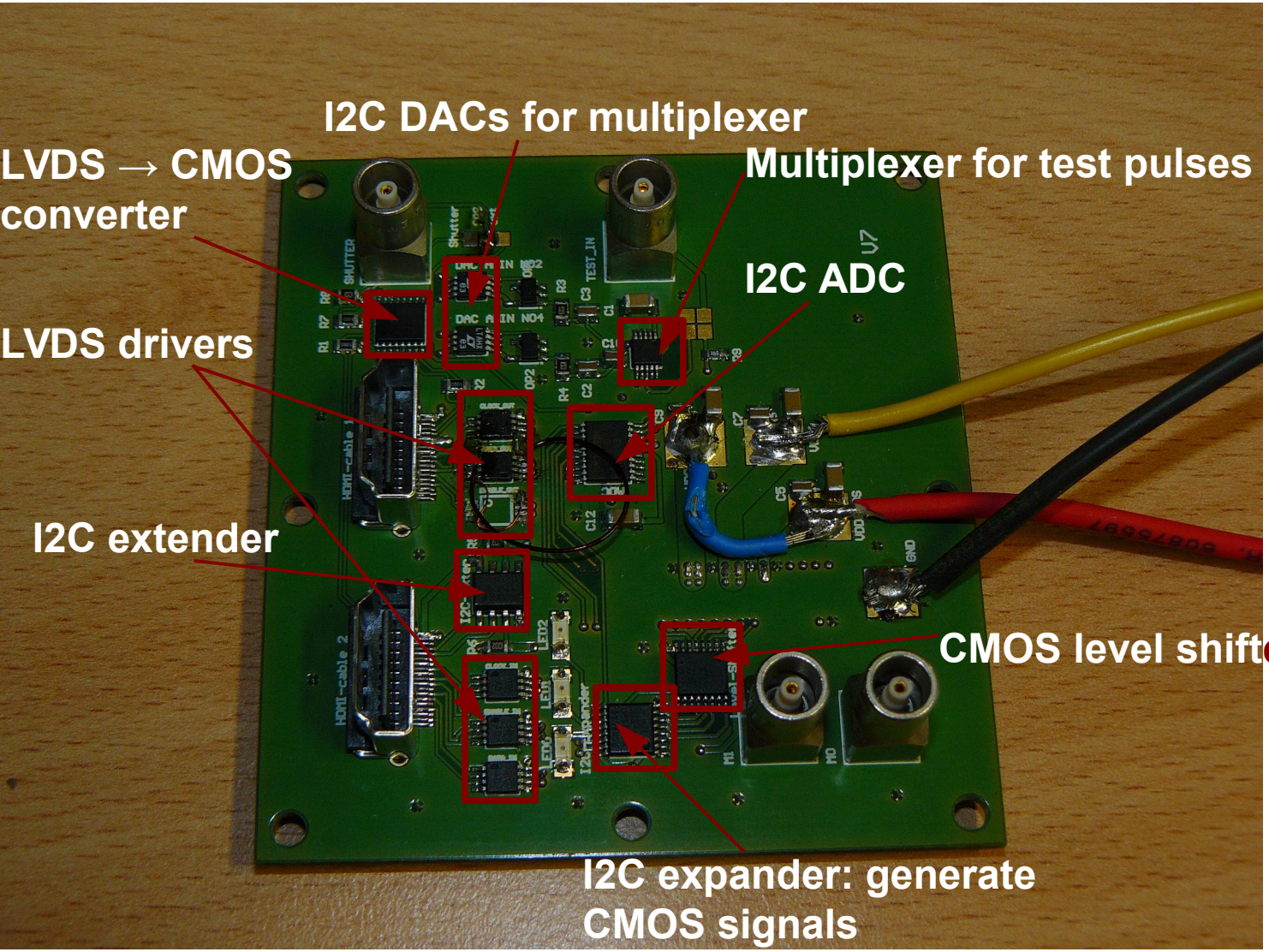
Small system

Intermediate board with HDMI connectors



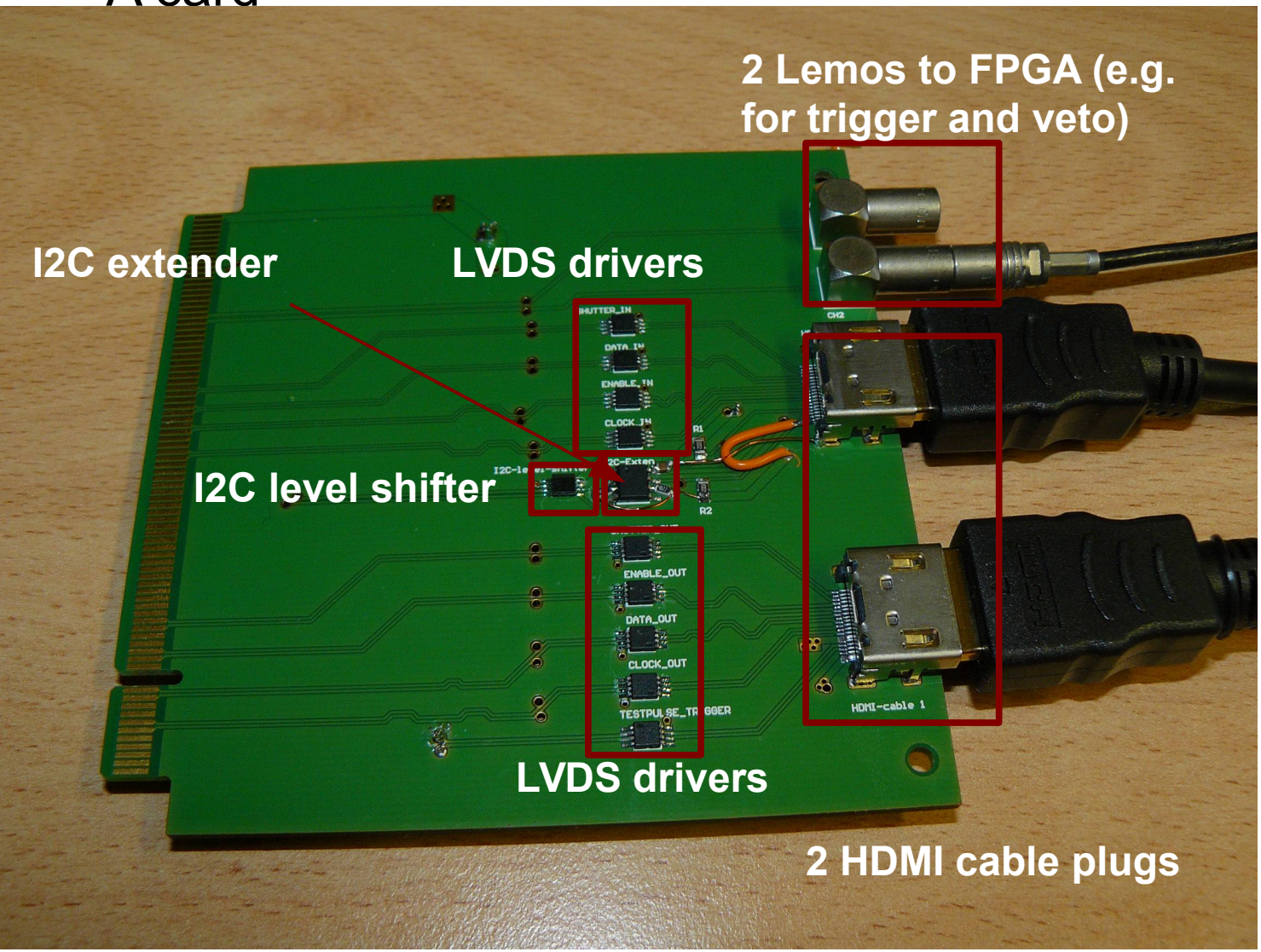
Small system

Intermediate board with HDMI connectors

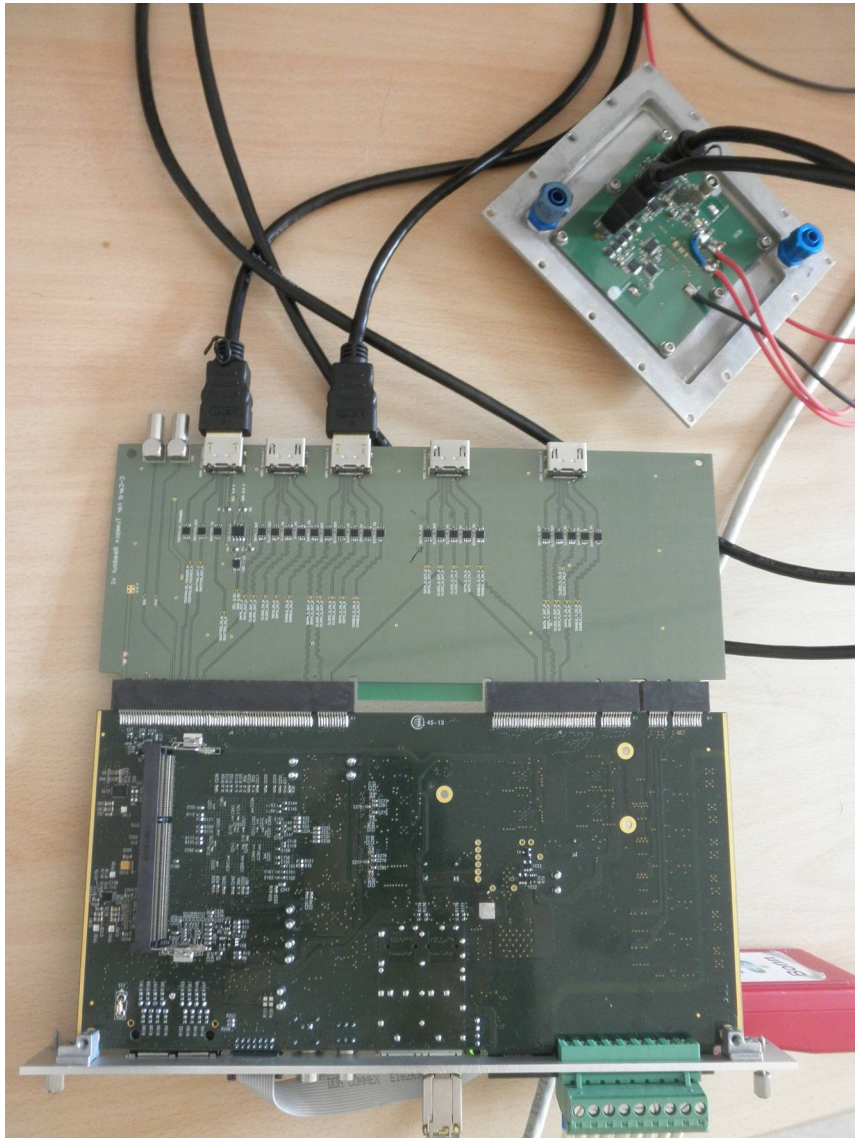


Small system

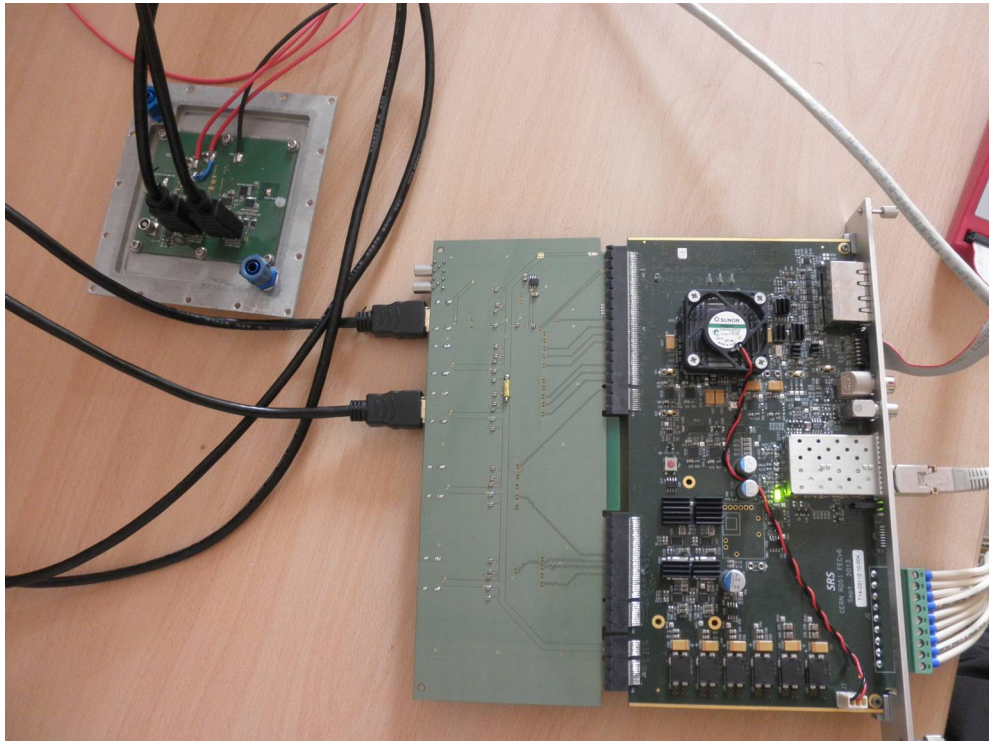
A card



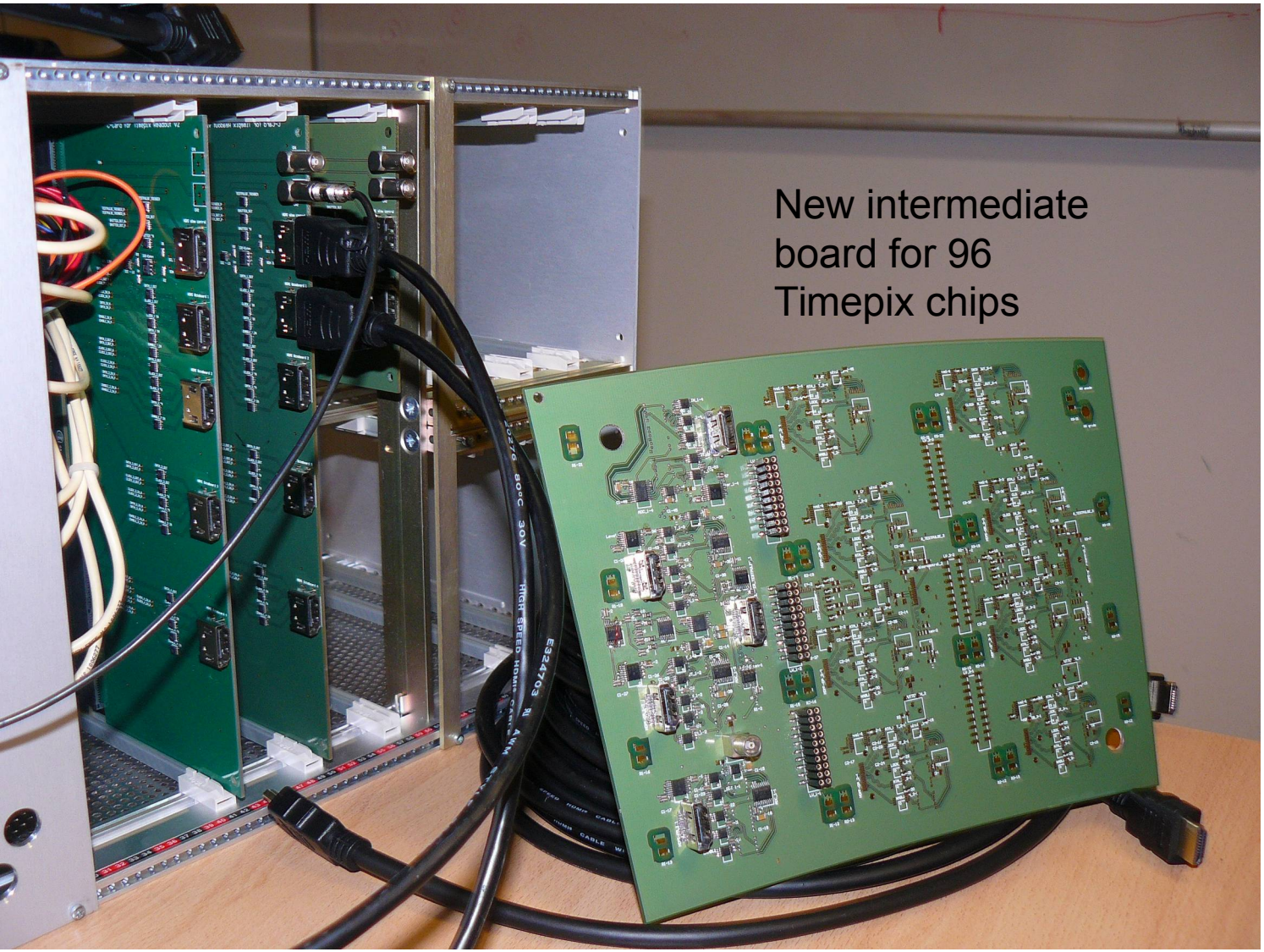
Medium system



C Card on FEC6



Medium system



3 FEC6 with C-Cards

Each FEC/C-Card:
5 HDMI plugs:
1 for slow control
1 per octoboard

=> 4 octoboards/ FEC

Up to 15m HDMI

Medium system

3 FEC6 with C-Cards

Each FEC/C-Card:
5 HDMI plugs:
1 for slow control
1 per octoboard

=> 4 octoboards/ FEC

New intermediate board for 96 Timepix chips

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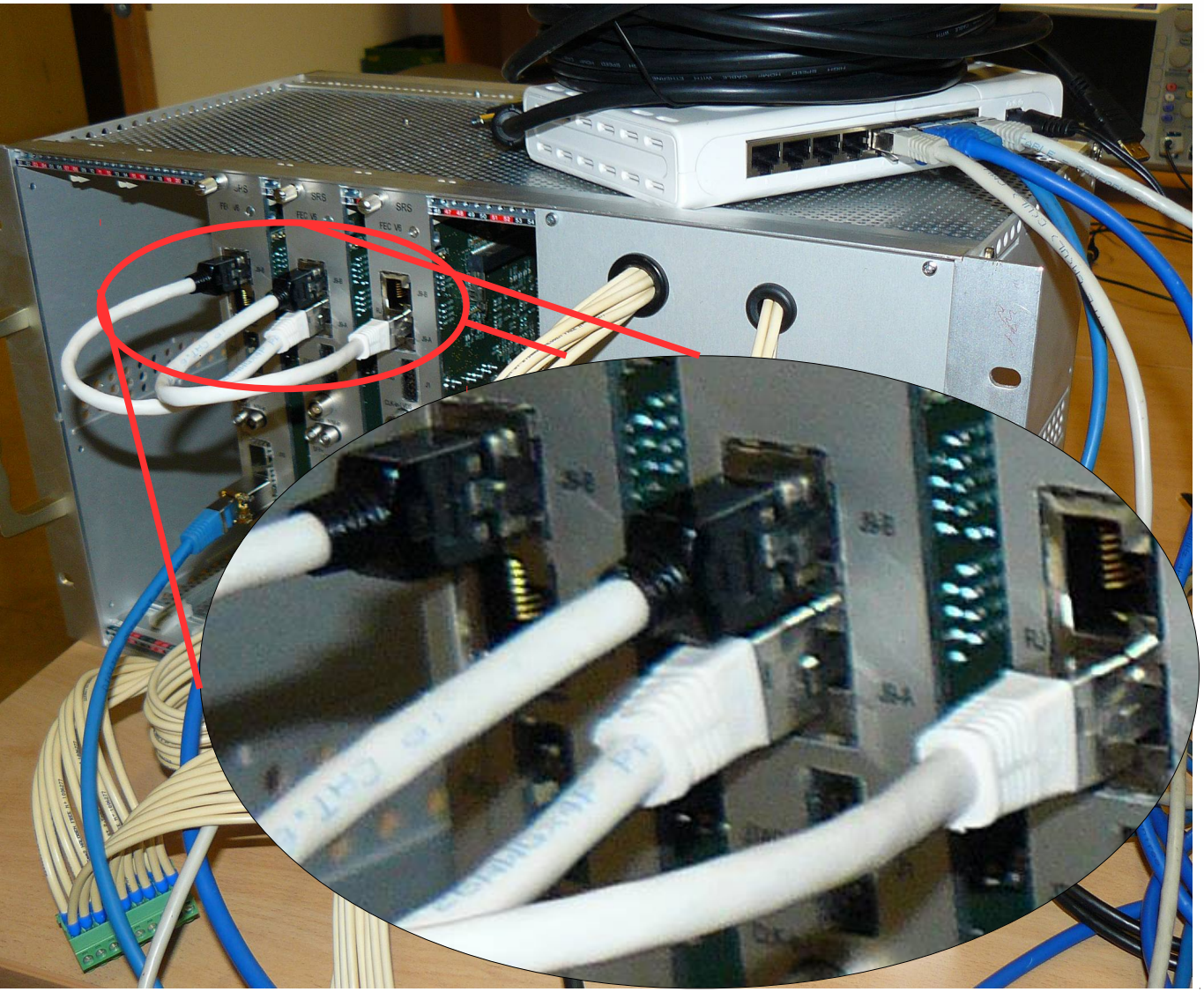
Medium system



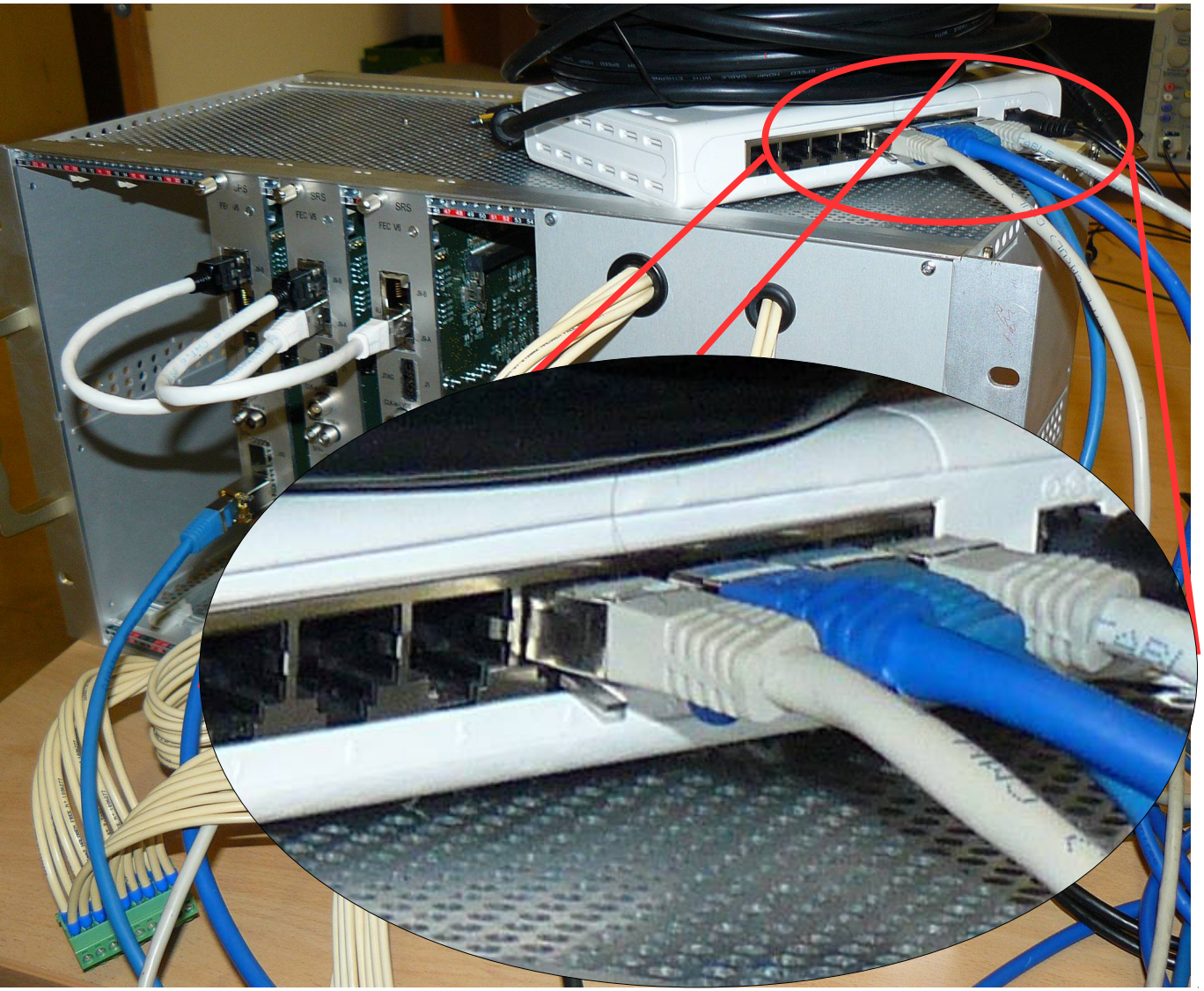
Clock synchronisation
using DTC link

Master FEC:
clk200 from oscillator
Clk40 and clk 200 out

Slave FECs:
Clk200 from Master
Clk40 from clk200
Synchronise clk40
With clk40 from master

Trigger:
From NIM_in or DTC
Slave → Master

Medium system



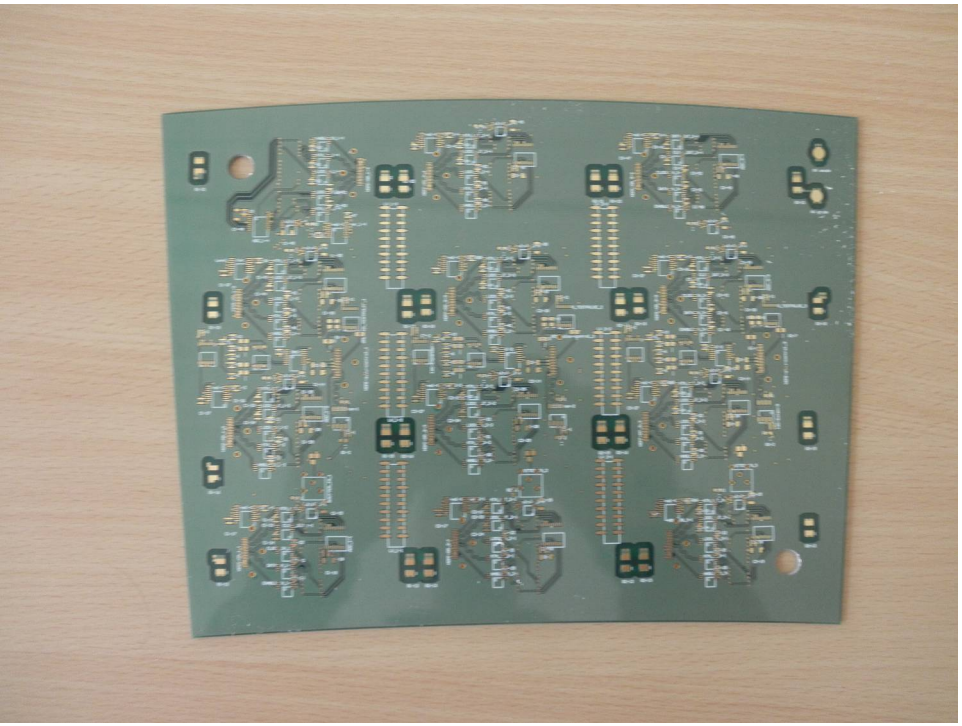
Gigabit Ethernet switch

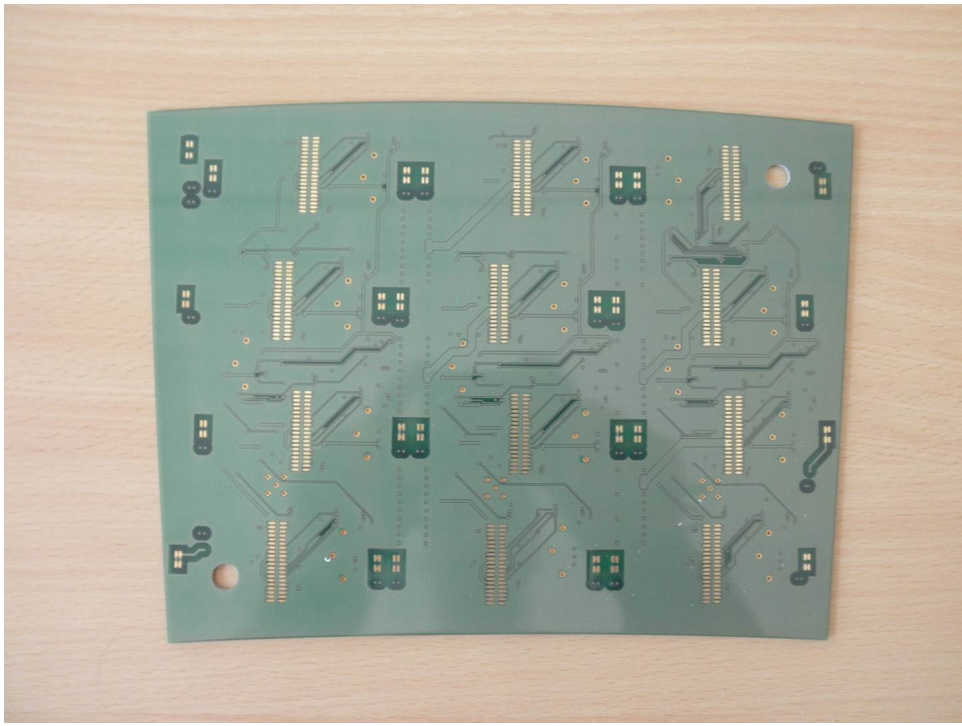
Software communicates with FECs by IP/MAC address

SFP used at each FEC

Medium system

Intermediate board for LCTPC module (96 chips on 12 octoboards) read out by 3 FECs





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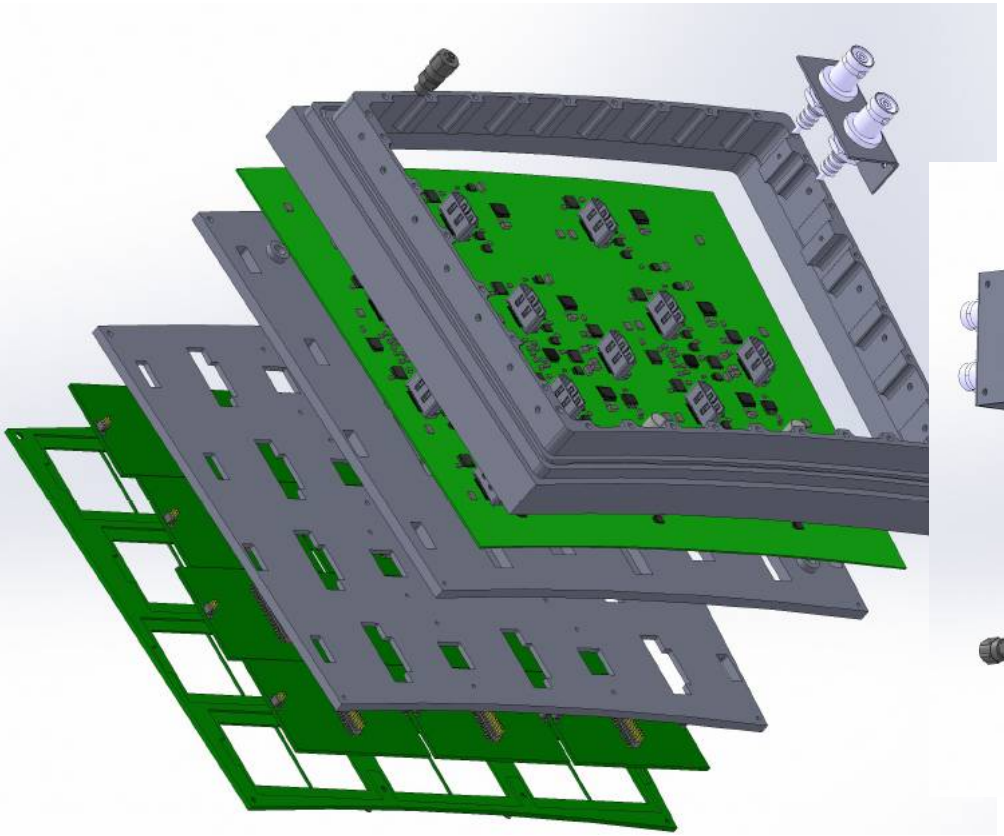
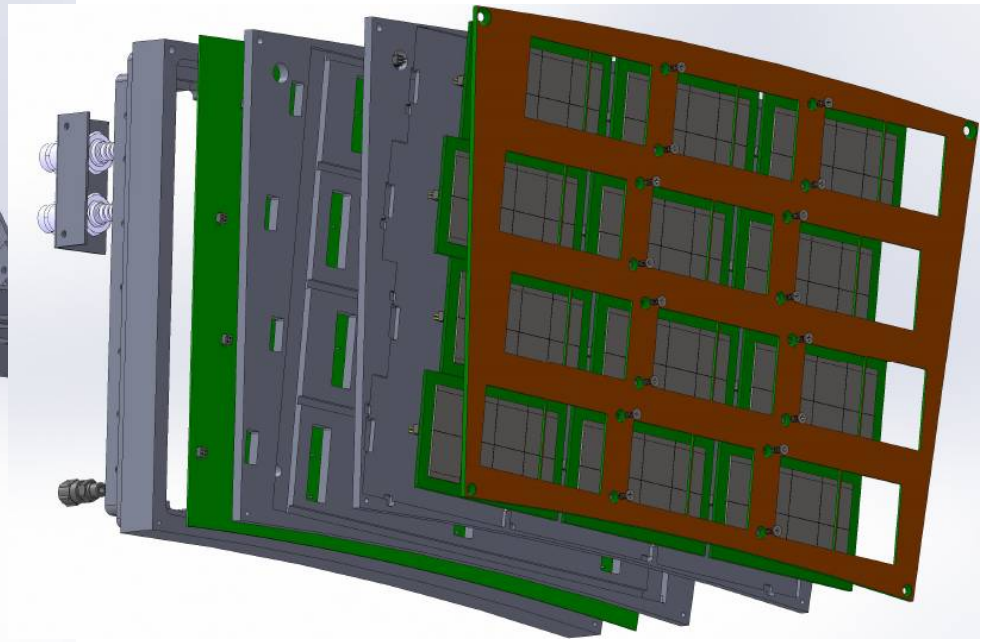
LCTPC Module





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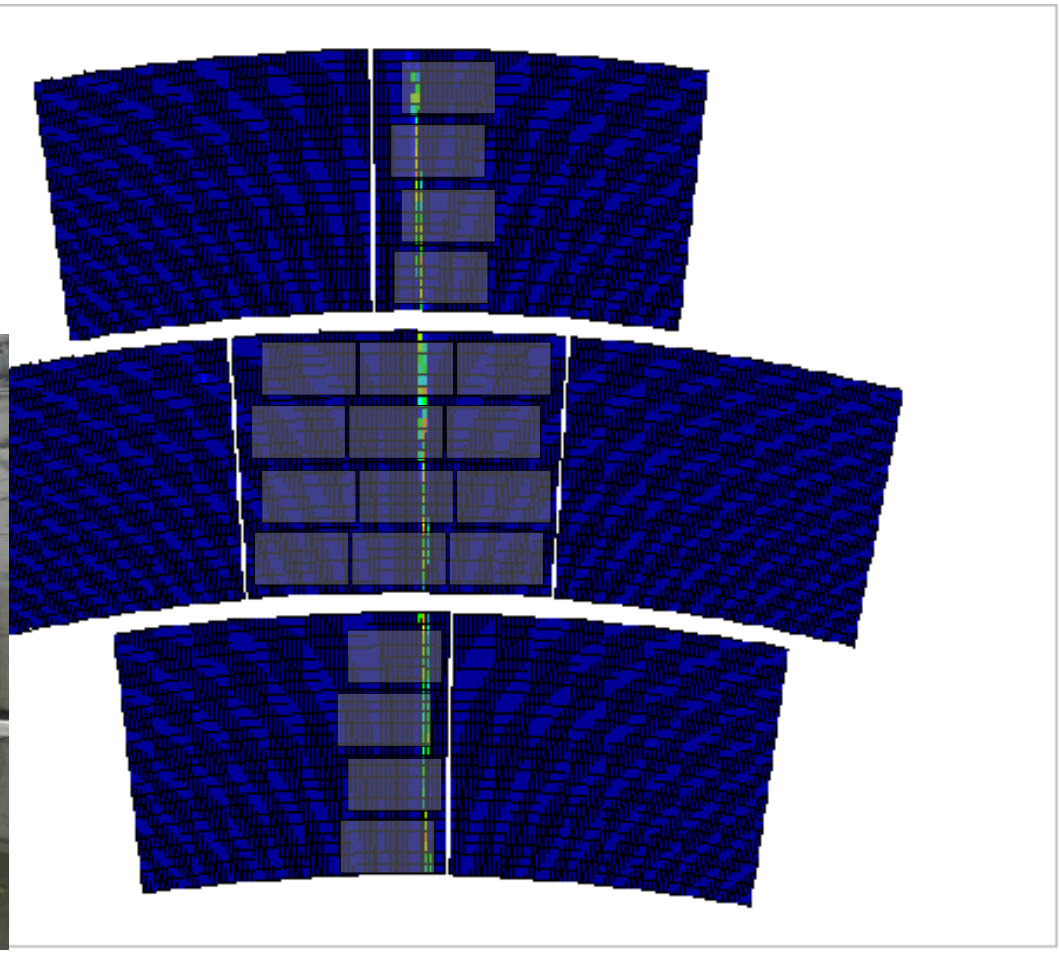
Testbeam 2015

- DESY: LCTPC Prototype: TPC for up to seven modules
  - 1 fully and two partly equipped with Timepix chips
  - 160 chips
  - 5 FECs
  - Need to borrow
    2 FEC6



Readout system

SRS C-Card + FEC6 in operation

- 1 design error found (powering of LVDS drivers) due to difference between FEC5 and FEC6
- 1 LVDS driver defect
- Development of firmware almost finished
  - Test with one octoboard of naked Timepix chips connected to any one of the four slots
  - Set DACs (FSR) in chip and read back chip ID √
  - Set matrix and read it back √
  - Zero suppressed readout √
  - Zero suppressed readout while sending data of last frame √
- Software: needs extension for several FECs multithreaded
  - Several FECs serail

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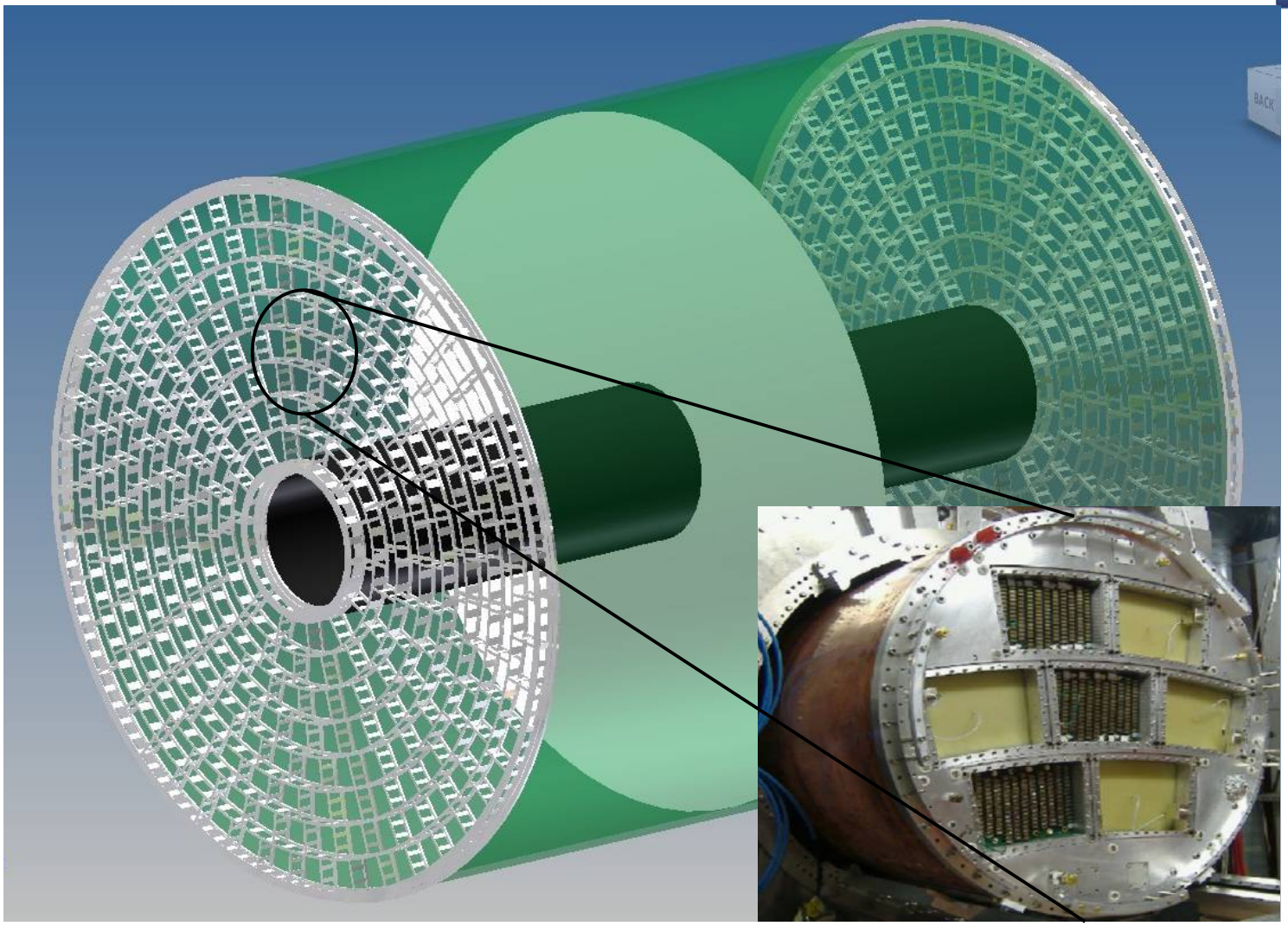
Large system



ILD TPC with pixel readout

FEC 6 experiences

- Problems with powering at beginning
  → Confusion with production and 0 Ω resistors
- Problems with Spansion memory
  → Confusion with memory size
- Problems with Jitter cleaner
  → not used after discussion with Raul
- NIM_out signal looks strange?
  → maybe change resistor in NIM_out network?
- Cooling seems to be sufficient
- FEC5/FEC6 compatibility: difficult for clock_in signals at PCI plug, VPIO3_3 not available any more

FEC6 works excellent!

Summary

Implementation of Timepix in SRS almost finished

- Small system verified at Testbeam 2013

- Medium size system
  - Firmware almost finished
  - Hardware ready
  - Detector in preparation
  - Testbeam in spring 2015