SDHCAL

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OUTLINE

- RPC-based calorimeters for leptons collider
- SDHCAL concept
- SDHCAL-GRPC prototype
- Prototype results
- Present and future development
- Conclusion

Motivations

For future colliders, jet energy resolution will be a determinant factor of understanding high energy physics.

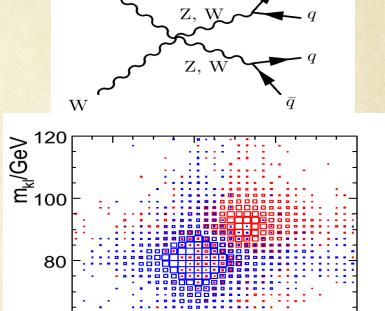
Exemples:

- → Trilinear Higgs self coupling measurement
- → WW scattering measurement

$$\frac{\sigma_E}{E} = \frac{21}{\sqrt{E}} \oplus 0.7 \oplus 0.004E \oplus 2.1 \left(\frac{E}{100}\right)^{+0.3} \%$$
Resolution Tracking Leakage Confusion

To improve on the jet energy resolution **PFA** is a promising solution to reduce the confusion term.

But PFA needs high granularity Calorimeters



80

100

m_{ii}/GeV

120

Different solutions of such calorimeters are being followed within the CALICE international collaboration. The option we are investigating is the Digital and Semi-Digital Hadronic CALorimeter using GRPC as sensitive medium

60

60

DHCAL:

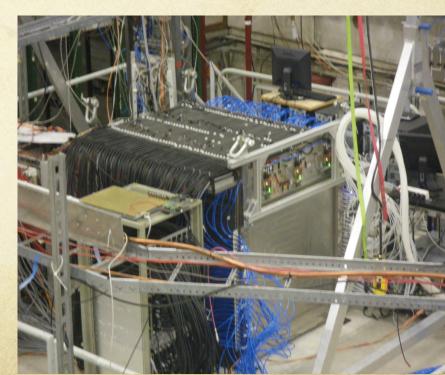
First prototype with embeded electronics

(> 480k ch) by Amercian groups



SDHCAL:

First technological prototype addressing technical problems for future lepton colliders (namely ILC)



SDHCAL concept

1- Detector choice

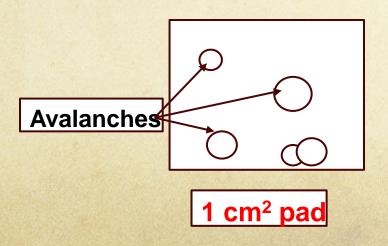
Gaseous detectors: homogenous, cost-effective and highly transverse and longitudinal granular.

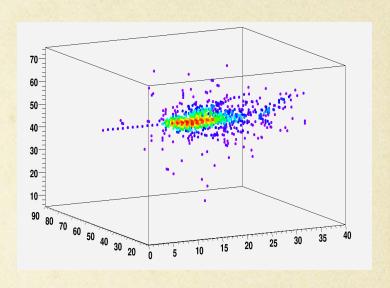
GRPC: is an adequate candidate for ILC and CEPC.

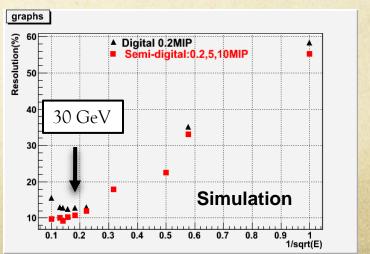
2- Electronics readout choice

At high energy the shower core is very dense

- → Simple binary readout will suffer saturation effect
- → Semi-digital readout (2-bit) can improve the energy resolution.







SDHCAL for ILD

The SDHCAL-GRPC is one of the two HCAL options proposed in the **ILD** Letter **O**f **I**ntention (LOI). Modules are made of 48 RPC chambers $(6\lambda_I)$ equipped with power-pulsing electronics readout.

The structure proposed for the SDHCAL-ILD:

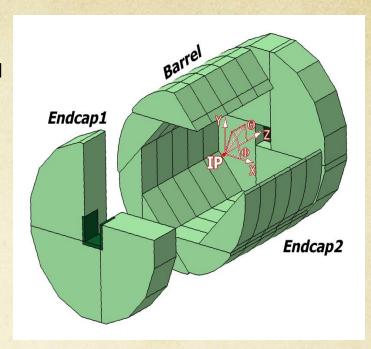
- Is self-supporting
- Has negligible dead zones
- Eliminates projective cracks
- Minimizes barrel / endcap separation (services leaving from the outer radius)

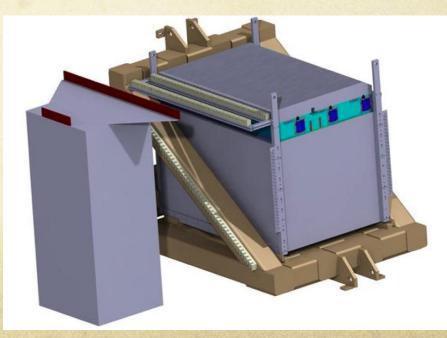
SDHCAL Prototype

- Come as close as possible to the ILD module and be able to study hadronic showers
- -48 units (active layer + absorber) fulfilling the ILD requirements.

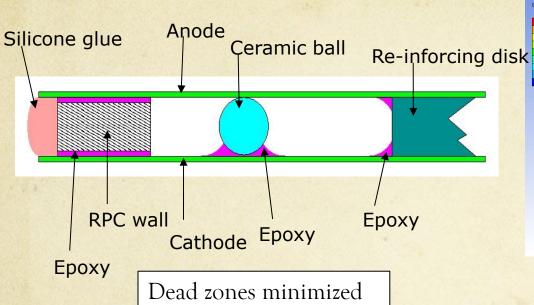
Challenges

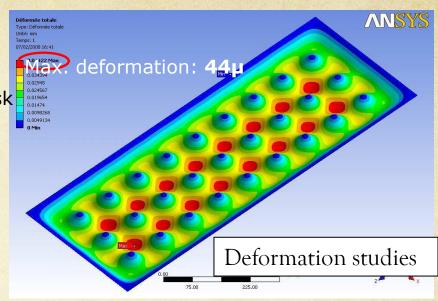
- -Homogeneity for large surfaces
- -Thickness of only few mms
- -Services from one side
- -Embedded power-cycled electronics
- -Self-supporting mechanical structure



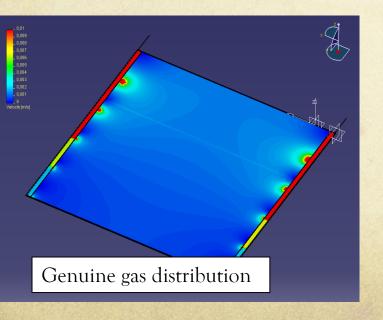


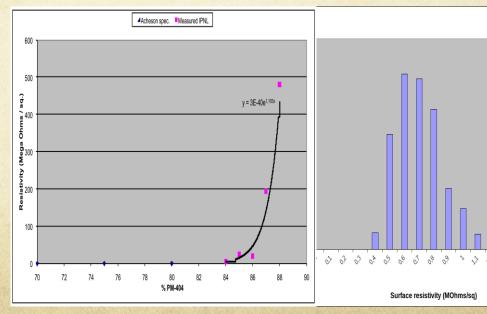
GRPC development





New resistive painting was developed





Electronics readout development

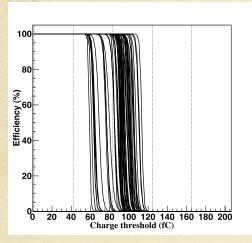
ASIC: HARDROC

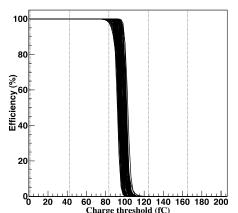
64 channels, trigger less mode, memory depth:

127 events

2-bit readout : 3 thresholds
Dynamic range: 10 fC-15 pC
Gain correction → uniformity

Power-pulsed → reduced power consumption

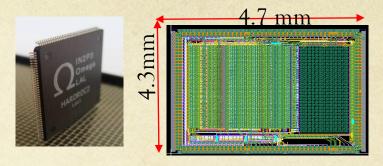


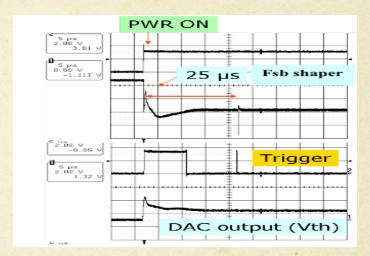


Printed Circuit Boards (PCB) were designed to reduce the x-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two (the 24X2 ASIC are daisy-chained).

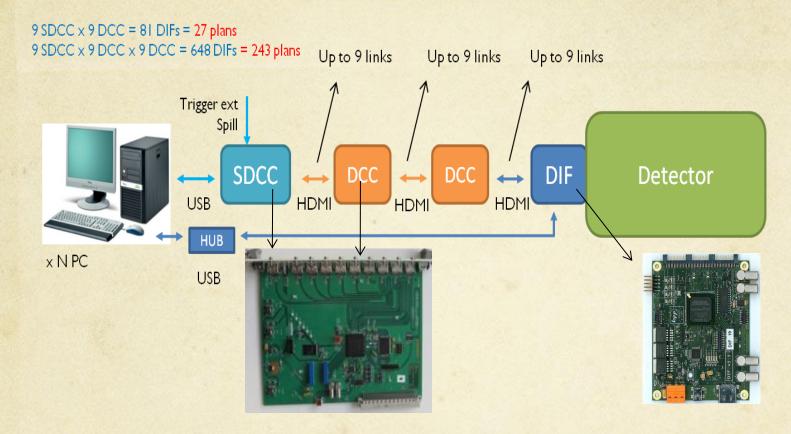
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.







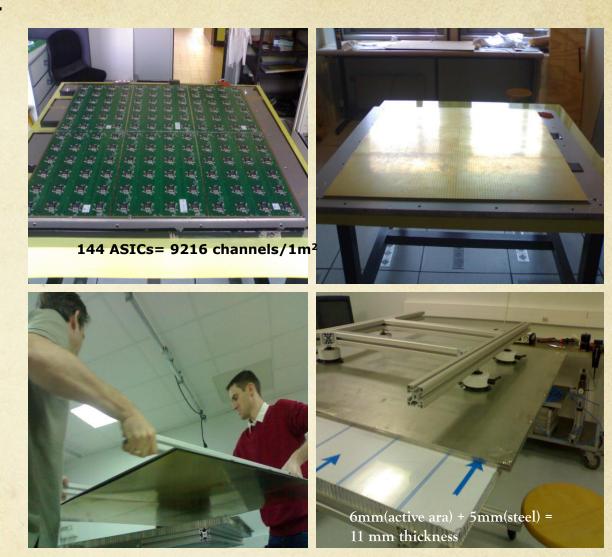
SDHCAL acquisition system



- → Acquisition software was developed to deal with the output of large number of electronics channels (> 460 000).
- → Oracle database used for ASIC configurations and slow control.
- → CMS Xdaq used to provide the DAQ framework.

Cassette development

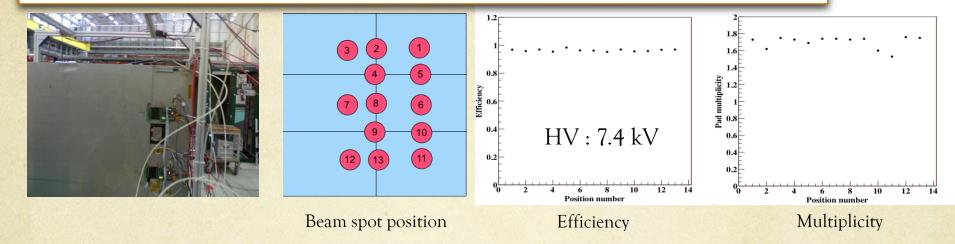
- → To provide a robust structure.
- → To maintain good contact between the readout electronics and the GRPC.
- \rightarrow To be part of the absorber.
- → It allows to replace detectors and electronics boards easily.



The cassettes are built of no-magnetic stainless steel walls 2.5 mm thick each → Total cassette thickness = 6mm (active layer)+5 mm (steel) = 11 mm

Test Beam validation

The homogeneity of the detector and its readout electronics were studied



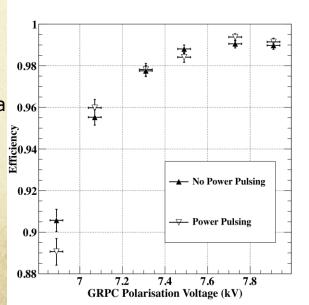
Power-Pulsing mode was tested in a magnetic field of 3 Tesla



The Power-Pulsing mode was applied on a GRPC in a 3 Tesla 0.96 field at H2-CERN

(2 ms every 10 ms)

No effect on the detector performance

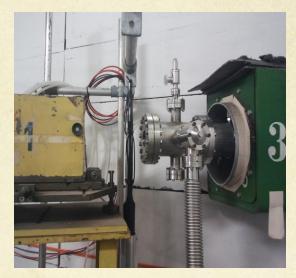


High-Rate GRPC

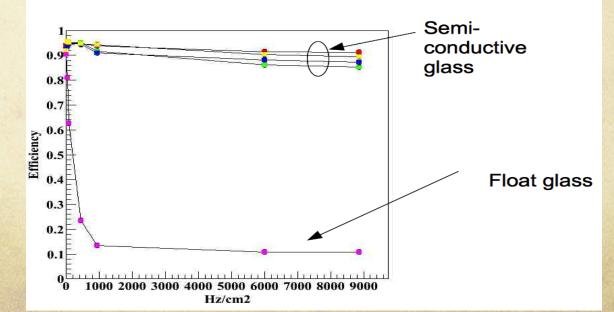
High-Rate GRPC may be needed in the very forward region

✓ Semi-conductive glass (10¹0 Ω.cm) produced by our collaborators from Tsinghua University was used to build few chambers. ✓ 4 chambers were tested at DESY as well as standard GRPC (float glass)

Performance is found to be excellent at high rate for GRPCs with the semiconductive glass and can be used in the very forward of ILD region if the rate exceeds 100 Hz/cm² in future ILD upgrades







SDHCAL prototype construction

- √ 10500 ASIC were tested and calibrated using a dedicated robot that was used by CMS (IPNL, OMEGA) (ASICs layout: 93%).
- √ 310 PCBs were produced, cabled and tested (IPNL).

 They were assembled by sets of six to make 1m²

 ASUs

 ASUs
- √ 170 DIF(LAPP), 20 DCC(LLR) were built and tested.
- √ 50 detectors were built and assembled with their electronics into cassettes. Cassettes were tested by sets of 6 using a cosmic test bench (IPNL).
- ✓ The mechanical structure was built in CIEMAT.
- ✓ HV, cooling services were built by UCL, Gent.
- ✓ Full assembly took place at CERN.



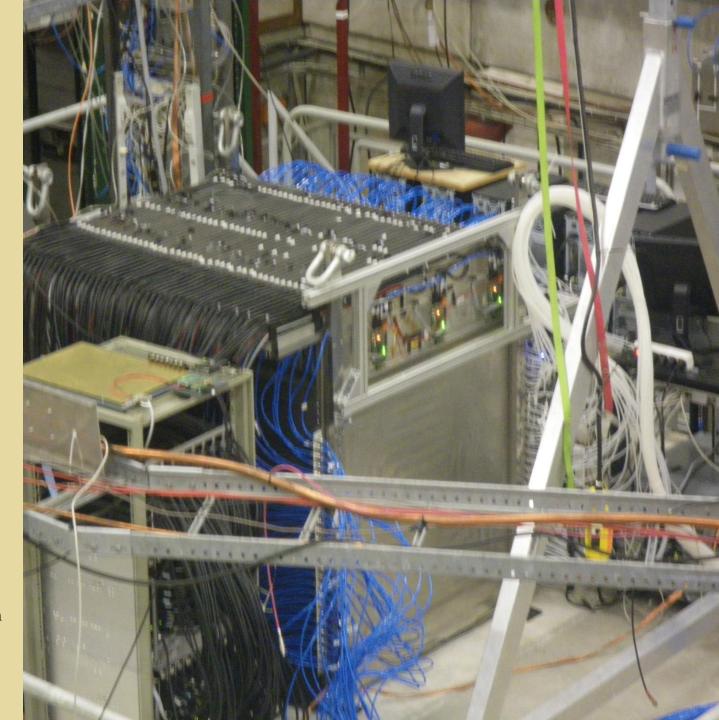


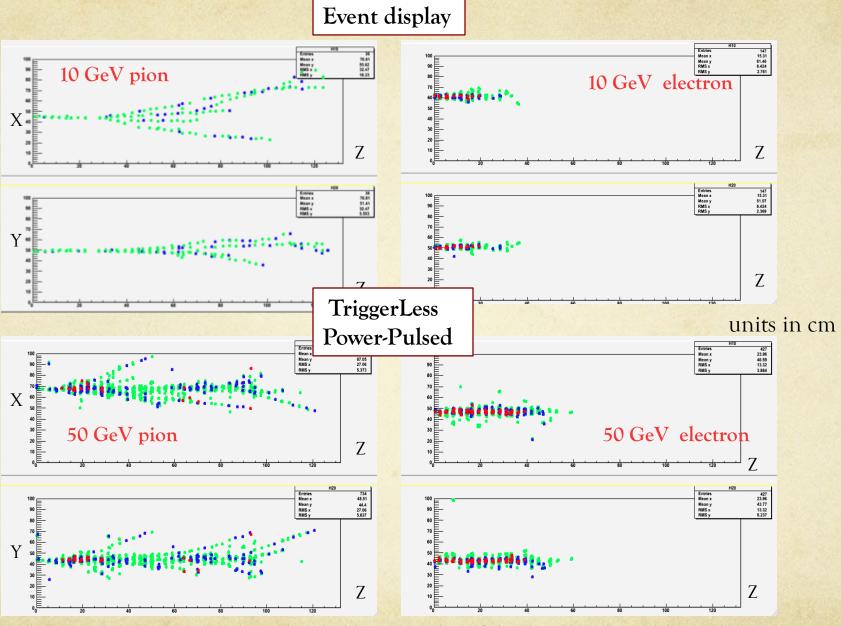


Prototype @TB

3 periods of TB in 2012 (5 weeks)

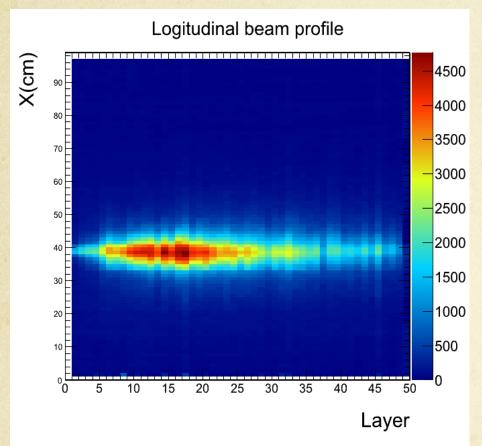
- → SDHCAL
 Commissioning with
 TrigerLess, Power-Pulsing
 modes;
- → Thresholds choice optimization;
- → Muons run calibration;
- → Pion, electron runs to study EM and hadronic showers;
- →No particle identification detector was used.

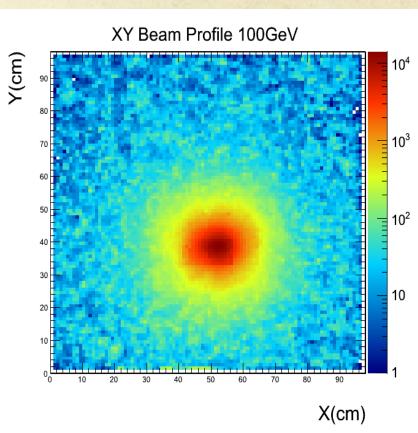




Colours correspond to the three thresholds: Green (100 fC), Blue (5 pC), Red (15 pC)

Raw data, no treatment except time hit clustering

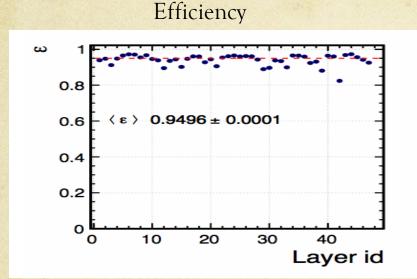




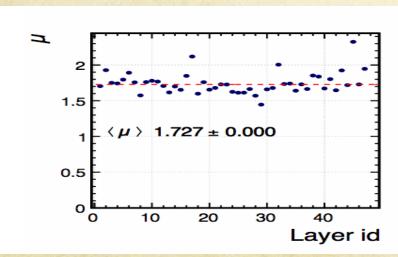
100 GeV pions

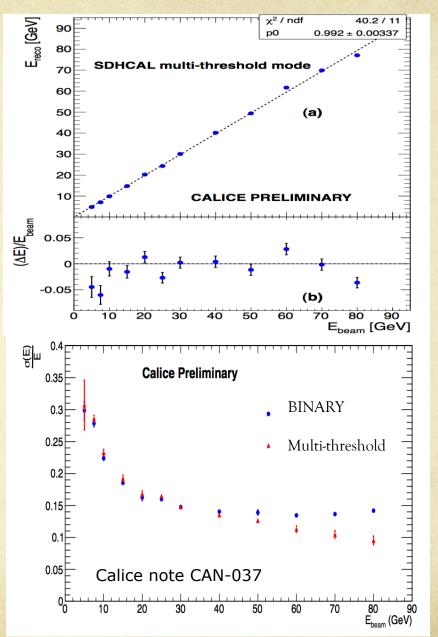
First results on linearity and energy resolution

with no calibration and with no gain correction.

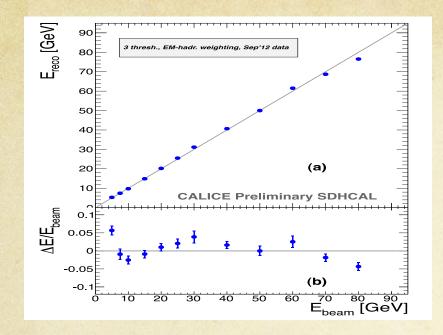


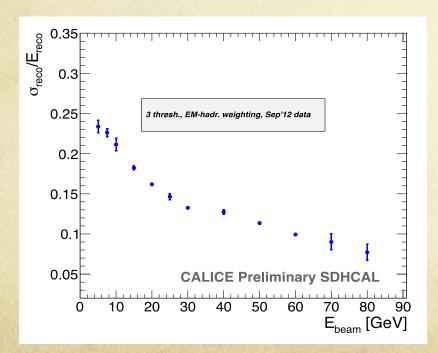
Pad multiplicity

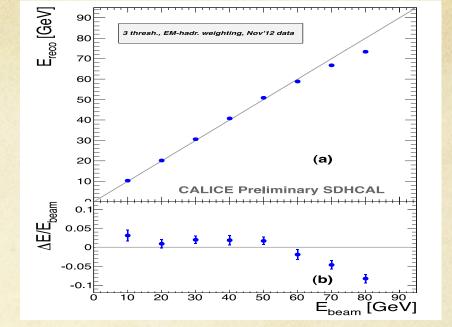


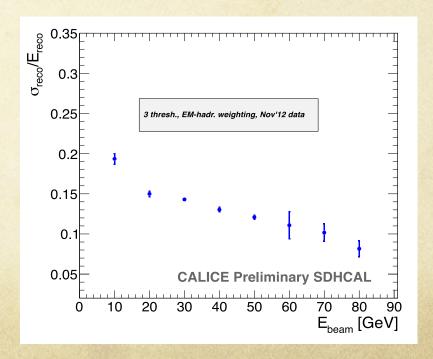


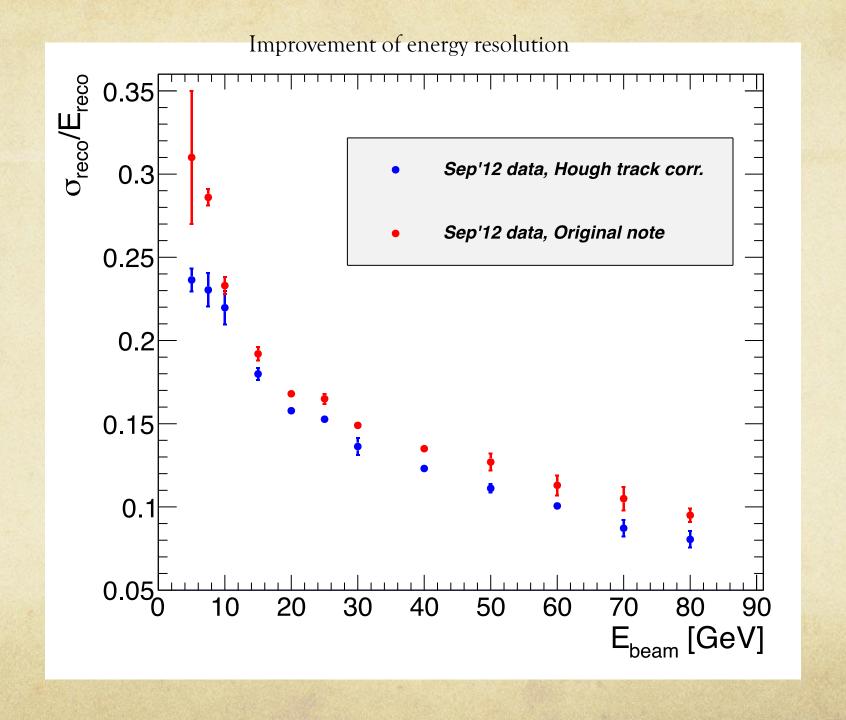
Semi-digital improvement with respect to digital version.







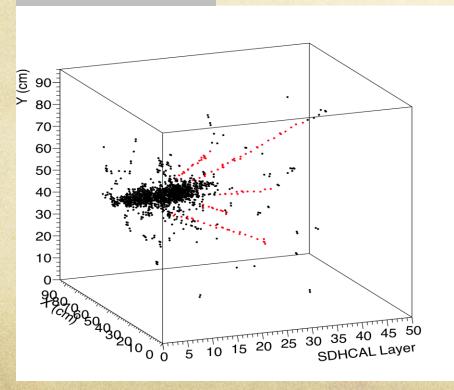


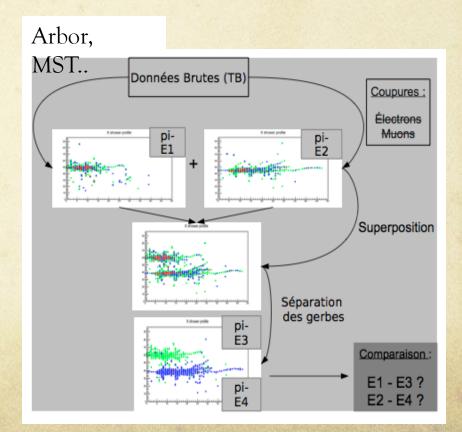


Ongoing analyses

- → Calibration study;
- →Electron-Pion separation;
- → Energy resolution improvement by taking into account hadronic shower structure and calibration correction: an improvement of 7-15% already achieved with respect to the preliminary ones obtained immediately after TB;
- → Imaging algorithm developments (HT, Arbor, MST) → PFA

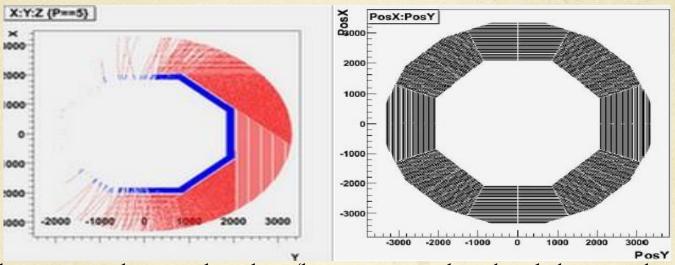
Hough Transform



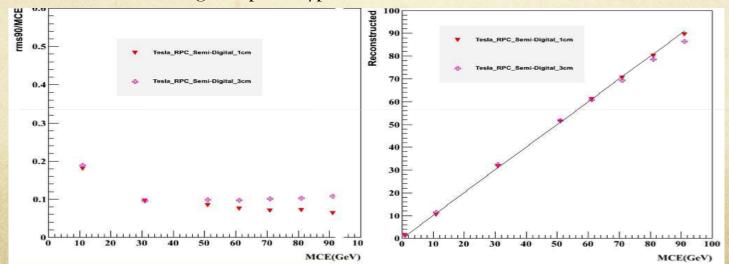


Simulation and optimization studies

SDHCAL was simulated with two mechanical structures for ILD (V and Tesla)



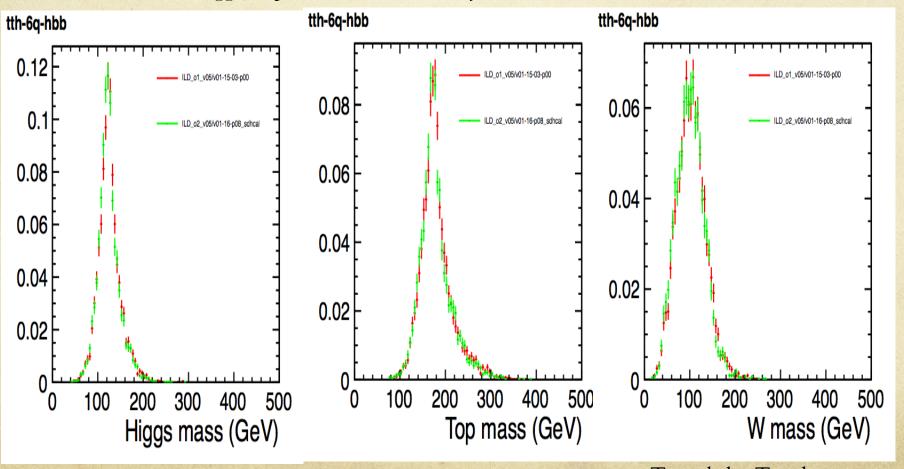
Studies on granularity and readout (binary vs semi-digital and also granularity of 1x1 cm² vs 3x3 cm²) were conducted. They allowed to confirm the SDHCAL choice before to start building the prototype



Simulation and optimization studies

The SDHCAL simulation was re-performed taking into account the constraints and the results of the prototype. The new version was used for the DBD studies, showing that same performance are obtained as for the AHCAL (albeit the PFA optimization was done for the AHCAL topology)

Higgs, top and W in the tth 8jet mode (1000 GeV).



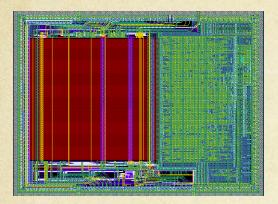
Tomohiko Tanabe

Road map in the 2-3 coming years

- -Improve on the energy reconstruction using new techniques;
- -Improve on simulation (digitizer) and compare hadronic shower models to data;
- -Develop PFA techniques to be used to separate close-by hadronic showers;
- -Complete TB (ECAL+SDHCAL+...);

- -Build few very large GRPC detectors (2-3 m2): gas circulation system, thickness...;
- -Test the new version of electronics (I2C, roll mode..);
- -Design a new ASU capable to read the large GRPC (up to 3 m²);
- -Develop a new DIF (low consumption, reduced size, new functionalities);
- -Build a small mechanical prototype to host the few large chambers and test it.

New version of the readout electronics



The new version brings improvements on the previous one:

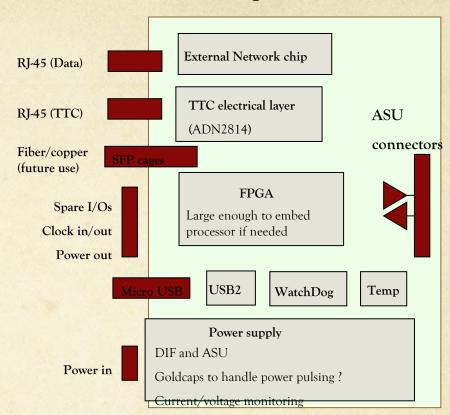
- →Independent channels and zero suppression
- →Independent ASICs (I2C)
- →Better dynamic range (up to 50 pC).
- → successfully tested;

 \rightarrow

This activity is funded essentially by **AIDA**

New ASU design for large detectors under study

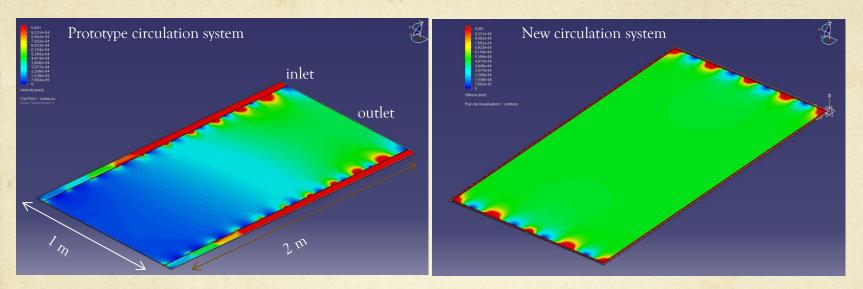
New features in the DAQ boards



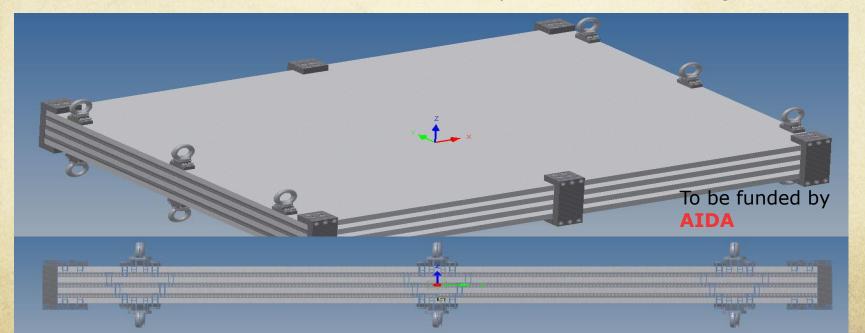
- → Only one DIF per plane. For the maximum length plane (1x3m) the DIF will handle 432 HR3 chips;
- → Slow control through the new HR3 I2C bus;
- → Data transmission to DAQ by Ethernet using commercial switches for concentration;
- → Clock and synchronization by TTC;

Synergy with R&D on fast links R&D of LHC (GBT) Funded essentially by CIEMAT

Detector improvement : to achieve same performances with very large GRPCs

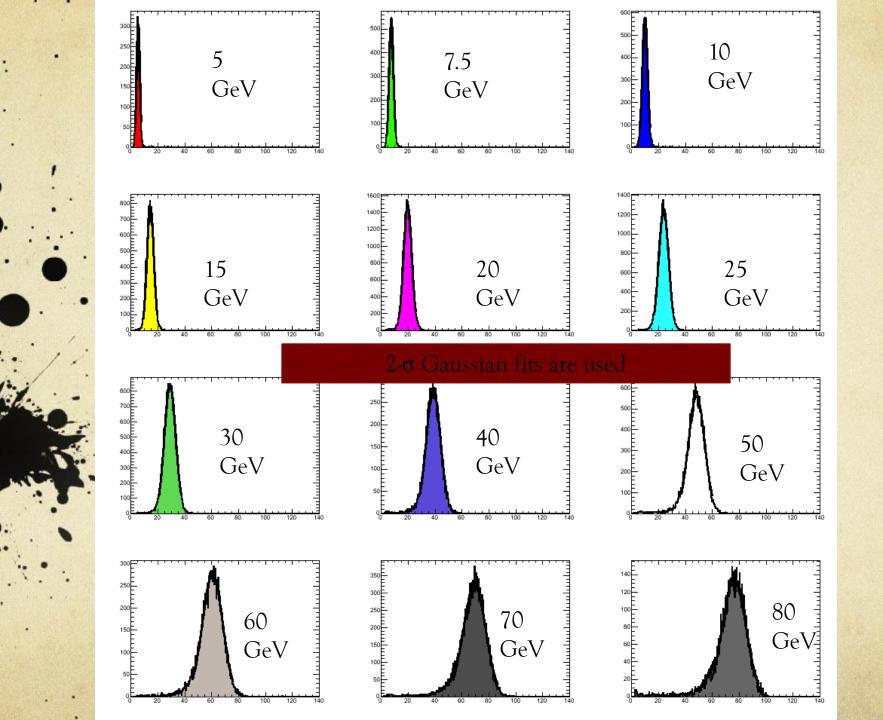


Mechanical structure: to be built with EBW techniques and to host few large detectors GRPCs



Conclusion and prospects

- -The SDHCAL prototype is the first and up-to-now unique **technological** calorimeter prototype. Its success proves that SDHCAL is an excellent option for ILD;
- -SDHCAL with its fine granularity is an excellent tool to develop and exploit PFA algorithms;
- -The expertise accumulated during the conception, construction and commissioning is very precious for physicists and technical staff in our labs;
- -The project has led to several spin-offs (TOMUVOL, CMS,..);
- Work on complete validation of the SDHCAL concept is ongoing.



Energy estimation:

The thresholds weight evolution with the total number of hits obtained by minimizing a χ^2

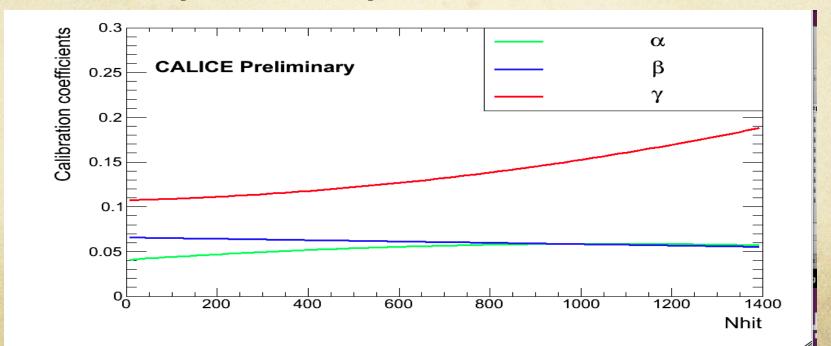
$$X^{2} = (E_{\text{beam}} - E_{\text{rec}})^{2} / E_{\text{beam}}$$

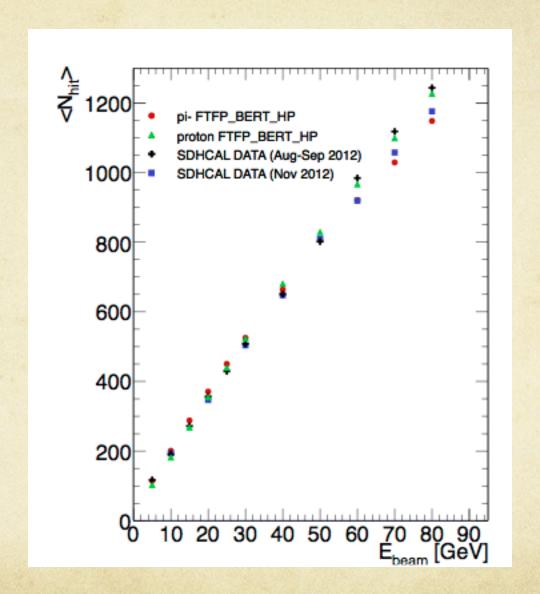
$$E_{\text{rec}} = \alpha (N_{\text{tot}}) N_{1} + \beta(N_{\text{tot}}) N_{2} + \gamma(N_{\text{tot}}) N_{3}$$

N₁,N₂ and N₃: exclusive number of hits associated to first, second and third threshold.

 α , β , γ are quadratic functions of the total number of hits (N_{tot}) For instance $\alpha = \alpha_0 + \alpha_1 N_{tot} + \alpha_2 N_{tot}^2$

Events of September runs corresponding to energies: 5, 10, 30, 60 and 80 GeV were used to fit the 9 parameters. This represents more than 50 k events.





HARDROC3

I2C link (@IPNL)

PLL: integrated before in a building block, first measurements are very good

Input frequency 2.5 MHz =>output frequency: 10, 20, 40, and 80 MHz available

Bandgap: new one with a better temperature sensitivity, tested in a building block

Roll mode

Triple voting

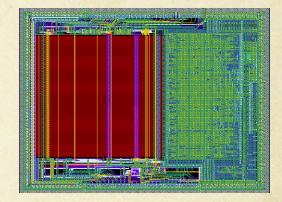
Temperature sensor: tested in a building block, slope - 6mV/°C

Die size ~30 mm2 (6.3 x 4.7 mm2)

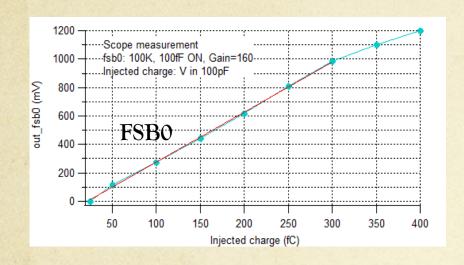
To be packaged in a TQFP208

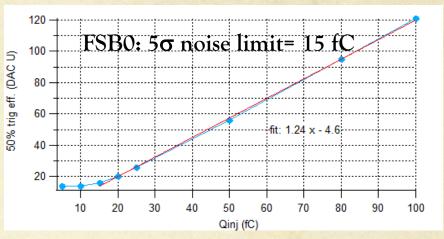
Submitted at the end of Feb 2013 (SiGe 0.35µm)

Currently tested.

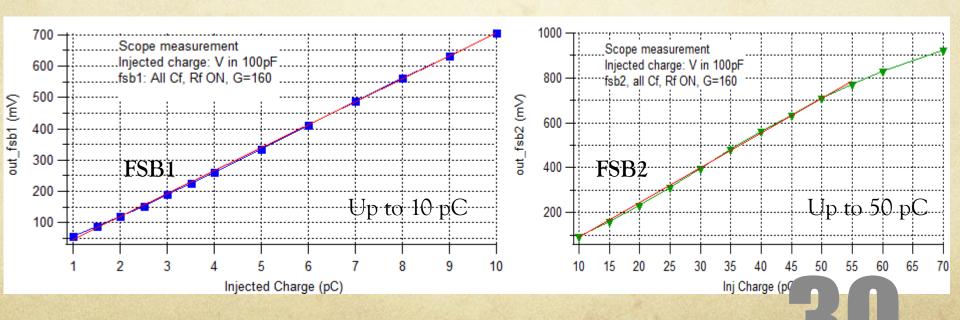


ANALOG PART: FSB LINEARITY



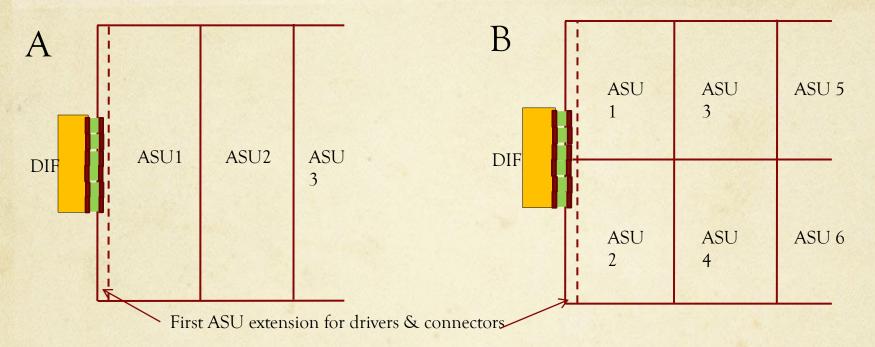


HR3 16/01/



New ASU layout options

As there will be only one DIF per plane, the distribution of the ASU boards in the plane will be rearranged to reduce the number of conections between the DIF and the plane



- In option B the common signals for the plane have to be sent twice (one per slab) while in option B they can be sent only once
- But, option A looks more risky from the point of view of the feasibility of the 1m long ASU boards.
- In both options the ASUs connected to the DIF will be a bit longer to host the connectors and the buffers for driving the long lines. This extension provides more freedom for the connectors selection and moves the drivers heat disipation to the ventilation area