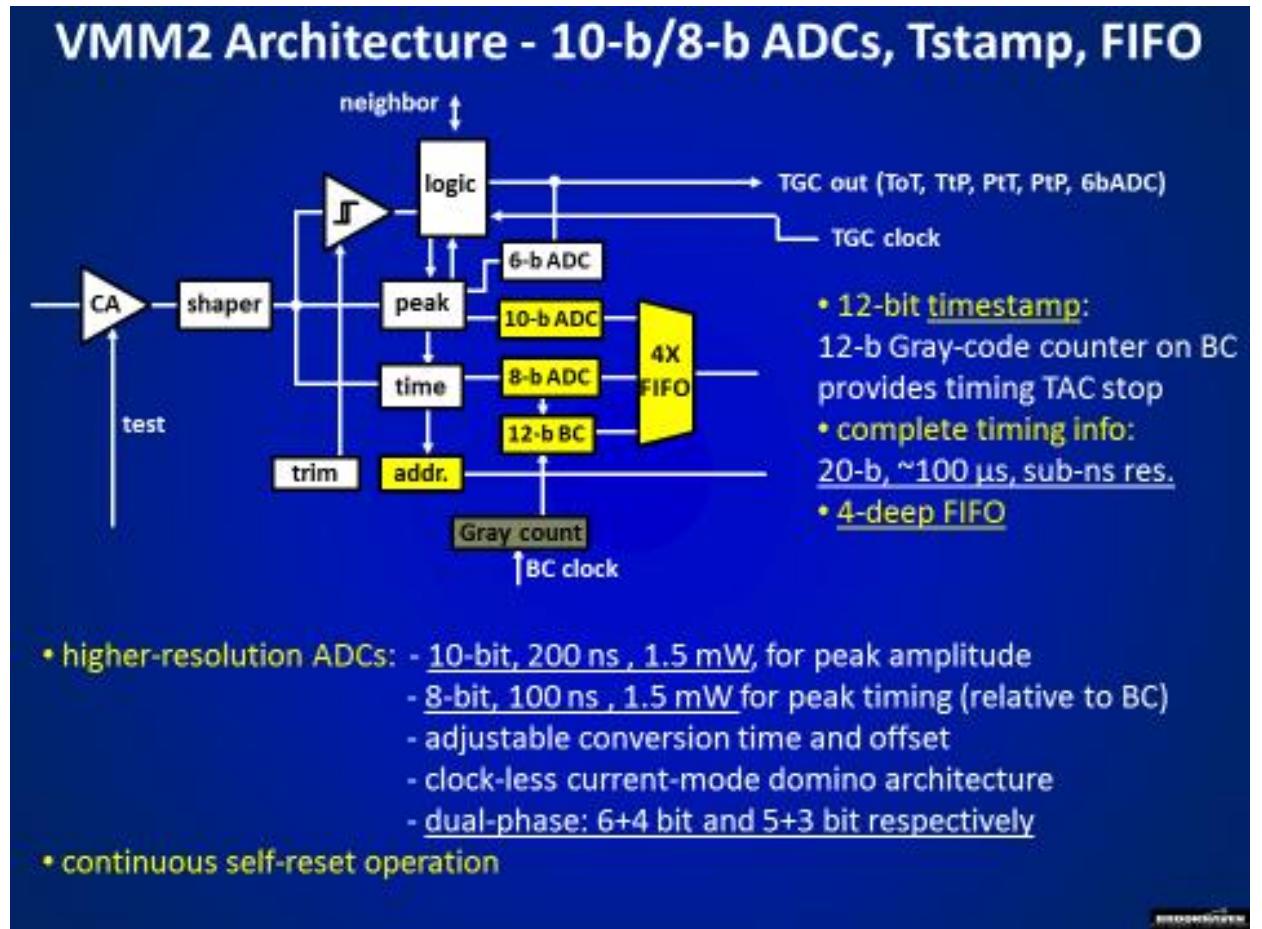
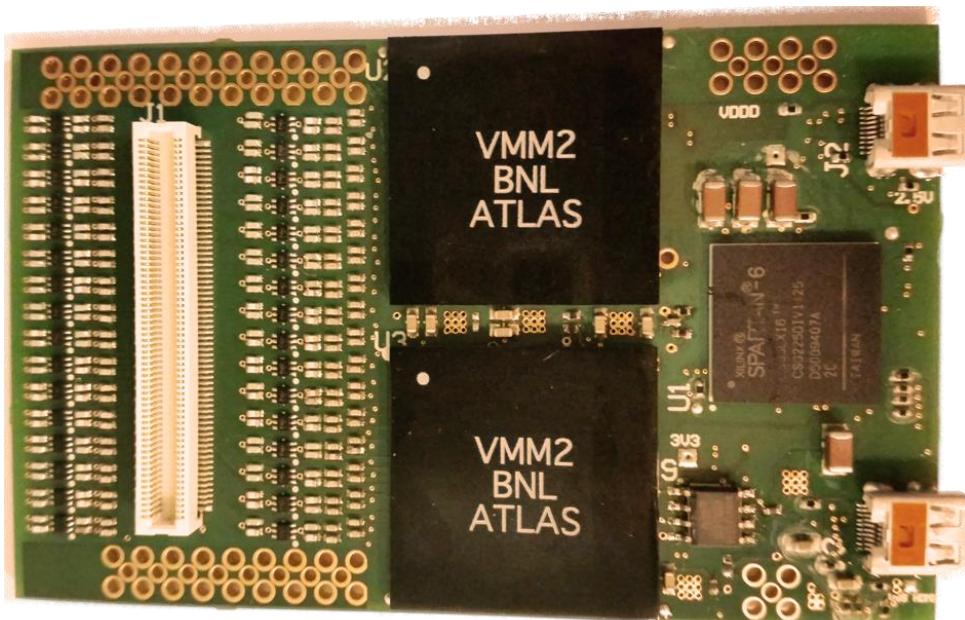


# SRS Activities at IFIN-HH

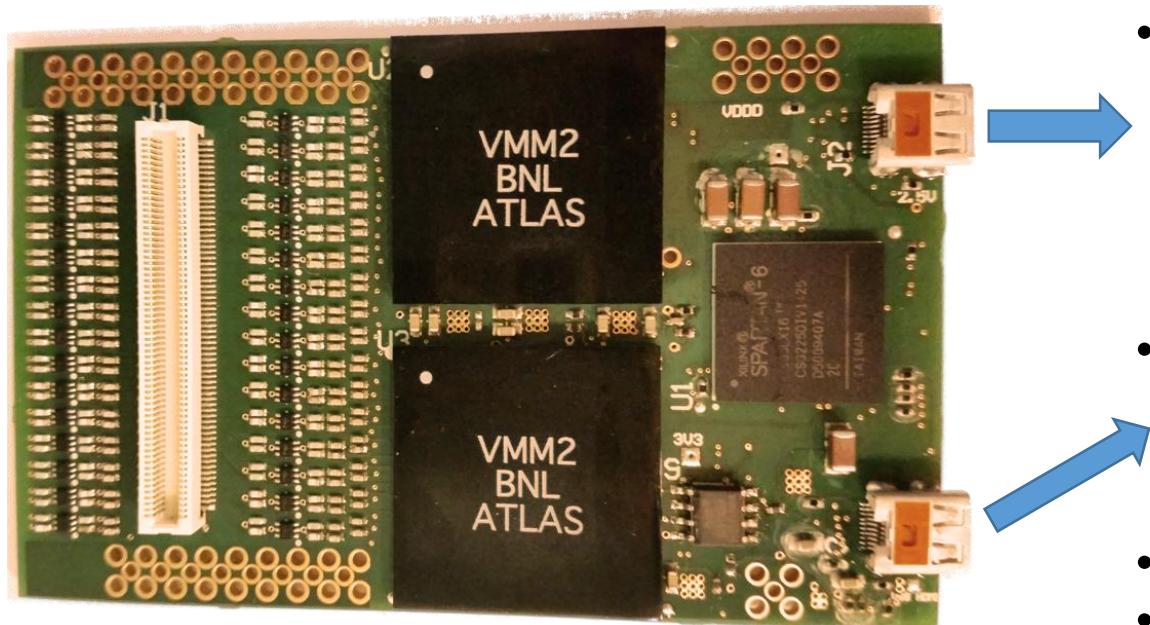
Sorin Martoiu (IFIN-HH Bucharest)

# VMM2 SRS Hybrid - Overview

G. De Geronimo, et al., VMM2 - An ASIC for the New Small Wheel,  
TWEPP 2014

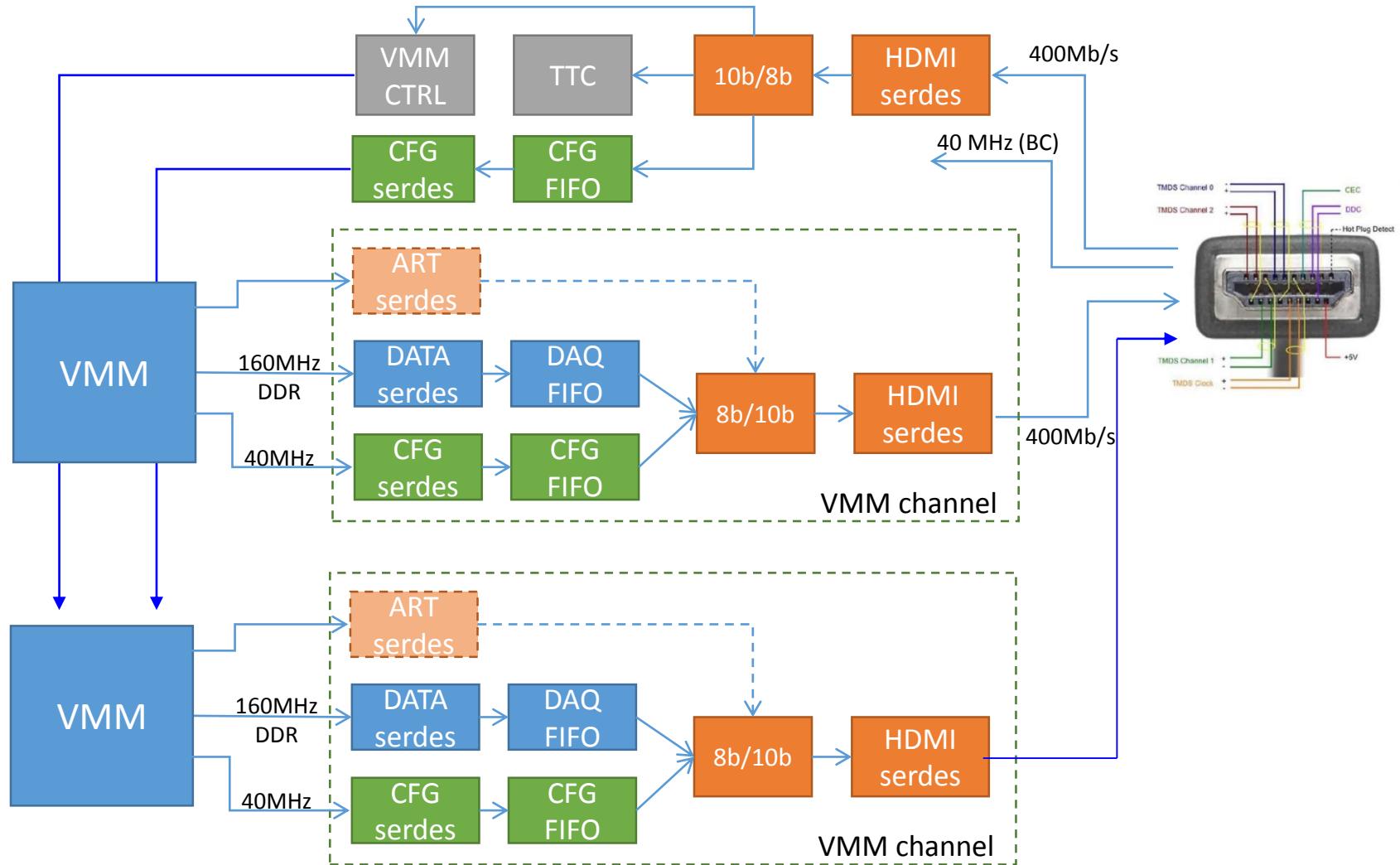


# VMM2 SRS Hybrid - Specifications

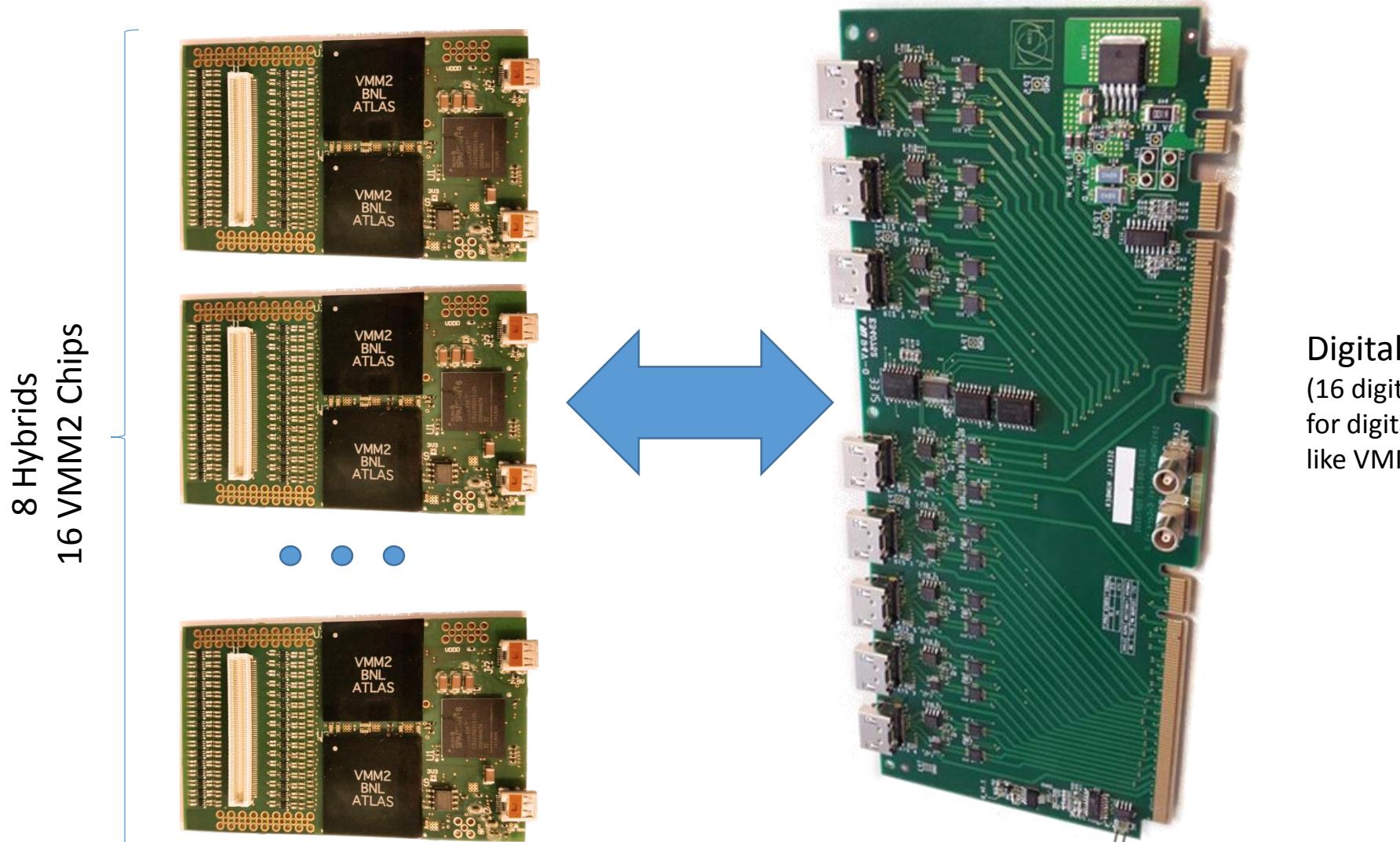


- Spartan6 LX9/16 FPGA for VMM control/data acquisition
- 1 x Micro HDMI for DAQ
  - Clk (40MHz)
  - TTC and configuration (400Mbps – 10b8b)
  - 2x data lines (400Mbps – 10b8b)
  - (opt.) ART info over data lines
- 1 x Micro HDMI for ART
  - Buffered ART signals (trigger signals)
  - (opt.) clk, ttc
- Power in via HDMI (> 2.7 V)
- On-board LDOs
  - 4 x 1.2V (analog, a/d, digital, fpga)
  - 1x 2.5V (fpga)

# VMM2 SRS Hybrid - Firmware

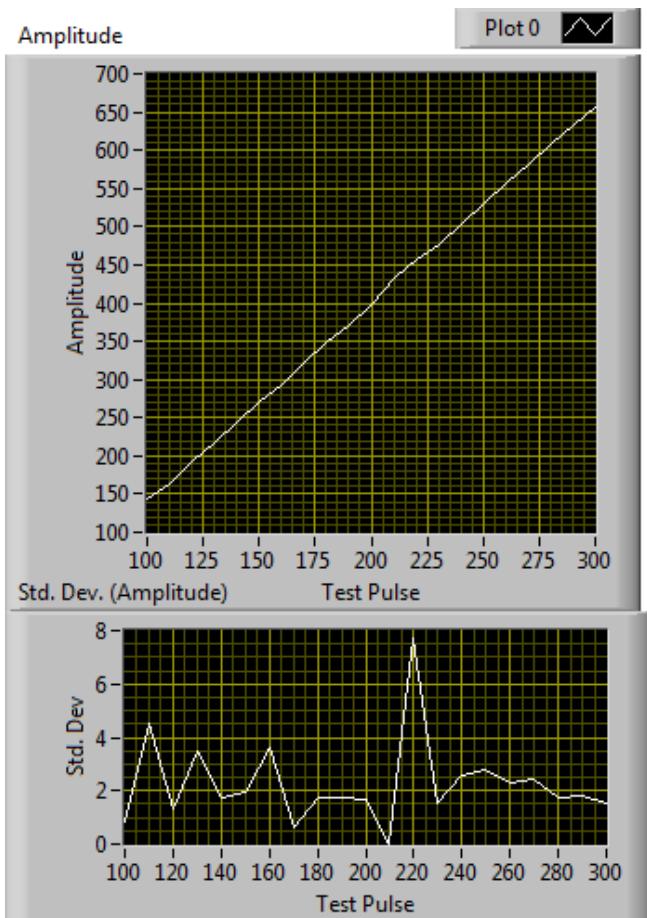


# VMM2 SRS Hybrid – Connectivity with SRS

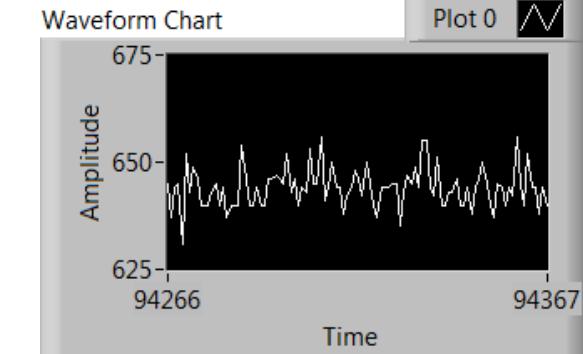
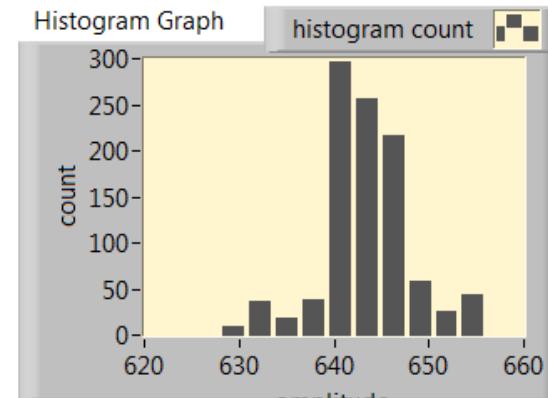


# VMM2 SRS Hybrid - Testing

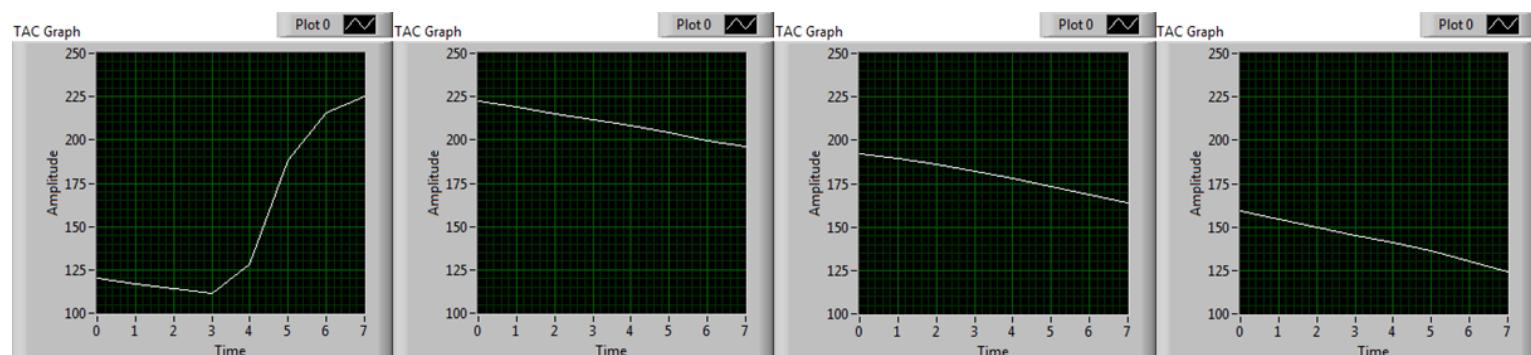
Amplitude (TestPulse) Scan



Pulse Amplitude Histogram



Timing Scan

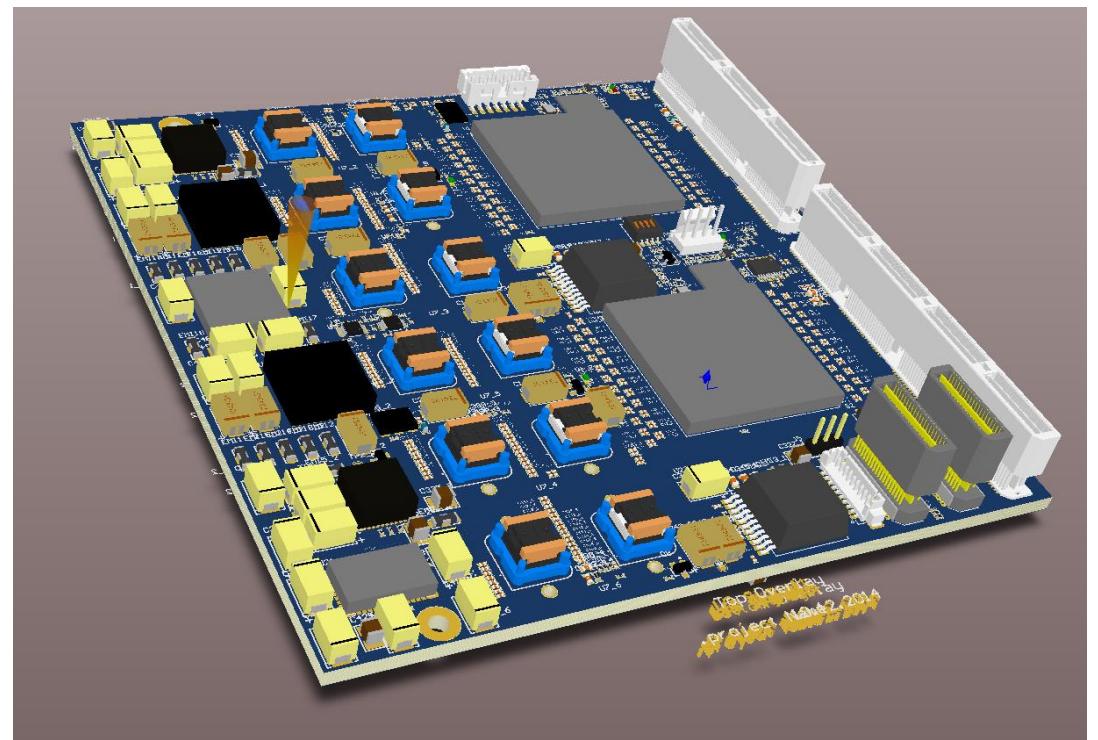
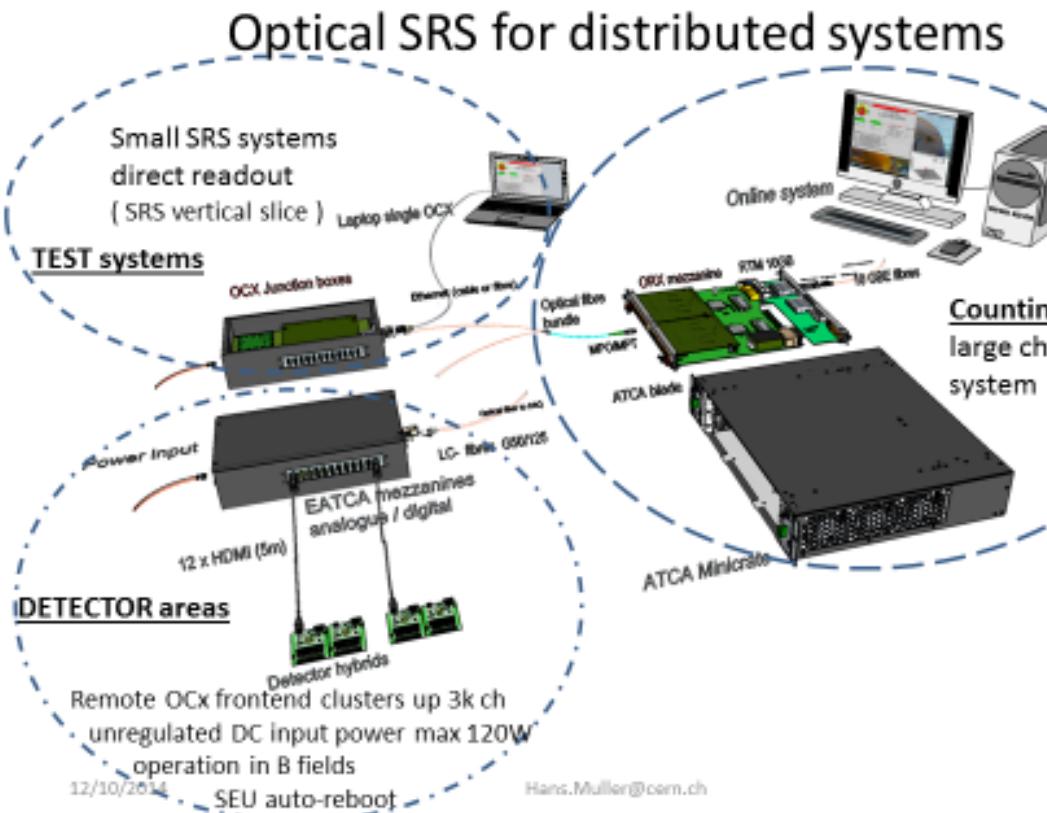


100 ns

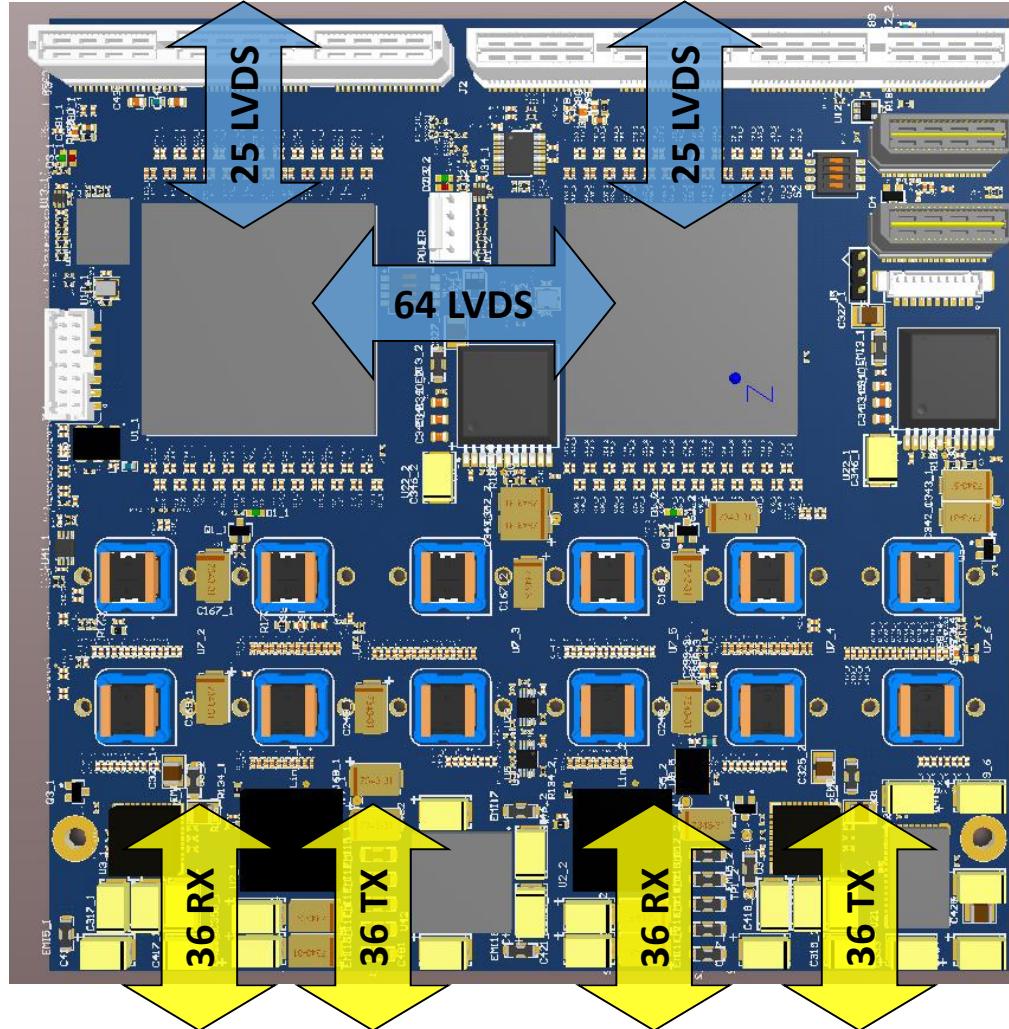
- Full characterization pending
- NSW MM / sTGC Beamtest going on right now

# High Density Optical Mezzanine for ATCA-SRS

## OVERVIEW

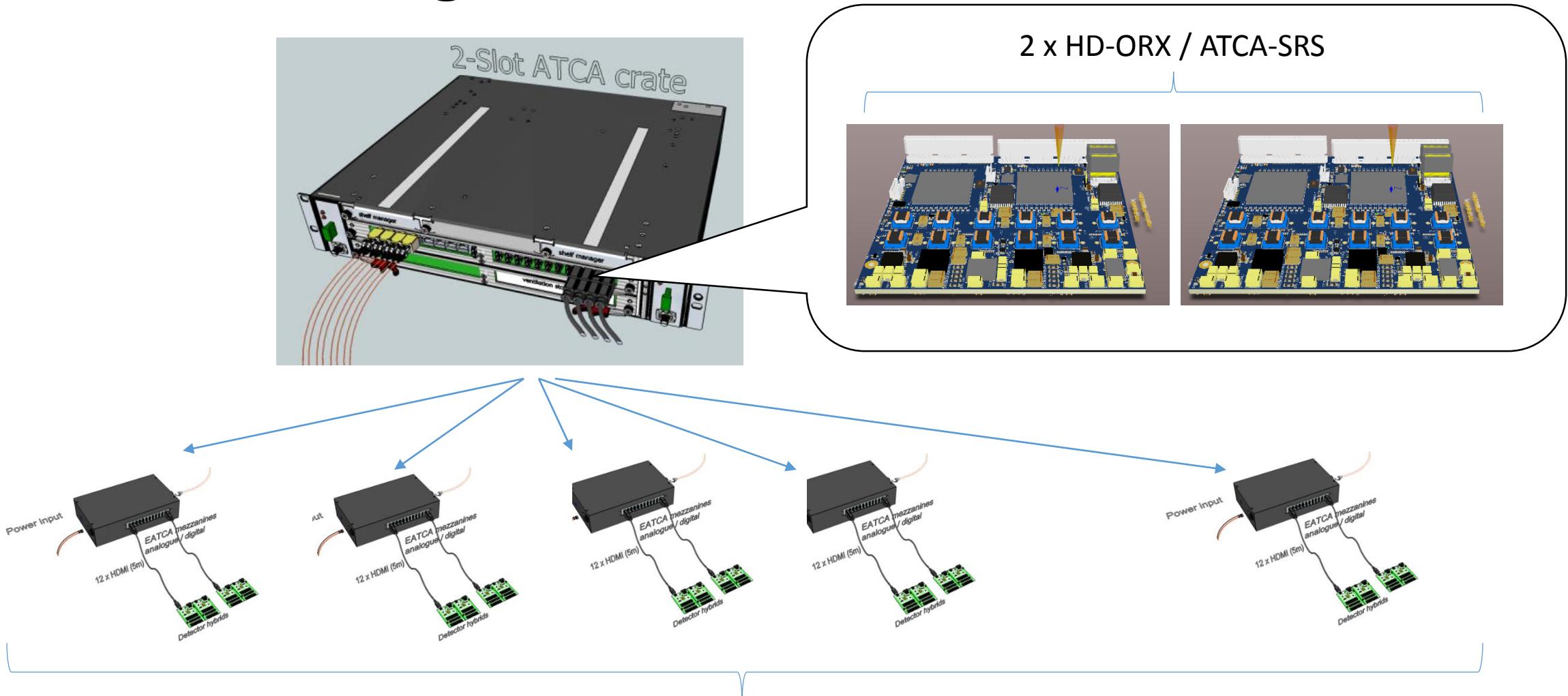


# High Density Optical Mezzanine for ATCA-SRS



- Build under specification for ATLAS NSW Trigger Processor
- 2 x Virtex-7 FPGA (356K – 477K logic cells)
- 72 RX + 72 TX Optical (36/36 each FPGA)
- 50 LVDS to blade
- 8 GTH to blade
- 64 LVDS inter-FPGA
- 8 GTH inter-FPGA
- Possibility to have light/low-cost version  
(1 x FPGA / 36 optical connections)
- Development under way
- First tests in Jan 2015

# HD-ORX Integration into ATCA-SRS



# Thank You