INNER TRACKING DEVICES AT THE Belle II EXPERIMENT

Outline
- The Inner Tracking System
- The PXD and SVD Main Features
- The System at Work
- The Production Status
- Conclusions

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EUROPEAN PHYSICAL SOCIETY CONFERENCE ON HIGH ENERGY PHYSICS
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The Inner Tracking System

The Vertex Detector (VXD) provides the precise measurement of the primary and secondary vertices of short-lived particles.

Typical Y(4S) Event

- Y(4S) center of mass is boosted
  - 7 GeV e− on 4 GeV e+→βγ = 0.28
  - reduced boost w.r.t. Belle
- average multiplicities
  - 11 charged tracks
  - 5 neutral pions
  - 1 neutral kaon
- soft charged tracks momentum spectrum

The most important factors affecting the precision of the vertex position determination are:
- the distance of the first measured hit
- the effect of multiple scattering

Other important factors taken into account in the design are:
- single hit resolution
- impact of the machine background in terms of occupancy and radiation damage
The VXD is composed of two systems, PXD and SVD, that are complementary to each other.

The combination of these two systems allow to reach the expected precision on tracking (see right plot) and vertexing.

Pixel Detector (PXD)
2 layers of DEPFET pixels (layers 1 & 2)
- innermost layer very close to IP ($r = 1.4$ cm)
- very low material budget ($\sim 0.2\% X_0$)
- excellent spatial granularity ($\sigma \approx 15$ µm)

Silicon Vertex Detector (SVD)
4 layers of double sided silicon strip detector (layers 3 to 6)
- excellent timing ($\sigma \sim 2-3$ ns)
- low material budget ($\sim 0.8\% X_0$)
- larger outer radius ($r = 14$ cm)
The Pixel Detector
The Pixel Matrix

**DEPleted p-channel Field Effect Transistor ~ DEPFET**

- fully depleted → large signal & fast signal collection
- low capacitance & internal amplification (0.5 nA/e⁻) → low noise
- the charge collected in the internal gate is digitised only when the FET is on → low power consumption
- 90 step complex fabrication process

<table>
<thead>
<tr>
<th>Inner layer (L1)</th>
<th>Outer layer (L2)</th>
</tr>
</thead>
<tbody>
<tr>
<td># modules</td>
<td>2 x 8</td>
</tr>
<tr>
<td></td>
<td>2 x 12</td>
</tr>
<tr>
<td>distance from IP (cm)</td>
<td>1.4</td>
</tr>
<tr>
<td></td>
<td>2.2</td>
</tr>
<tr>
<td>thickness (µm)</td>
<td>75</td>
</tr>
<tr>
<td></td>
<td>75</td>
</tr>
<tr>
<td>total # pixels</td>
<td>3.072 x 10⁶</td>
</tr>
<tr>
<td></td>
<td>4.608 x 10⁶</td>
</tr>
<tr>
<td>pixel size (µm²)</td>
<td>55, 60 x 50</td>
</tr>
<tr>
<td></td>
<td>70, 85 x 50</td>
</tr>
<tr>
<td>sensitive area (mm²)</td>
<td>44.8 x 12.5</td>
</tr>
<tr>
<td></td>
<td>61.44 x 12.5</td>
</tr>
<tr>
<td>sensor length (mm)</td>
<td>90</td>
</tr>
<tr>
<td></td>
<td>123</td>
</tr>
<tr>
<td>frame/row rate</td>
<td>50 kHz / 10 MHz</td>
</tr>
<tr>
<td></td>
<td>50 kHz / 10 MHz</td>
</tr>
</tbody>
</table>

- active region with different z-pixel-pitch to optimise readout
- VS wanted precision
- most of the readout region is outside the tracking volume

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The Readout Sequence

Rolling Shutter Mode
- the readout is not destructive
- all rows are sensitive, only one is active
- only when the gate is ON the current circulates
  → low power consumption
- read-clear cycle is 100 ns
- readout time is 20 \( \mu s \) for the entire frame

Gated-Mode Operation
2 noisy (injected) bunches over 2500 would result in huge occupancy and 20\% of dead time in the PXD
- disable the PXD (no charge collected in the internal gate) in a window of 300 ns around the transit of the noisy bunches
Control & Readout Electronics

Drain Current Digitizer (DCD)
- 8 bit ADCs
- Compensates for pedestal current variation (2bit DAC)
- Programmable gain

Switcher
- Fast voltage pulses up to 20V to activate gate rows and to clear the internal gate

Data Handling Processor (DHP)
- Pedestal correction
- Common mode correction
- Controls the Switcher sequence

Kapton Flex cable
- Power Supply via soldered contacts and bond wires
- Data transmission via bond wires

“all-silicon module”
- All the ladder components are silicon-based
  - Silicon sensor
  - Metal connections from sensor to the ASICs are integrated in the silicon substrate
  - Self-supported silicon structure

Large prototype matrix:
- Belle II pixel cell design: 50x75x50 µm³
- All readout components installed
- Smaller pixel matrix, 640x192
The Silicon Vertex Detector
The SVD Silicon Sensors

- 4 layers of DSSD on N-type silicon with AC coupled readout
- individual readout on each silicon sensor:
  - straightforward for sensors facing the non-tracking region
  - origami concept for all the other sensors (see next slide)
- lamp-shade geometry for layers 4, 5, and 6
  - optimize track incident angle
  - reduced material budget in the forward region ($\theta<0.7$)

Three sensor layouts, to reduce the design and production cost:

<table>
<thead>
<tr>
<th>layer</th>
<th>type</th>
<th>readout strip (p/r-(\phi))</th>
<th>readout strip (n/z)</th>
<th>strip pitch (p/r-(\phi))</th>
<th>strip pitch (n/z)</th>
<th>sensors # (+ spares)</th>
<th>active area (mm(^2))</th>
</tr>
</thead>
<tbody>
<tr>
<td>4,5,6</td>
<td>Large</td>
<td>768</td>
<td>512</td>
<td>75 µm</td>
<td>240 µm</td>
<td>120+18</td>
<td>122.90x57.72 = 7029.88</td>
</tr>
<tr>
<td>4,5,6</td>
<td>Trapezoidal</td>
<td>768</td>
<td>512</td>
<td>50-75 µm</td>
<td>240 µm</td>
<td>38+6</td>
<td>122.76x(57.59+38.42)/2 = 5893.09</td>
</tr>
<tr>
<td>3</td>
<td>Small</td>
<td>768</td>
<td>768</td>
<td>50 µm</td>
<td>160 µm</td>
<td>14+4</td>
<td>122.90x38.55 = 4737.80</td>
</tr>
</tbody>
</table>

Radiation length VS polar angle
The Origami Concept

- SVD will operate at a high-luminosity machine ($8 \times 10^{35} \text{cm}^{-2}\text{s}^{-1}$)
- Need short strips & short pitch adapters
  ‣ reduce the occupancy
  ‣ reduce the noise (lower capacitance at the charge preamplifier input)
- Readout chips inside the tracking volume
- The “chip-on-sensor” Origami concept allows to minimise the analog path length

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!! hidden micro bonding below the pitch adapter !!

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SVD Hit Time Resolution

The readout chip: APV25

- developed for CMS by the Imperial College London and Rutherford Appleton Lab (0.25 μm CMOS process)
- read 128 channels per chip
- read several samples along the shaping curve (multi-peak mode)
- 50 ns shaping time → low occupancy
- Noise: 250e +36 e/pF → minimise C

- the shaped pulse is sampled at multiple points @ 40 MHz (25 ns)
  - bunch crossing frequency 500 MHz (2ns)
- the 3 (or 6) samples are fitted on FPGA to reduce the sensitive window
- the peaking time is estimated with a precision of 3 ns
4 SVD modules + 1 PXD module have been tested together at the DESY test beam facility:
- 2 to 6 GeV electrons
- trigger rate: a few kHz
- 1T magnetic field

Pocket DAQ version was also installed and functioning.

Online Tracking and Region Of Interest finding worked fine!

Region Of Interest (ROI) Finding
use the 4 SVD layers to find, fit and extrapolate the track back to the PXD layers and define ROIs where to expect signal hits:
- online tracking (fast and efficient)
- PXD and SVD DAQ talk to each other
VXD Production Status

2015
- Pilot run assembled (3 wafers)
- Start main sensor production, phase 2/3 (27 wafers)

2016
- DESY test beam with final ASICs
- Start forward & backward module production
- First mass production ladder L4-L6

2017
- PXD installation readiness at KEK
- Start of ladder mount to support structure

2018
- PXD+SVD combined cosmic test
- PXD+SVD installation readiness at KEK

Data taking

PXD

VXD
The Belle II Vertex Detector is composed by two systems with different characteristics, complementary to each other:

- PXD: unambiguous 2D position, very low material budget
- SVD: excellent time resolution, low material budget

The VXD will allow an unprecedented precision in the determination of the primary and secondary vertices.

The Vertex Detector construction is ongoing. The PXD and SVD will be integrated at KEK in June 2017 and installed in April 2018, to be ready for data taking starting in the end of 2018.
The Belle II Collaboration:

615 collaborators, 98 institutes, 23 countries

July 2015

Thank You!
Don't PANIC!
backup slides
The *Belle II* Detector

**EM calorimeter**
Csl(Tl), waveform sampling electronics (barrel)
Pure CsI + waveform sampling (end-caps) later

**Vertex Detector**
PXD: 2 layers Si pixels (DEPFET),
SVD: 4 layers double sided Si strips (DSSD)

**Vertex Detector**

**Central Drift Chamber**
He(50%):C₂H₆(50%),
smaller cell size,
long lever arm,
faster electronics

**Particle Identification**
Time-of-Propagation counter (barrel),
Proximity focusing Aerogel Cherenkov
Ring Imaging detector (forward)

**Kₐ & μ Detector**
Resistive Plate Counter (barrel outer layers),
Scintillator + WLSF + MPPC (end-caps, inner 2 barrel layers)

Electrons (7 GeV)

Positrons (4 GeV)
The Cooling System

- SVD and PXD share the same CO$_2$ system

CO$_2$ pipe holder

Giulia Casarosa

BelleII Vertex Detector
**PXD Sensor Processing**

**Phase I – before metal**
- Implantations
- Polysilicon
- Dielectric depositions

**Phase II – Aluminum**
- Metal 1
- Isolation
- Metal 2

**Phase III – Thinning & Copper**
- Handle Wafer Removal
- Dielectric deposition
- Metal 3
- Passivation

**thinning phase:**

![Thinning process](image)

- 450 μm
- 50 μm