Upgrade of the ALICE Inner Tracking System

L. Musa - CERN

LHeC Workshop
25 June, 2015
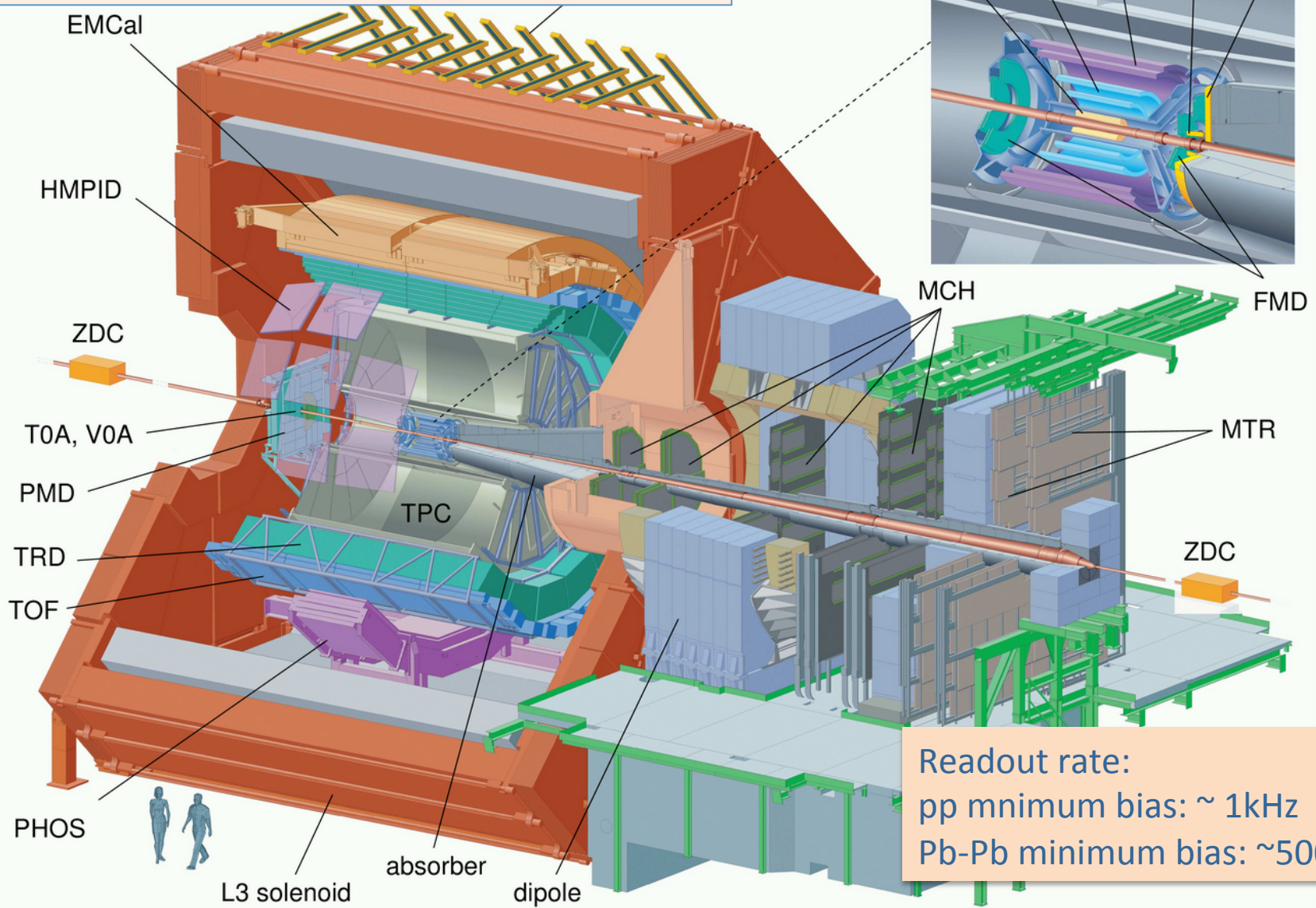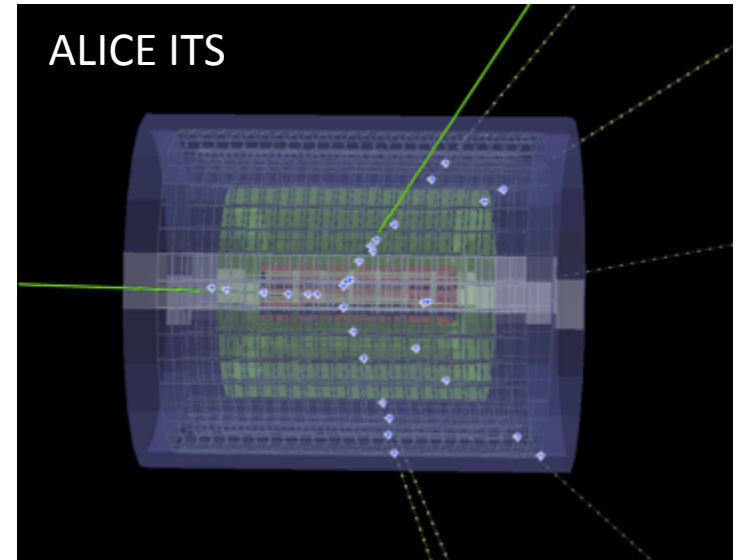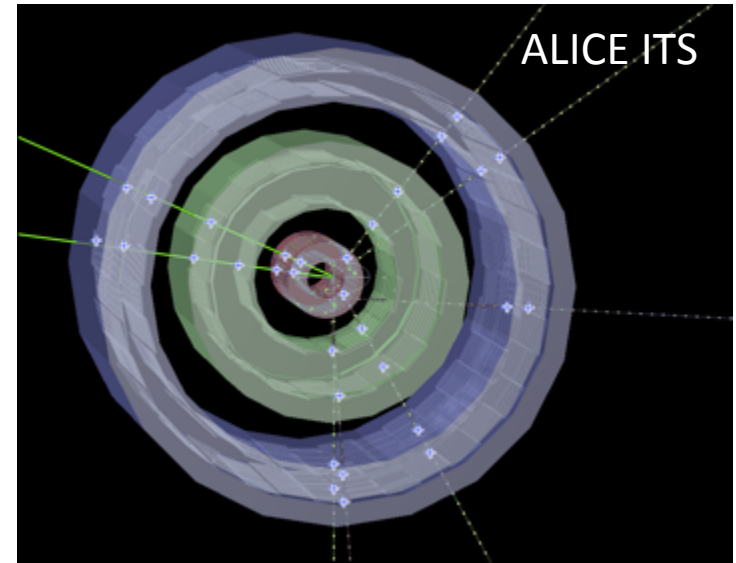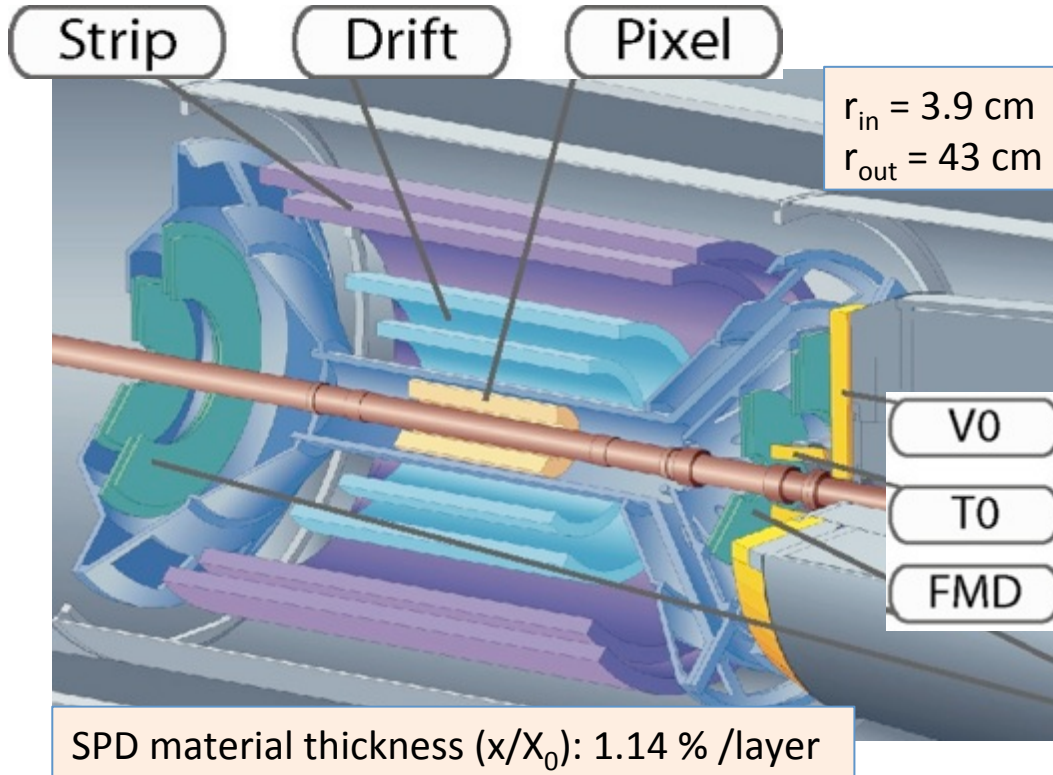
Upgrade of the ALICE Inner Tracking System

OUTLINE

⊙ ALICE current set-up and Inner Tracking System

⊙ Upgrade motivations and strategy

⊙ Upgrade design objectives

⊙ Layout and main components

⊙ Detector simulated performance

The Current ALICE Detector

Only LHC experiment dedicated to HI collisions

Readout rate:
pp mnimum bias: ~ 1kHz
Pb-Pb minimum bias: ~500 Hz

The Current ALICE Inner Tracking System

Strip | Drift | Pixel

r_{in} = 3.9 cm
r_{out} = 43 cm

V0
T0
FMD

SPD material thickness (x/X_0): 1.14 % /layer

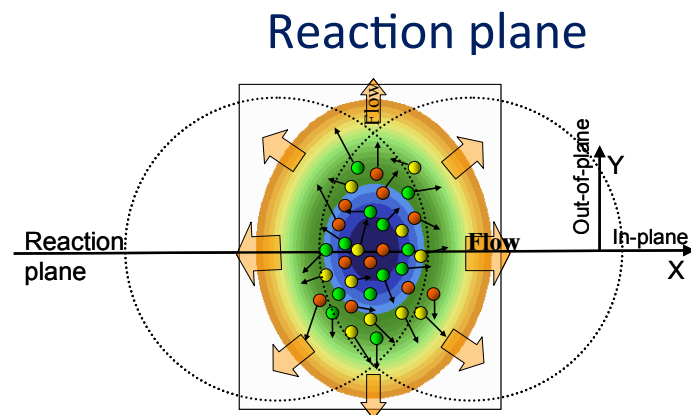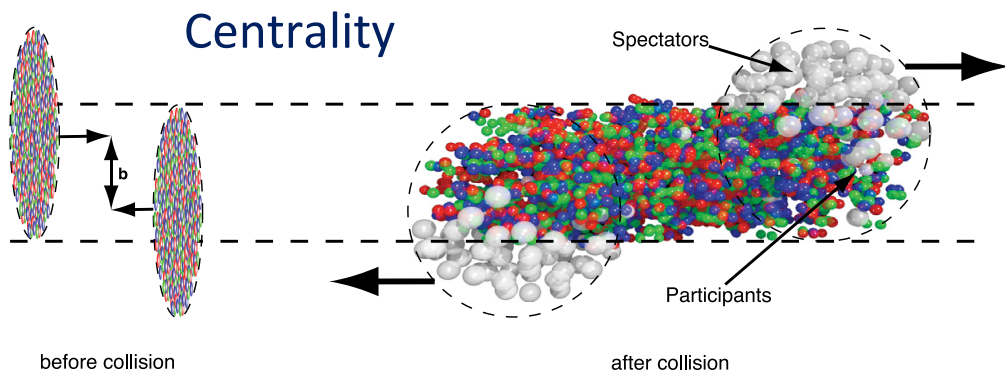ALICE ITS

ALICE ITS

Current ITS

6 concentric barrels, 3 different technologies

• 2 layers of silicon pixel (SPD)

• 2 layers of silicon drift (SDD)

• 2 layers of silicon strips (SSD)

ALICE Upgrade: study QGP properties

Progress on the characterization of QGP properties

- precision measurements of rare probes
- over a large kinematic range (from high to very low transverse momenta)
- and as function of multi-differential observables: centrality, reaction plane, …

Centrality

Spectators

Participants

before collision

after collision

Reaction plane

Flow

Out-of-plane

In-plane

Reaction plane

Flow

Y

X

One example:

precision measurements of spectra, correlations and flow of heavy flavour hadrons
at low transverse momenta (not possible to trigger!!)

ALICE Upgrade Strategy

This requires statistics (luminosity) and precision measurements

Target for **upgrade programme** (Run3 + Run4)

- Pb-Pb recorded luminosity ≥ 10 nb^{-1} ➡ 8×10^{10} events
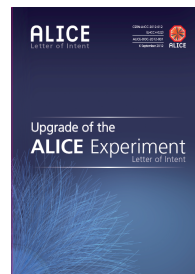
I. Upgrade detectors, readout systems and online systems to

- read out all Pb-Pb interactions at a maximum rate of 50kHz (i.e. L = 6×10^{27} cm^{-2}s^{-1}), with a minimum bias trigger (at present 500Hz)

➡ Gain a factor **100** in statistics over originally approved programme (Run1 + Run2)

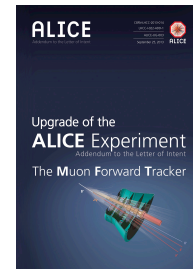II. Significant improvement of vertexing and tracking capabilities at low p_T

- **New Inner tracking System**

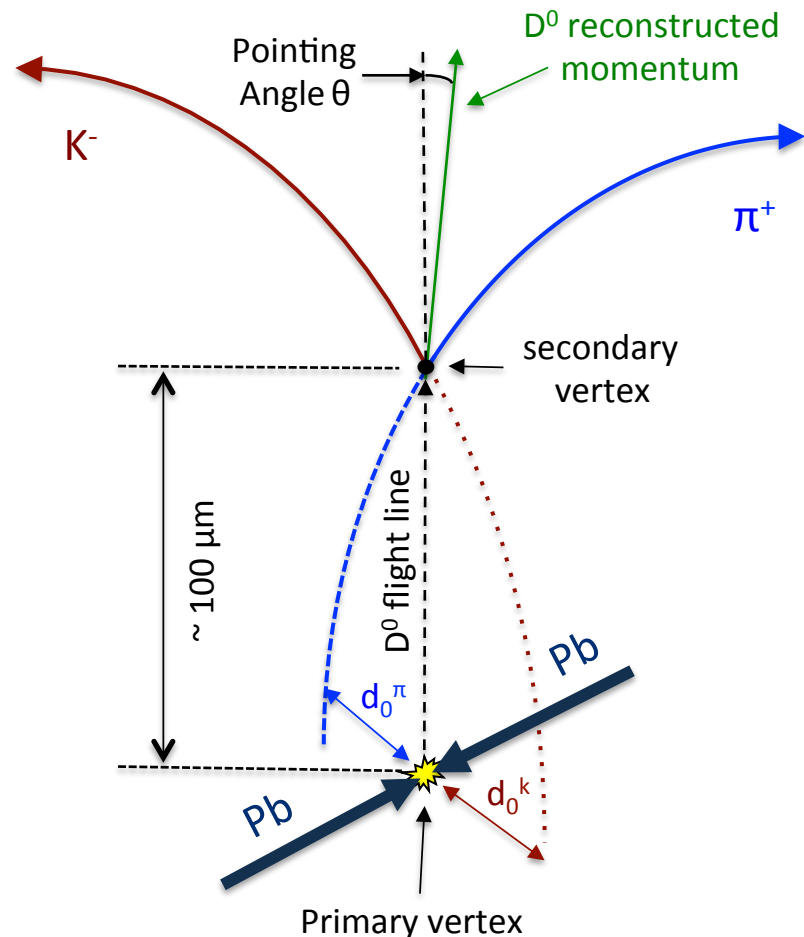**It targets LHC 2nd Long Shutdown (2018/19)**
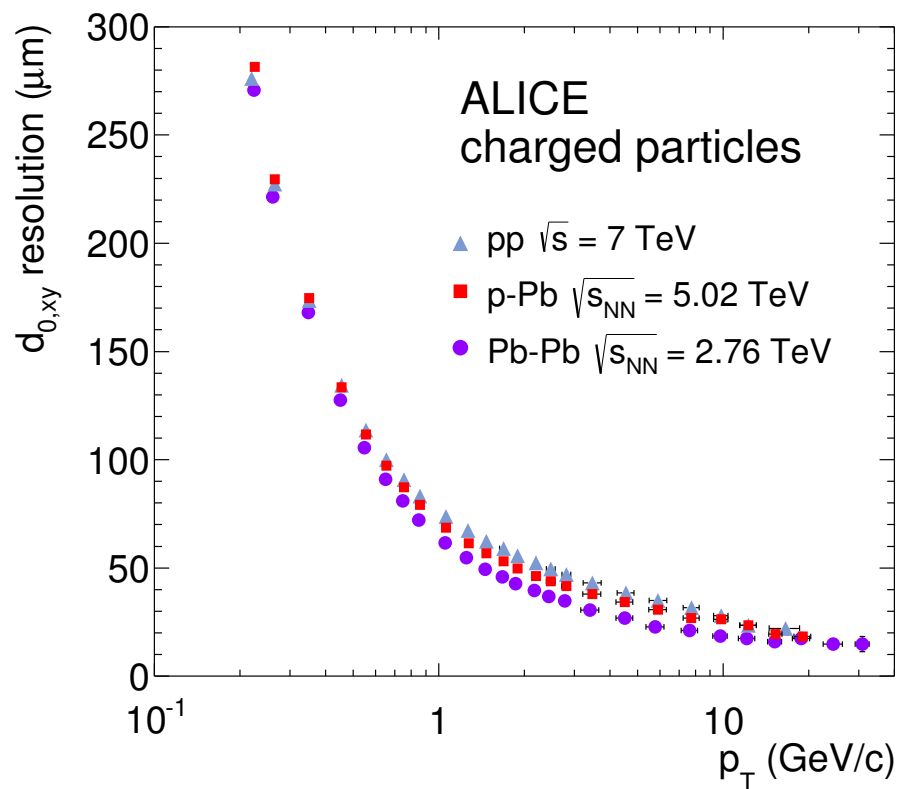
ALICE Upgrade LoI
September 2012

Addendum
September 2013

ITS – Secondary vertex determination

Example: D⁰ meson

Pointing Angle θ

D⁰ reconstructed momentum

K⁻

π⁺

secondary vertex

~ 100 μm

D⁰ flight line

d_0^π

d_0^k

Pb

Pb

Primary vertex

Very weak dependence on the colliding system

ALICE charged particles

▲ pp $\sqrt{s}$ = 7 TeV

■ p-Pb $\sqrt{s_{NN}}$ = 5.02 TeV

● Pb-Pb $\sqrt{s_{NN}}$ = 2.76 TeV

ALICE, Int. J. Mod. Phys. A29 (2014) 1430044

Analysis based on decay topology and invariant mass technique

ITS upgrade design objectives

1. Improve impact parameter resolution by a factor of ~3

- Get closer to IP (position of first layer): 39mm ➡ 23mm

- Reduce x/X_0 /layer: ~1.14% ➡ ~ 0.3% (for inner layers)

- Reduce pixel size: currently 50μm x 425μm ➡ O(30μm x 30μm)

CERN-LHCC-2013-24

2. Improve tracking efficiency and p_T resolution at low p_T

- Increase granularity:

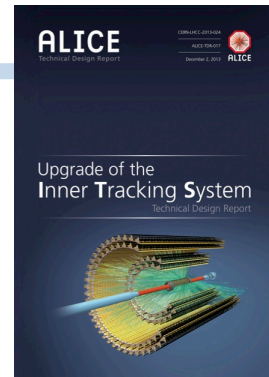 - 6 layers ➡ 7 layers

  - silicon drift and strips ➡ pixels

3. Fast readout

J. Phys. G (41) 087002

- readout Pb-Pb interactions at > 100 kHz and pp interactions at ~ several 10^5 Hz (currently limited at 1kHz with full ITS)
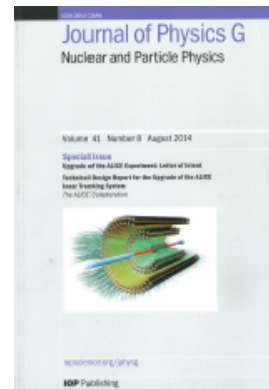
4. Fast insertion/removal for yearly maintenance

- possibility to replace non functioning detector modules during yearly shutdown

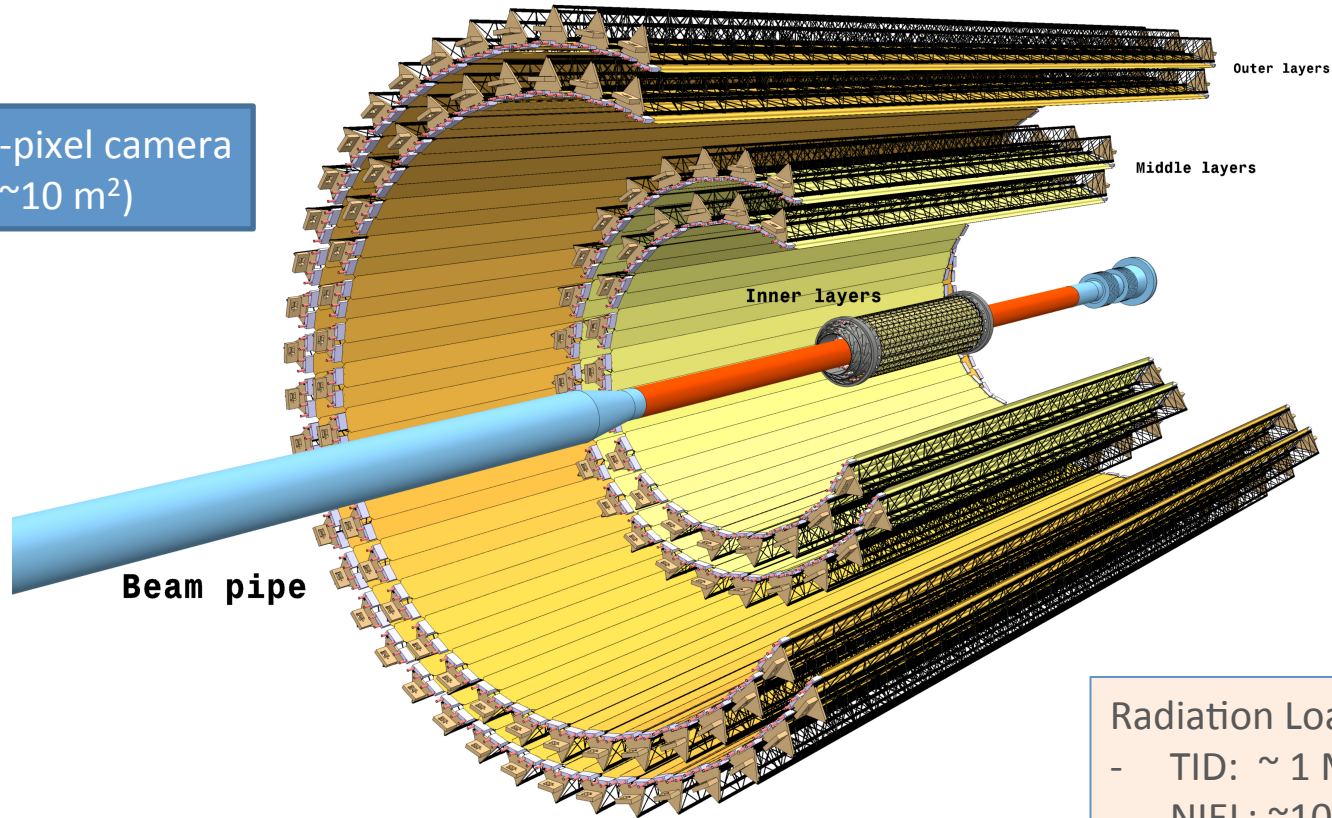Install detector during LHCC LS2 (2018-19)

New ITS Layout

12.5 G-pixel camera (~10 m²)

Outer layers

Middle layers

Inner layers

Beam pipe

Radiation Load
- TID: ~ 1 Mrad
- NIEL: ~10^{13} 1MeV n_{eq} / cm²

7-layer barrel geometry based on MAPS

r coverage: 23 – 400 mm

η coverage: |η| ≤ 1.22
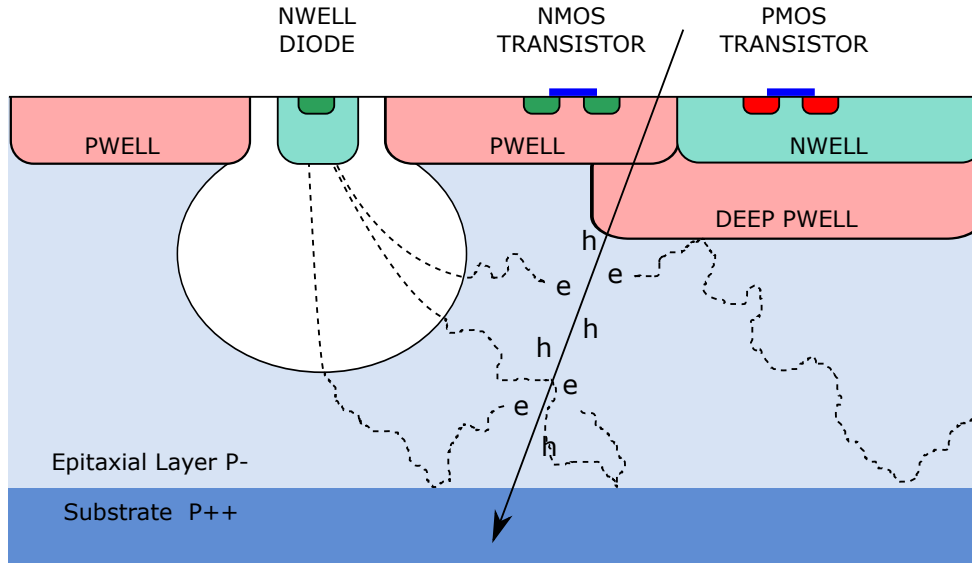for tracks from 90% most luminous region

3 Inner Barrel layers (**IB**)

4 Outer Barrel layers (**OB**)

Material /layer : 0.3% X_0 (IB), 1% X_0 (OB)

ITS Pixel Chip – technology choice

CMOS Pixel Sensor using TowerJazz 0.18μm CMOS Imaging Process

Tower Jazz 0.18 μm CMOS
- feature size   180 nm
- metal layers   6
→ Suited for high-density, low-power
- Gate oxide   3nm
→ Circuit rad-tolerant

▶ High-resistivity (> 1kΩ cm) p-type epitaxial layer (20μm - 40μm thick) on p-type substrate

▶ Small n-well diode (2-3 μm diameter), ~100 times smaller than pixel => low capacitance

▶ Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode

▶ Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

ITS Pixel Chip – two architectures

ALPIDE (BASELINE)

continuous
or
external trigger

MISTRAL - O

rolling shutter
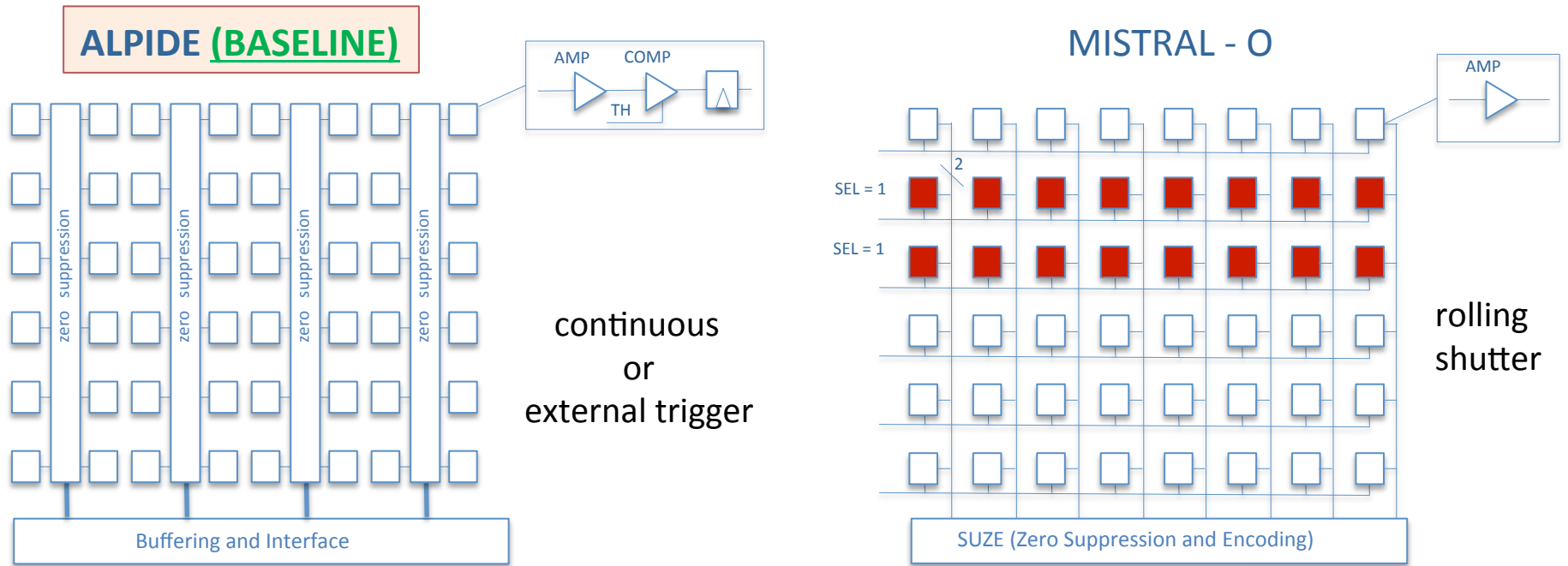
	ALPIDE		MISTRAL - O
Pixel pitch	28μm x 28μm	Pixel pitch	36μm x 64μm
Event time resolution	<2μs	Event time resolution	~20μs
Power consumption	39mW/cm^2	Power consumption[*]	97mW/cm^2
Dead area	1.1 mm x 30mm	Dead area	1.7 mm x 30mm

ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

[*] might further reduce to 73mW/cm^2

pALPIDE-1 (May 2014) – first full-scale prototype

ALPIDE Full Scale prototype

- Dimensions: 30mm x 15 mm

- Pixel Matrix: 1024 cols x 512 rows

- Final pixel pitch: 28μm x 28μm

- Power consumption: < 40mW/cm^2

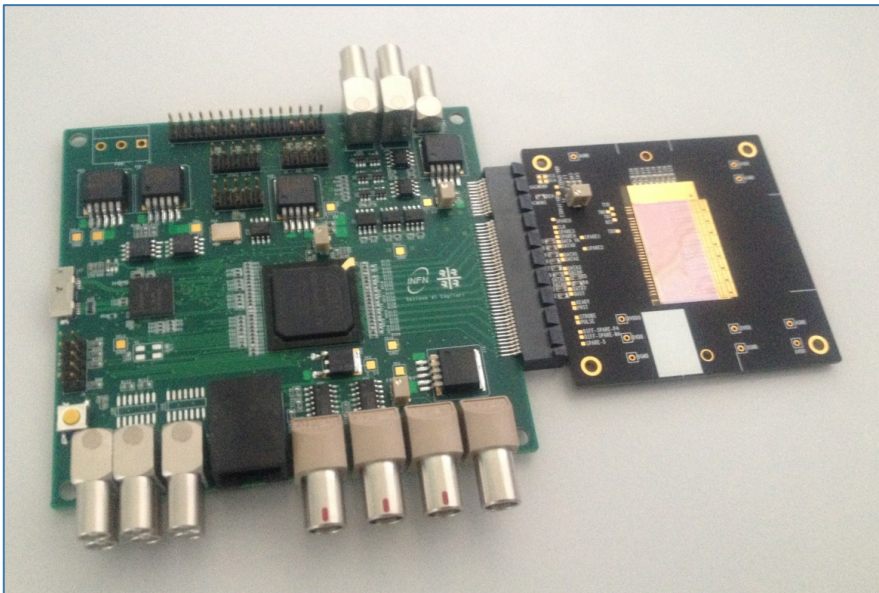- Interface pads over matrix
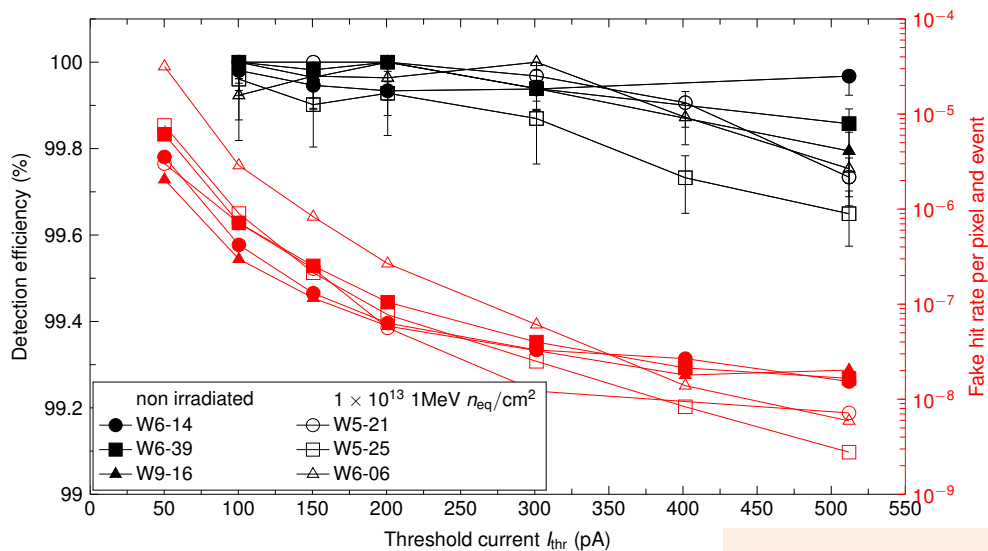
- 1 register/pixel, no final interface

pads over matrix
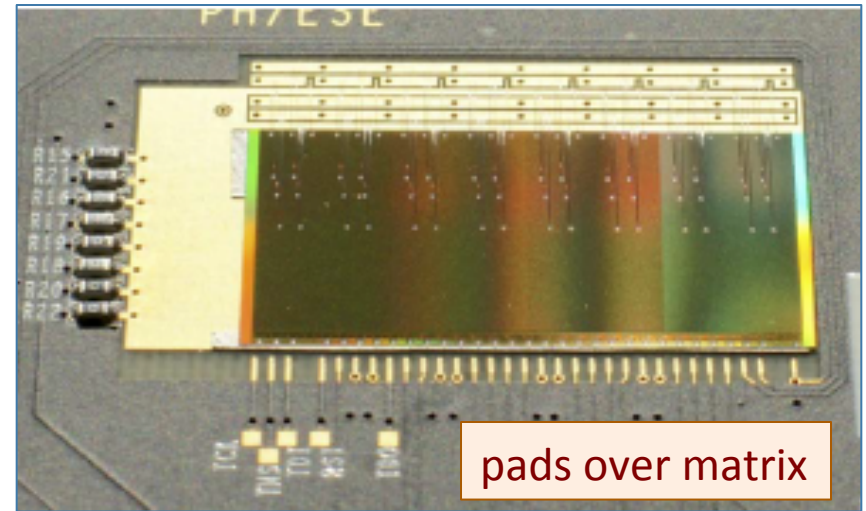
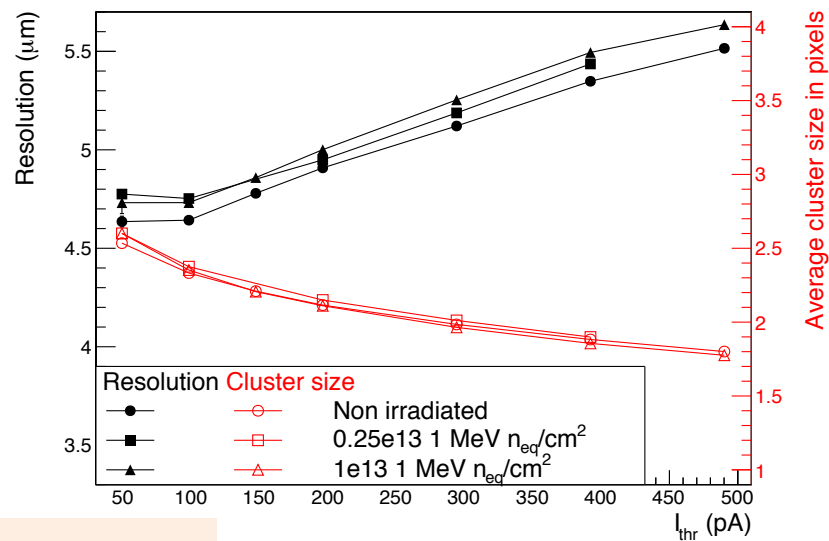Figure: picture of pALPIDE-1

7-plane telescope based on pALPIDE-1 chip
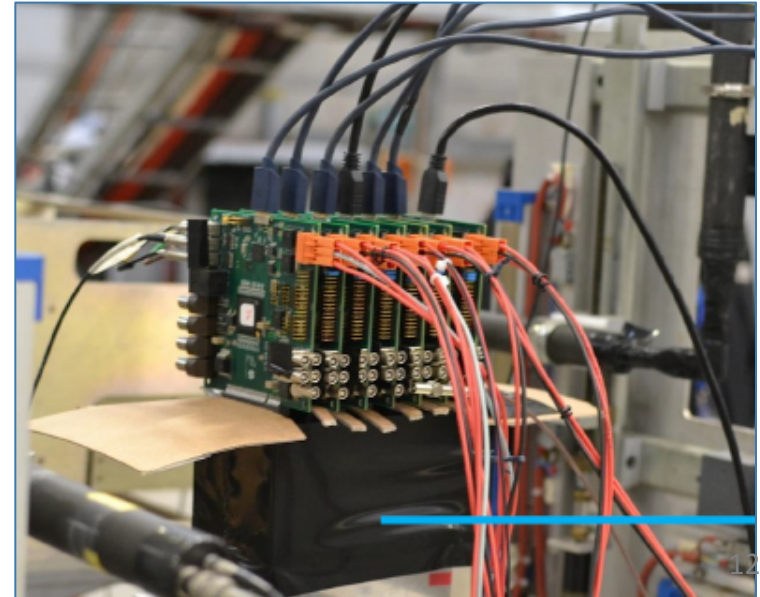
Efficiency and fake hit rate

Spatial resolution

50 pA ~80 e,   500 pA ~180 e

CERN PS: 5 – 7 GeV π^- (Dec 2014)

- Results refer to 50 μm thick chips:
  - 3 non irradiated and
  - 3 irradiated with 10^{13} 1MeV n_{eq} / cm^2

- CERN PS: 5 – 7 GeV π^- (Sep 2014)

- Results refer to 50 μm thick chips:
  - non irradiated
  - irradiated with 0.25x10^{13} n / cm^2
  - irradiated with 10^{13} n / cm^2

λ_{fake} << 10^{-5} / event/pixel @ ε_{det} > 99%   ➡   very large margin over design requirements

σ_{det} ~ 5 μm ➡ large margin of operation

New ITS layout

Beam pipe

Outer layers

Middle layers

Inner layers

90 Outer layer STAVES

54 Middle layer STAVES

48 Inner layer STAVES
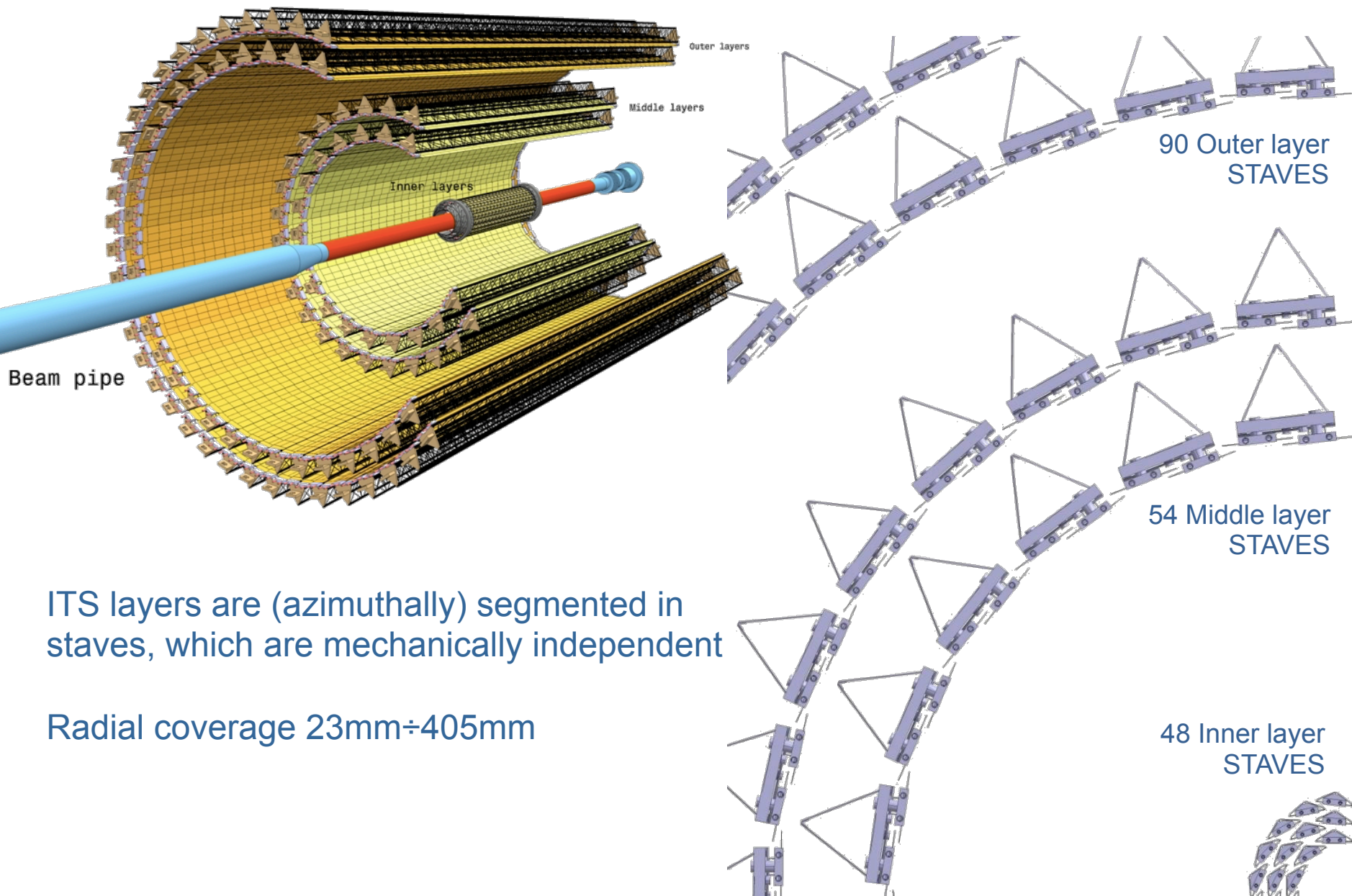
ITS layers are (azimuthally) segmented in staves, which are mechanically independent

Radial coverage 23mm÷405mm

New ITS Layout - Inner Barrel Stave

Mean $X/X_0 = 0.276\%$

Cooling Ducts

Space Frame

Cold Plate

Mechanical Connector

9 Pixel Chips

Soldering Balls

Flex Printed Circuit

Total weight 1.5 grams
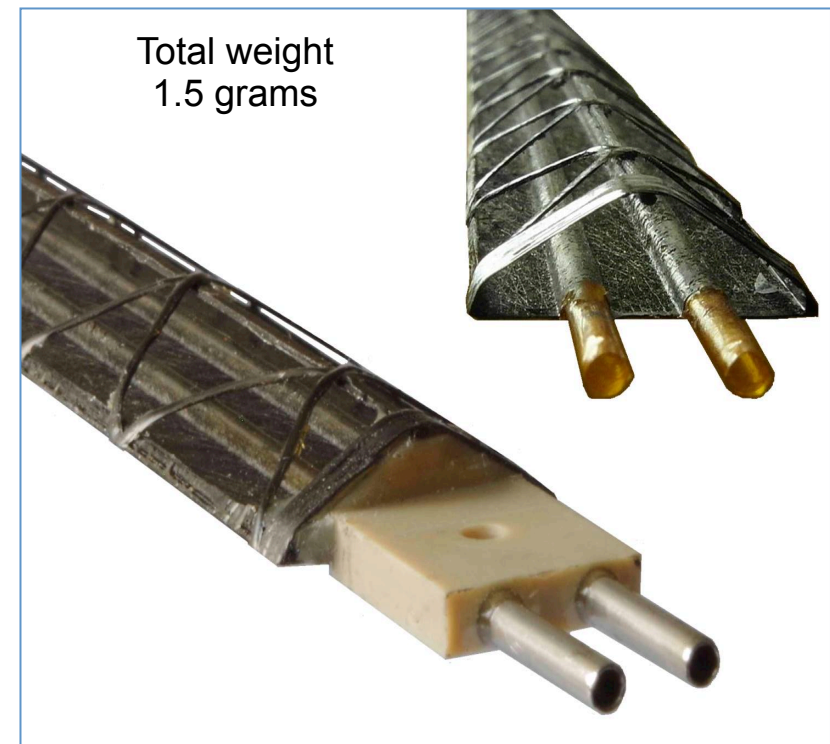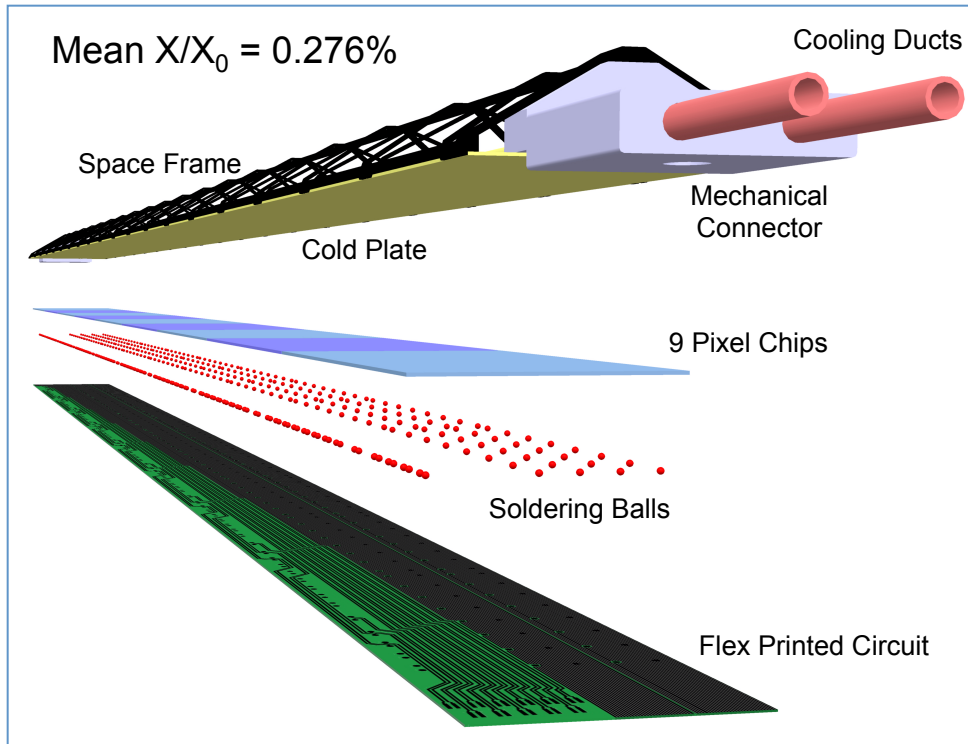
<Radius> (mm): 23,31,39

Nr. of staves: 12, 16, 20

Nr. of chips/layer: 108, 144, 180

Power density: < 100 mW/cm^2

Length in z (mm): 290

Nr. of chips/stave: 9

Material thickness: ~ 0.3% X_0

Throughput (@100kHz): < 80 Mb/s × cm^{-2}

Interconnection of pixel chip to flex PCB

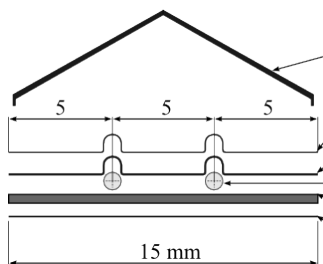## Laser soldering: Interconnection of Pixel chip on flexible printed circuit

Laser soldering machine
(Dr. Mergenthaler GMBH

2 Layers, Vacuum deposition

Layer	Thickness
Coverlay	20 µm
Metal	25 µm
Polyimide	75 µm
Metal	25 µm
Coverlay	20 µm
Chip	50 µm

200 µm
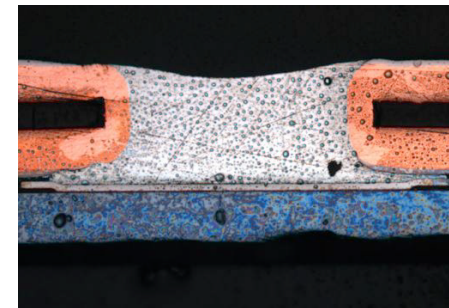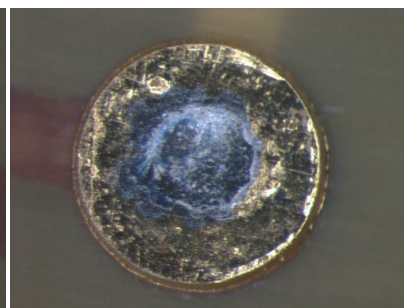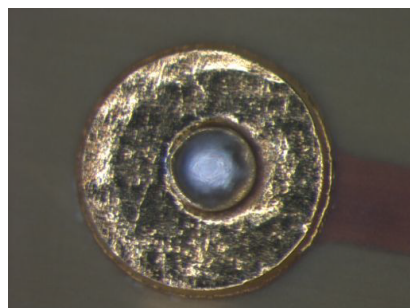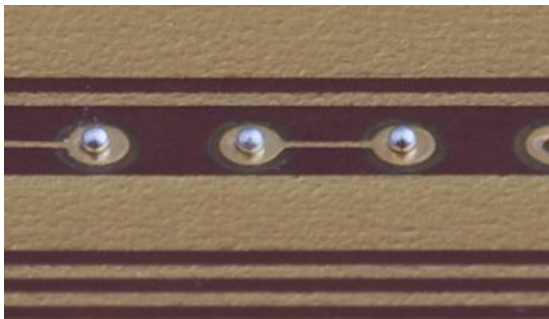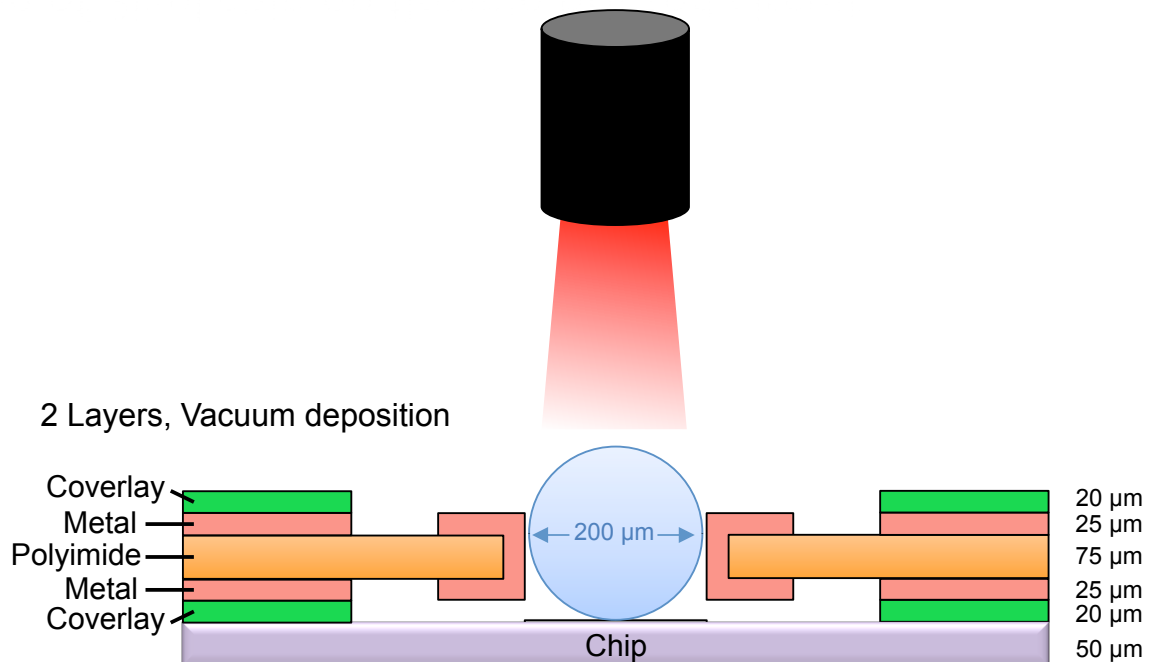
Inner Barrel Stave - thermal test

Transversal section:

P_{in}= 1 bar
T_{in}=15.8° C

Q= 3 L/h

T_{out}=16.6 °C
P_{out}= 0.7 bar

Heating is provided by dummy metalized chip : thickness= 50 µm chip + 20/200 nm Titanium /Platinum

Nominal

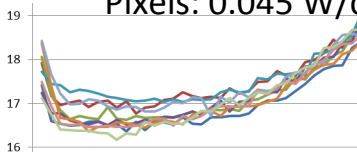Periphery: 0.145 W/chip
Pixels: 0.03 W/chip

Min T pixel =16° C
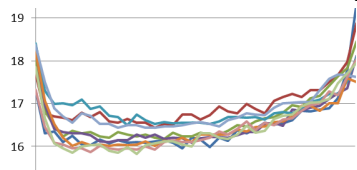
Max T periph=17.5° C

50% safety factor

Periphery: 0.217 W/chip
Pixels: 0.045 W/chip
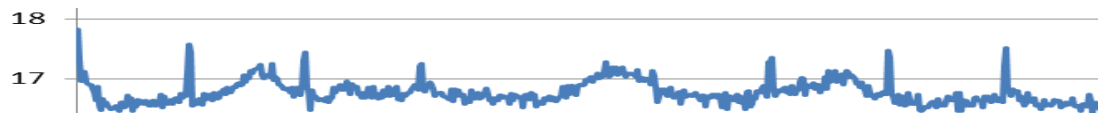
Min T pixel =16.5° C

Max T periph=18.5° C

status
verification of thermal behaviour with
- non uniform power dissipation
- uniform layer of glue
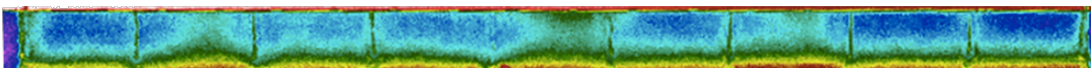
ongoing
verification of thermal behaviour with
- non uniform power dissipation
- no glue at the periphery (2mm) of the chip

no glue

glue

no glue
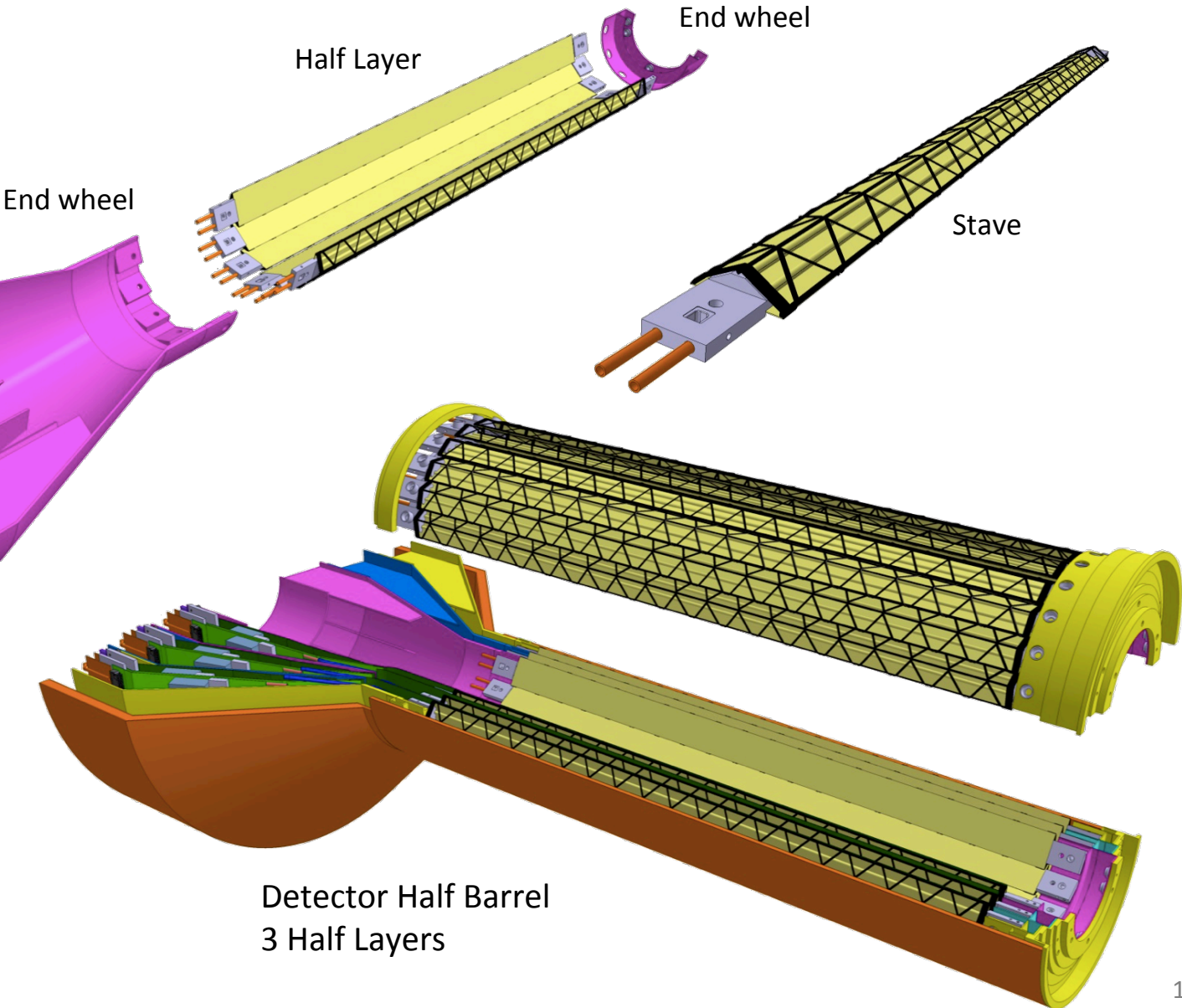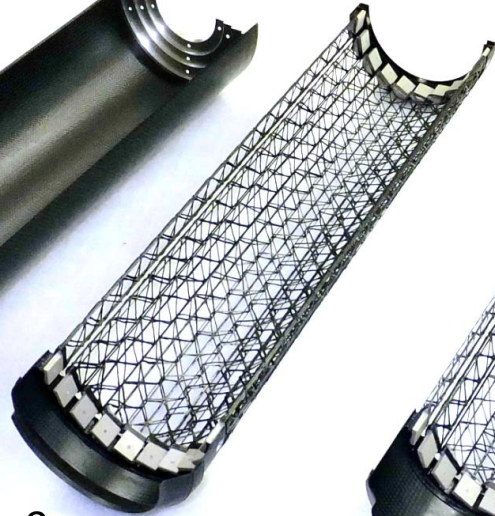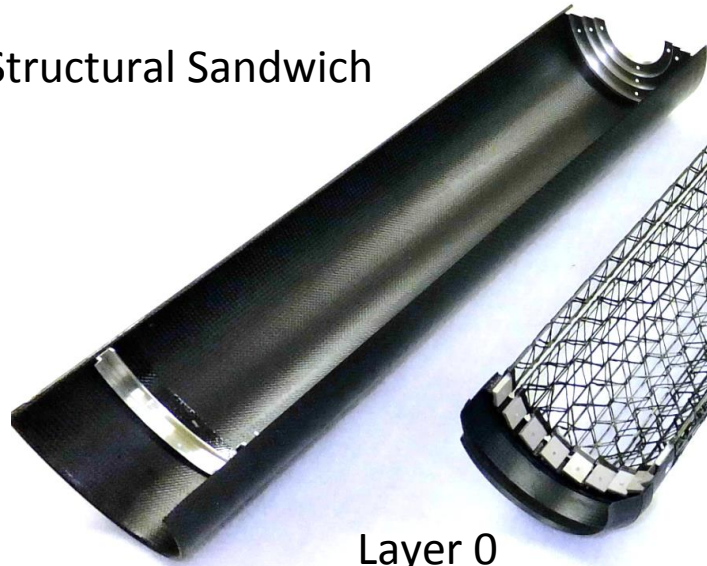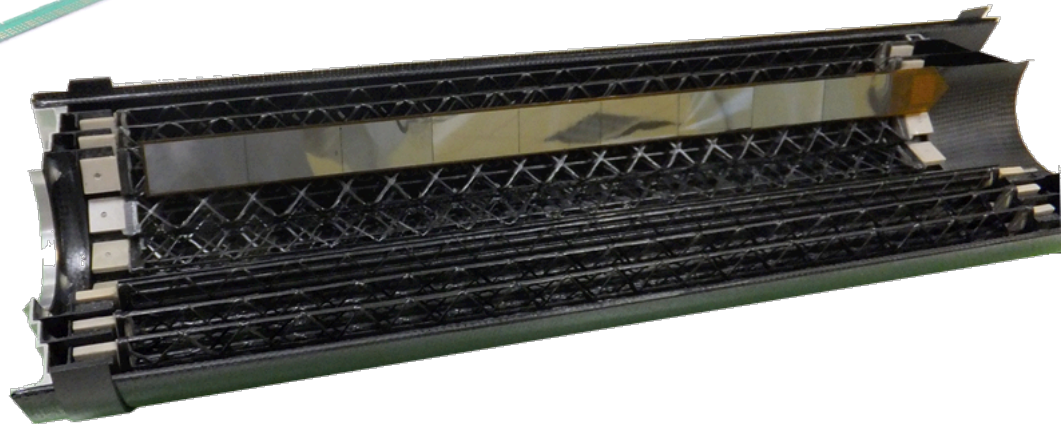
17

Inner Barrel

End wheel

Half Layer

End wheel

Stave

Detector Half Barrel
3 Half Layers

Structural Sandwich

Layer 0

Layer 1

Layer 2

Prototype

ITS Outer Barrel

Power Bus

Flexible PCB

2 x 7 sensors

Cold Plate

Space Frame

Half-Stave **Half-Stave**
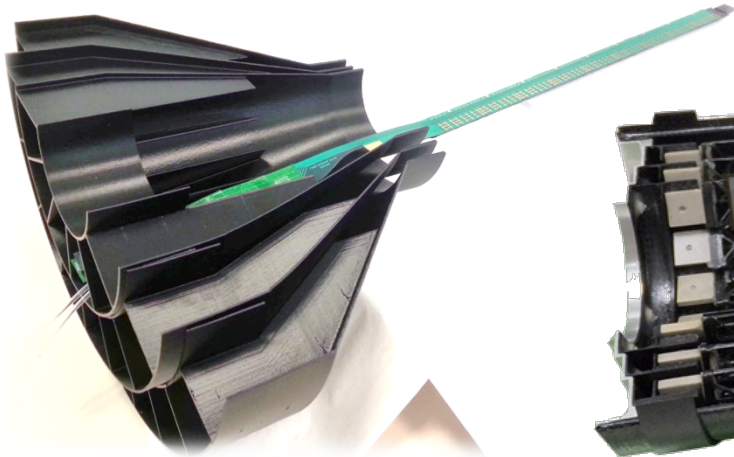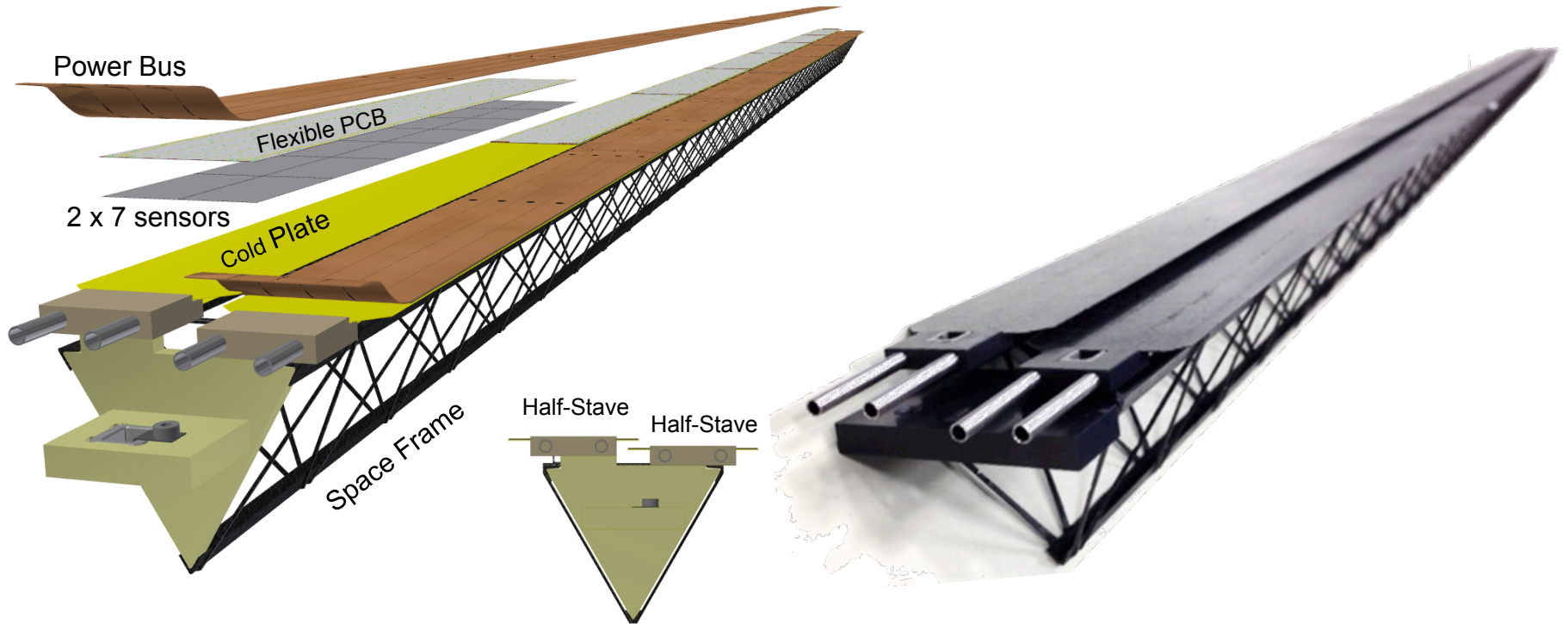
Outer Barrel (OB)

|	
<radius> (mm): 194, 247, 353, 405	Length (mm): 900 (ML), 1500 (OL)
Nr. staves: 24, 30, 42, 48	Nr. modules/stave: 4 (ML), 7 (OL)
Nr. Chips/layer: 6048 (ML), 17740(OL)	Material thickness: ~ 1% X_0
Power density < 100 mW / cm^2	Throughput (@100kHz): < 3Mb/s × cm^{-2}

HIC: Interconnection of pixel chip on flexible printed circuit (FPC)

Bari

FPC side

pixel chip side
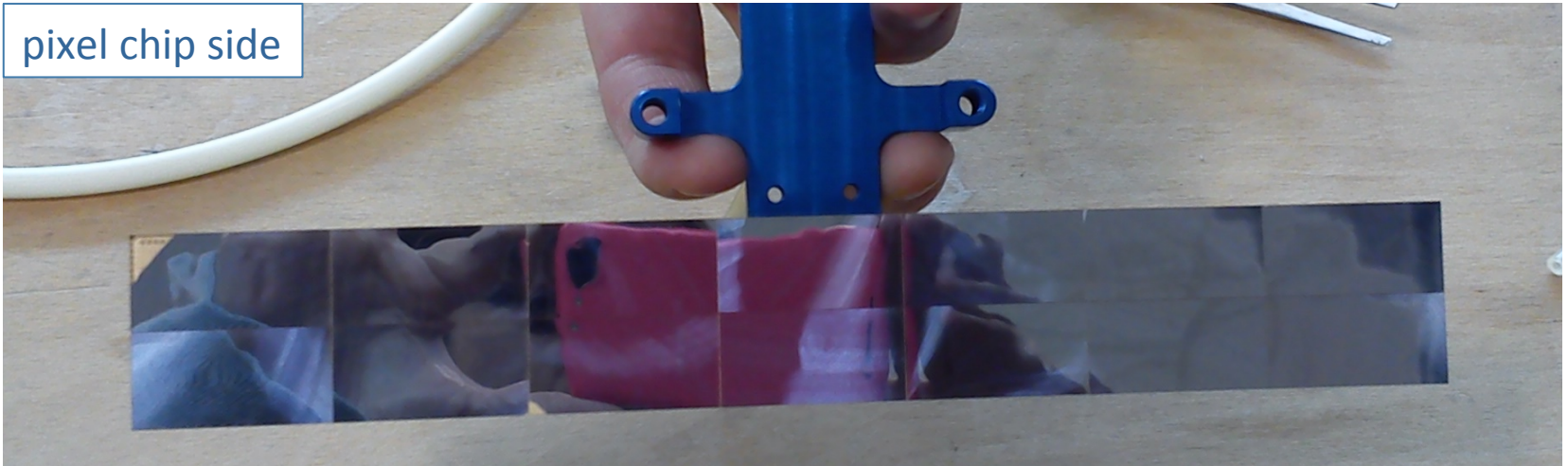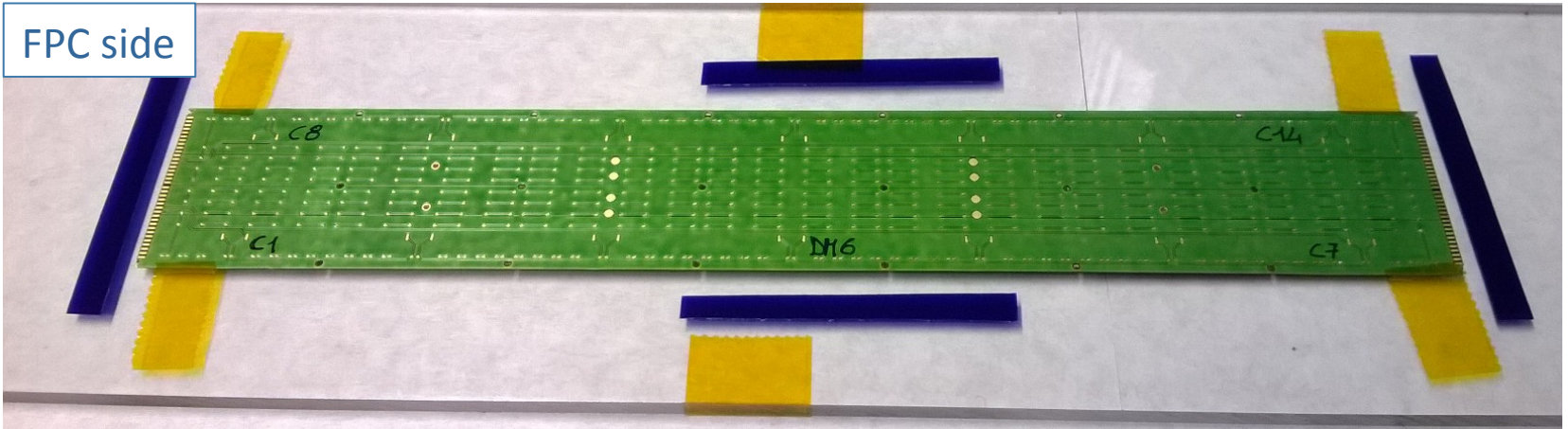
ITS Outer Detector Barrel

Outer Half Barrel
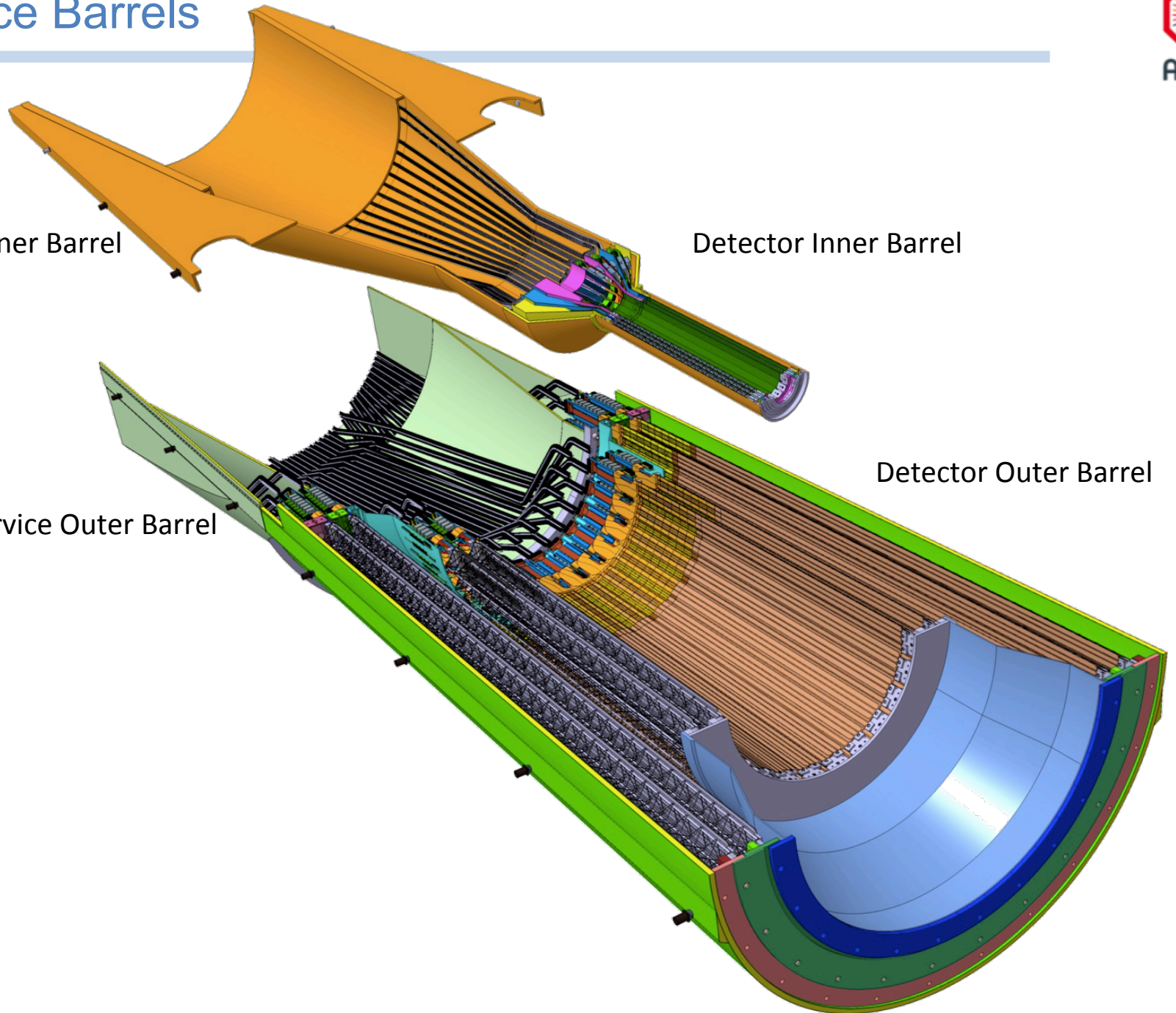
2 Middle Layers

2 Outer Layers

Stave
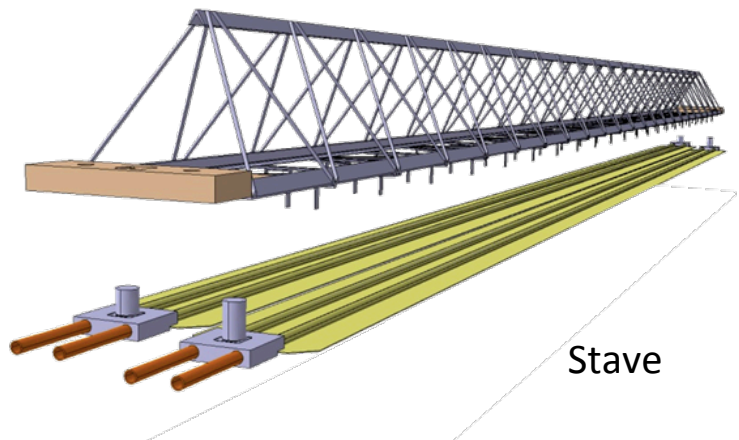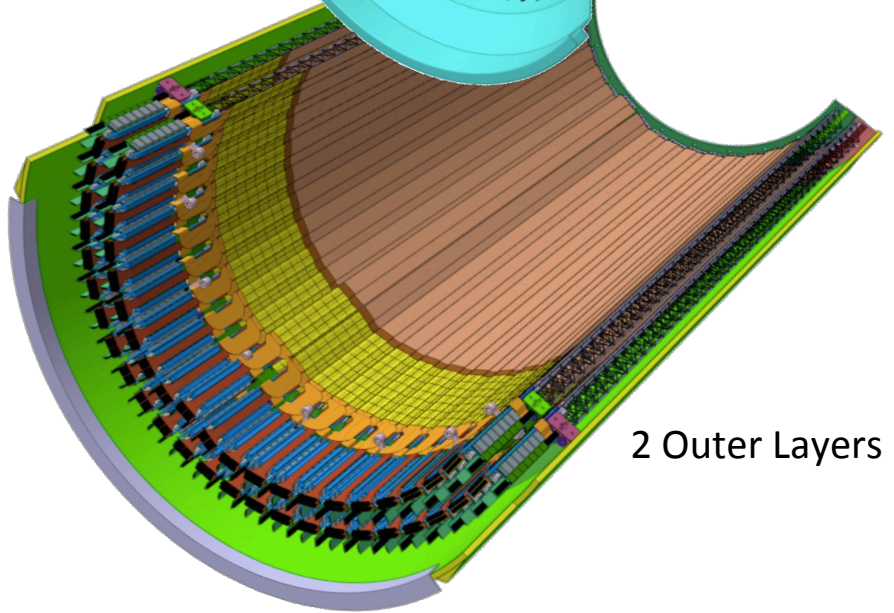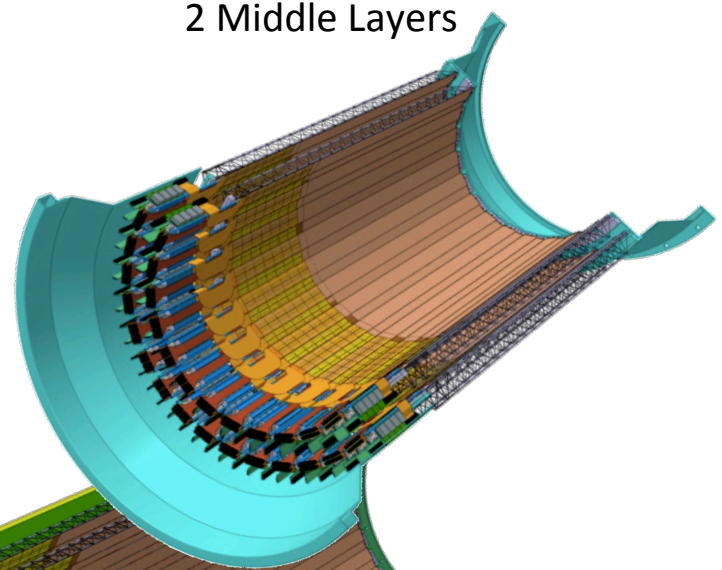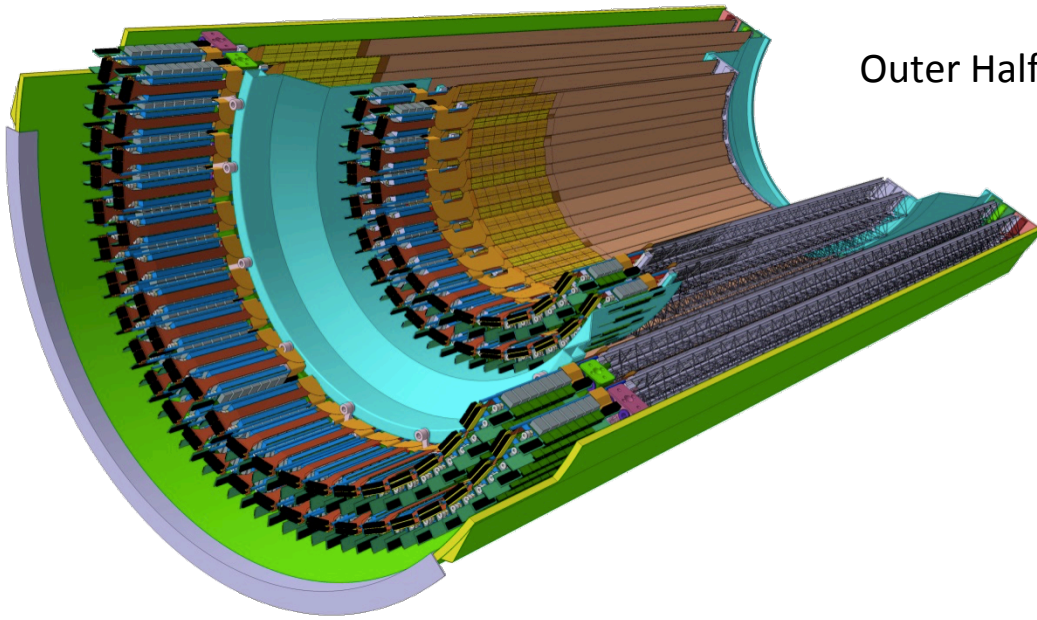
Service Barrels

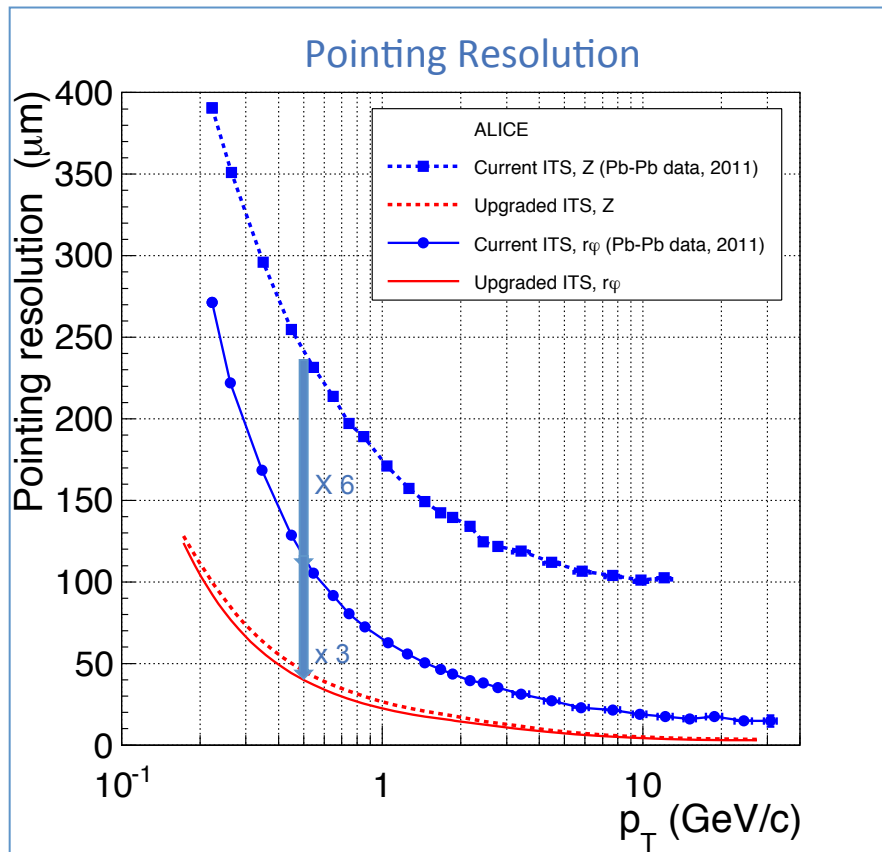Service Inner Barrel

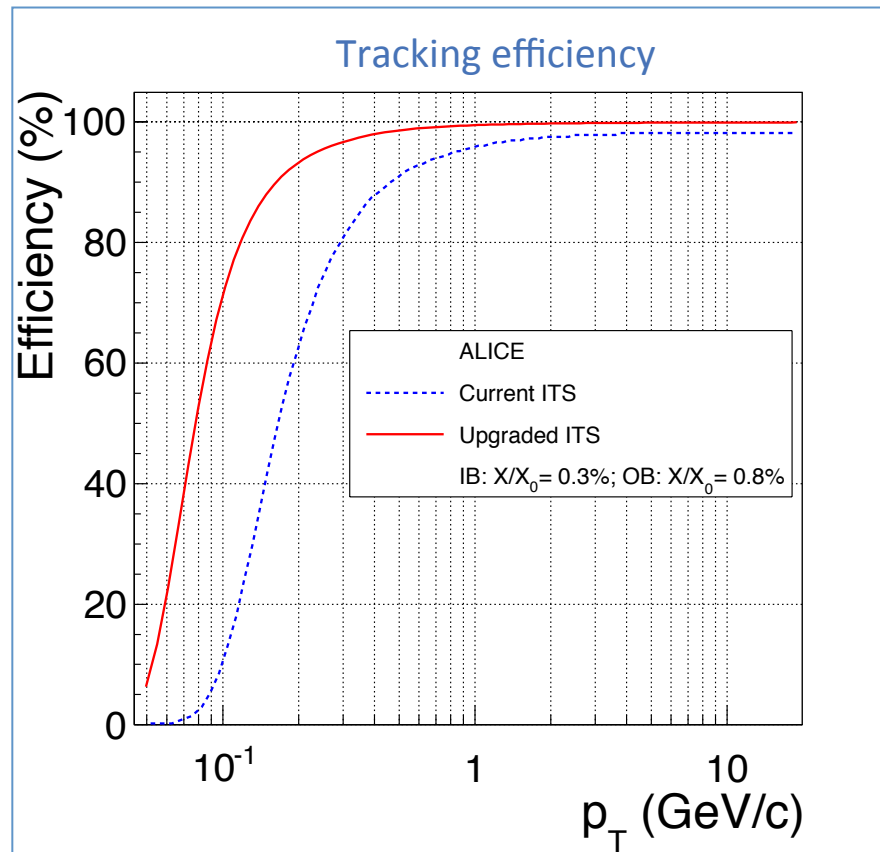Detector Inner Barrel

Service Outer Barrel

Detector Outer Barrel

ALICE

Performance of new ITS (MC simulations)

Impact parameter resolution

Tracking efficiency (ITS standalone)

~40 µm at p_T = 500 MeV/c

Project Timeline and Collaboration

Completion of R &D

Integration, commissioning at surface

High lumi Pb-Pb with upgraded ALICE

2016

2017

2019

2014 2015 2018 2020

Production, construction, tests

Installation in ALICE
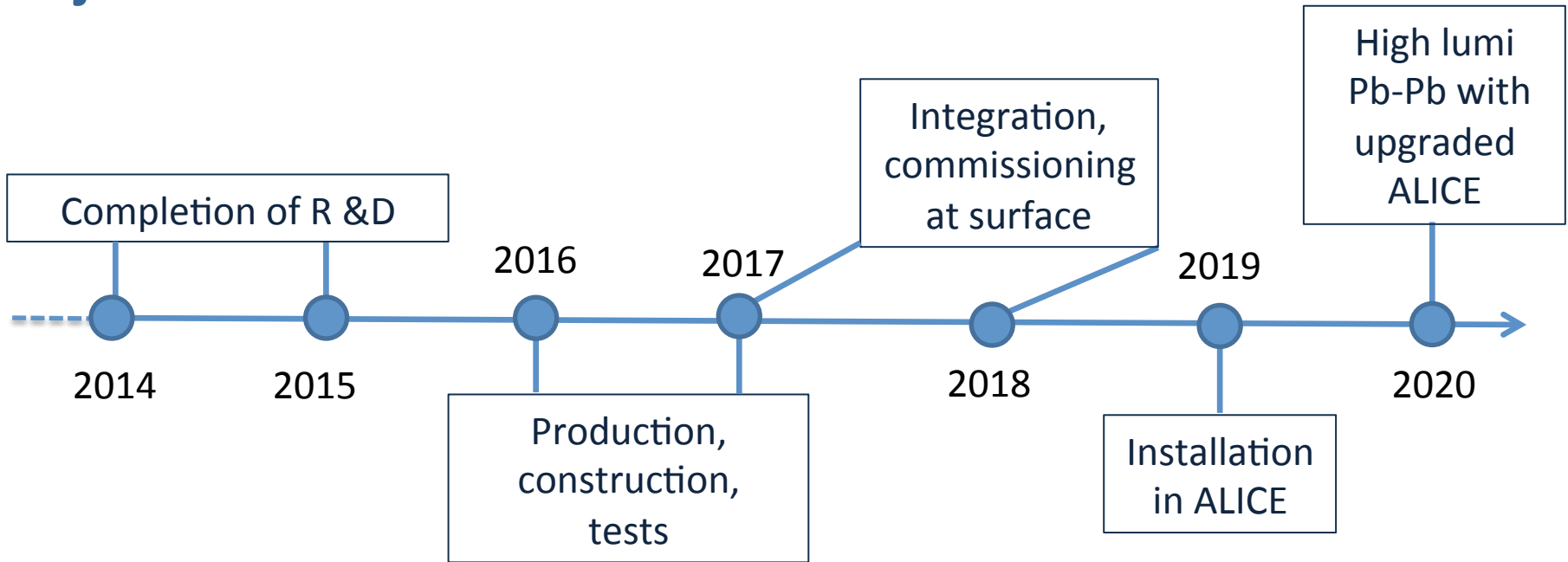
ALICE ITS Collaboration

CERN, China (Wuhan), Check Republic (Prague), France (Grenoble, Strasbourg), Italy (Aless., Bari, Cagliari, Catania, Frascati, Padova, Roma, Trieste, Torino), Indonesia (LIPI), Korea (Pusan, Inha, Yonsei), Netherlands (Nikhef, Utrecht), Pakistan (CIIT-Islamabad), Russia (St. Petersburg), Slovakia (Kosice), Thailand (Suranaree, SLRI, TMEC), UK (Daresbury, Liverpool, RAL), Ukraine (Kharkov), USA (Austin, Berkeley)

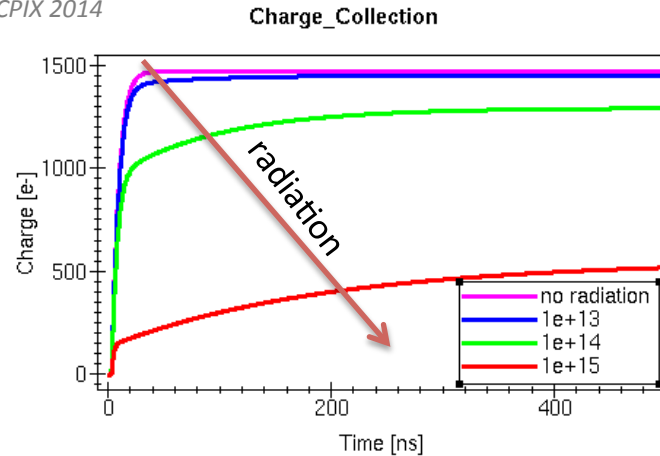Institute = participated in current ITS

SPARES

ITS Pixel Chip – starting material
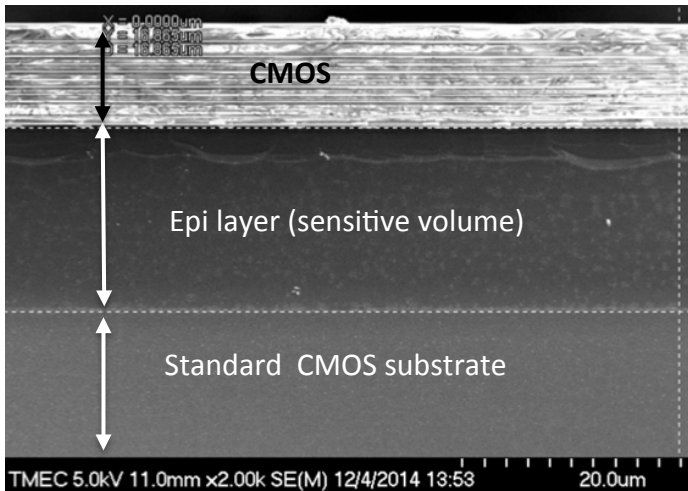
Charge collection time and recombination depend on doping concentration (Si resistivity) and radiation induced dislocations

T. Hemperek (Uni Bonn) – CPIX 2014
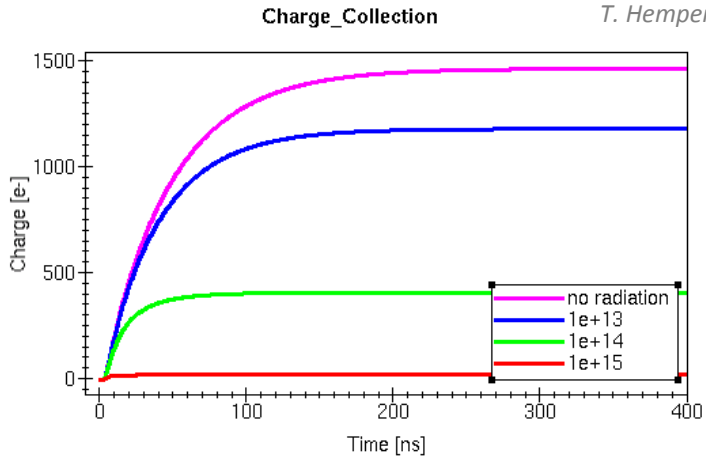
Substrate: 10 Ohm cm, NWELL: @1V PW: @ 0V

Substrate: 2k Ohm cm, NWELL: @1V PW: @ 0V

SEM picture: epi thickness 20μm

ITS Pixel Chip – charge recombination
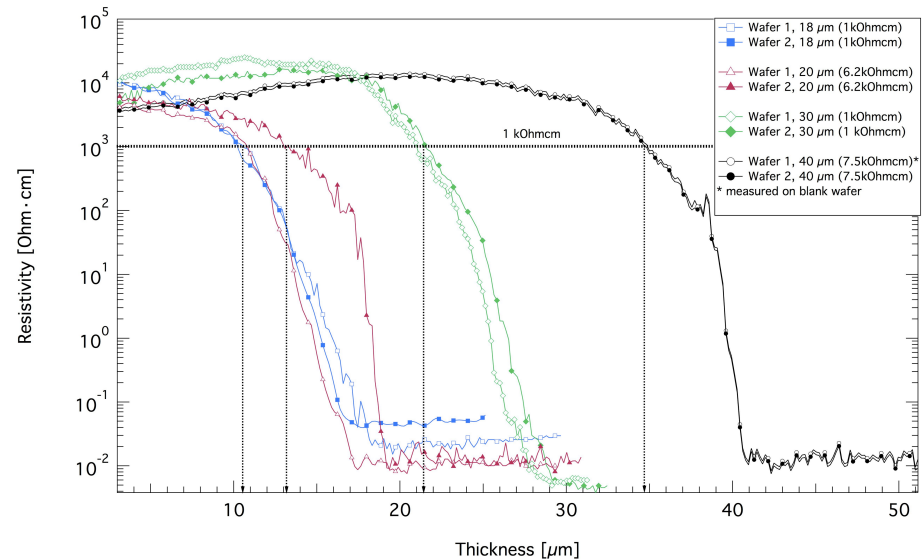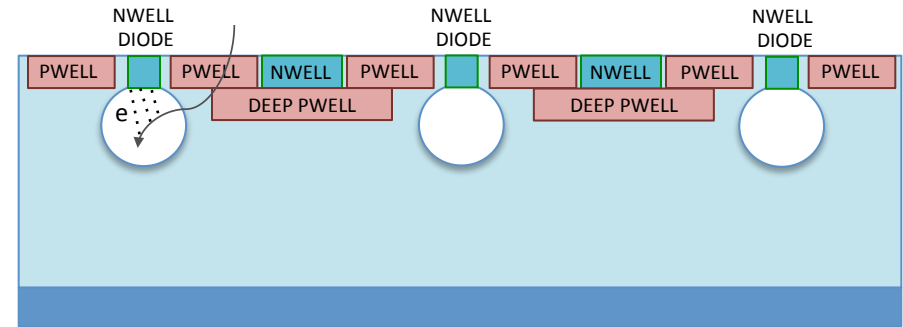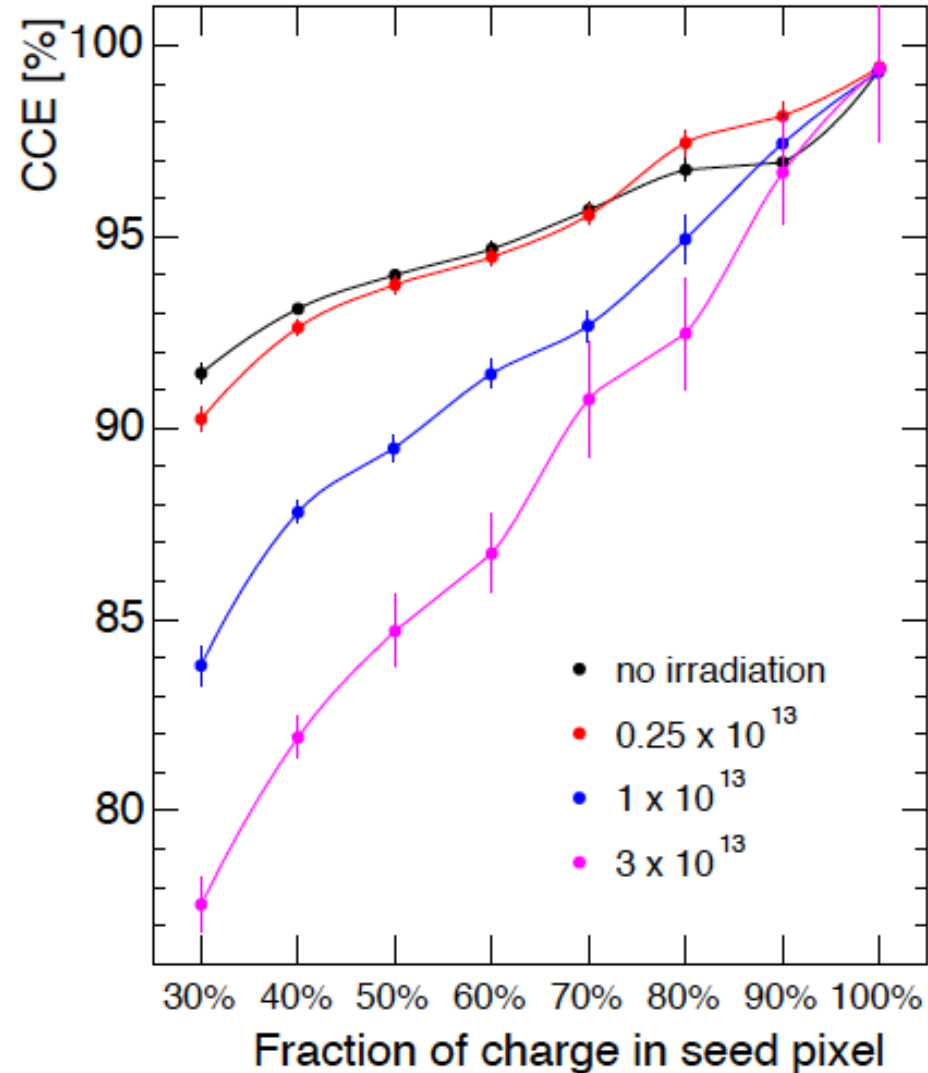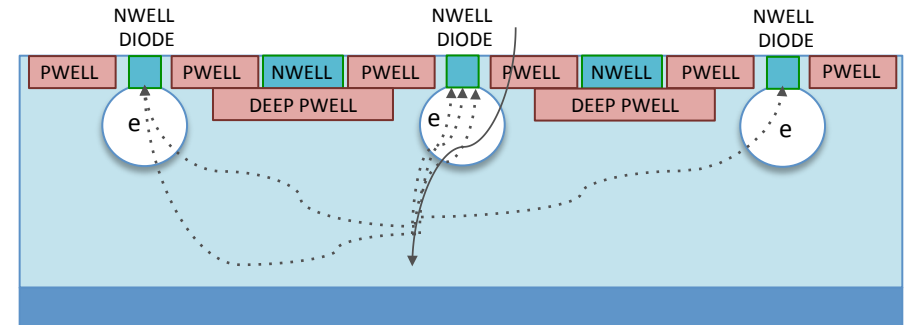

^{55}Fe X-ray absorption close to collection diode
- small diffusion => small recombination
- **Signal collected in a single pixel**

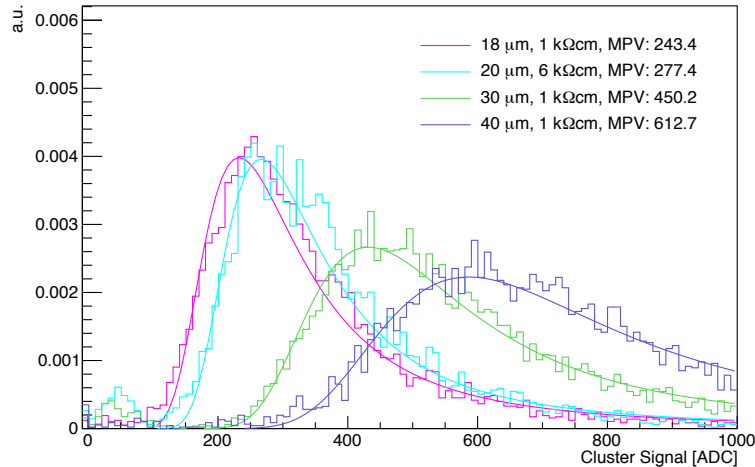^{55}Fe X-ray absorption far from collection diode
- large diffusion => large recombination
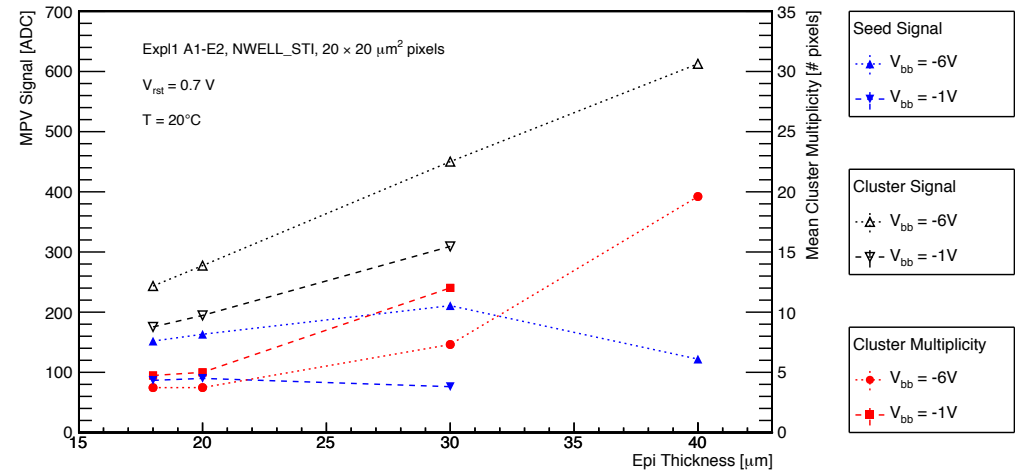- **signal spreads over several pixels**

ITS Pixel Chip – starting material

Thicker epitaxial layers will yield more charge but … diffusion increases cluster size

Cluster Signal (5x5), Explorer-1, A1-E2, Sector 5

- 18 μm, 1 kΩcm, MPV: 243.4
- 20 μm, 6 kΩcm, MPV: 277.4
- 30 μm, 1 kΩcm, MPV: 450.2
- 40 μm, 1 kΩcm, MPV: 612.7

J. Van Hoorne, TIPP2014

J. Phys. G (41) 087002

Expl1 A1-E2, NWELL_STI, 20 × 20 μm² pixels

V_{rst} = 0.7 V

T = 20°C

Seed Signal
- V_{bb} = -6V
- V_{bb} = -1V

Cluster Signal
- V_{bb} = -6V
- V_{bb} = -1V

Cluster Multiplicity
- V_{bb} = -6V
- V_{bb} = -1V

Measurements done at Desy test beam with 3.2 Gev/c positrons

- Cluster charge increases linearly with epi-layer thickness
- Cluster size increases with epi-layer thickness

optimum epi thickness (maximum seed signal) increases by increasing depletion volume
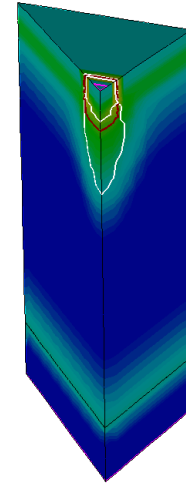
ITS Pixel Chip – starting material

Low input capacitance decisive to achieve large S/N at low power
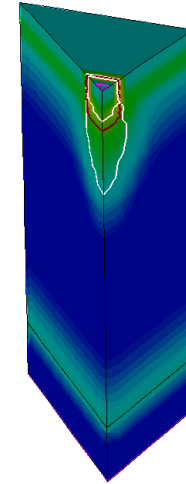
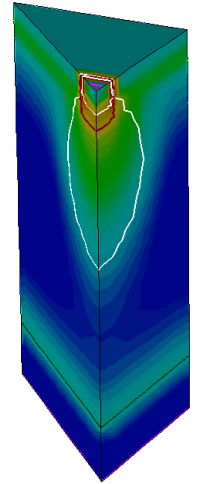*(W. Snoeys, NIMA 731 (2013) 125-130)*
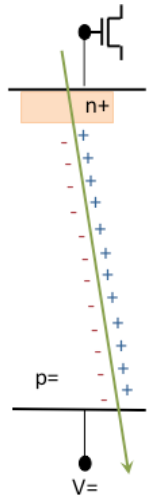
NWELL DIODE output signal = Q /C

- Minimize spread of charge over many pixels

- minimize capacitance:
  - ➡ small diode surface
  - ➡ large depletion volume

-1V, 1x10^{13} cm^{-3} -1V, 1x10^{12} cm^{-3} -6V, 1x10^{12} cm^{-3}

Diode 3μm x 3μm square n-well , White line: boundaries of depletion region

Explorer chip

- HR-18 (> 1 kΩcm)
- HR-20 (6.2 kΩcm)
- HR-30 (1 kΩcm)
- HR-40A (1 kΩcm)
- HR-40B (7.5 kΩcm)
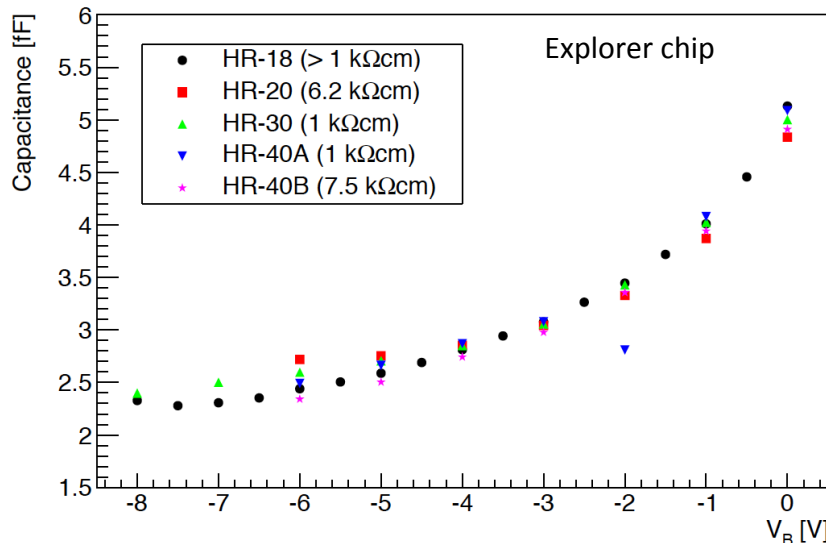
☞ Pixel input capacitance decreases with increasing reverse bias, in agreement with simulated size of depletion region

☞ Minor influence of epi resistivity for current pixel layout

30

Pixel chip – interconnection to flex PCB

Solder Pads

- to solder the chip on the FPC, Al pads need Ni-Au plating (wet-able surface)

- plating is done on wafer using electroless Ni-Au plating, prior to thinning and dicing

- R&D experience 2012-now: plating of about 50 wafers (pad wafers and CMOS wafers)

Status
Market survey concluded
Tendering starting soon

Ni/Au plated pads

ALPIDE-1
(~15 x 30 mm^2)
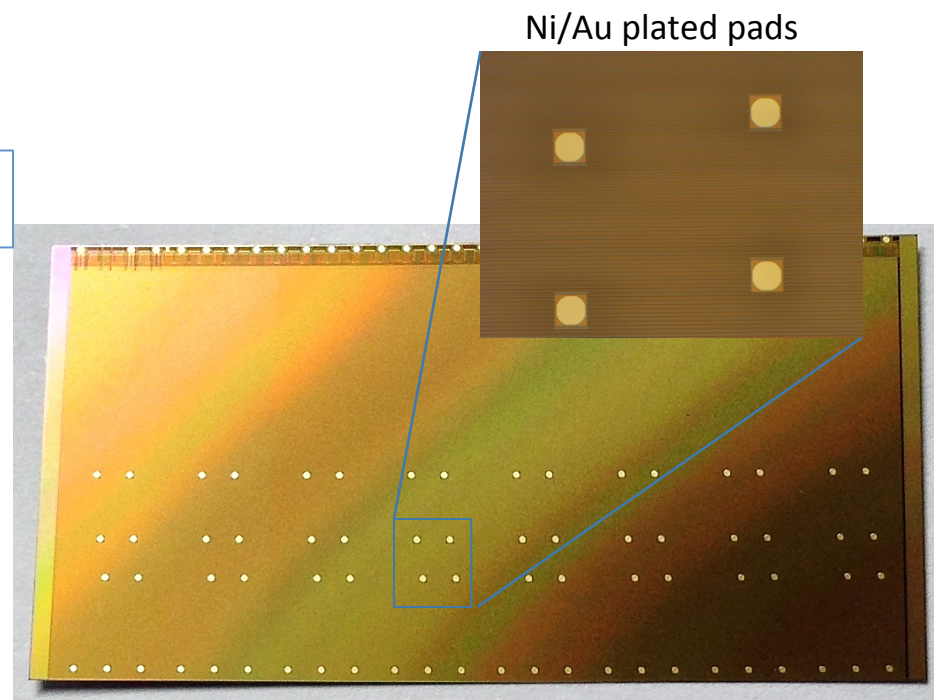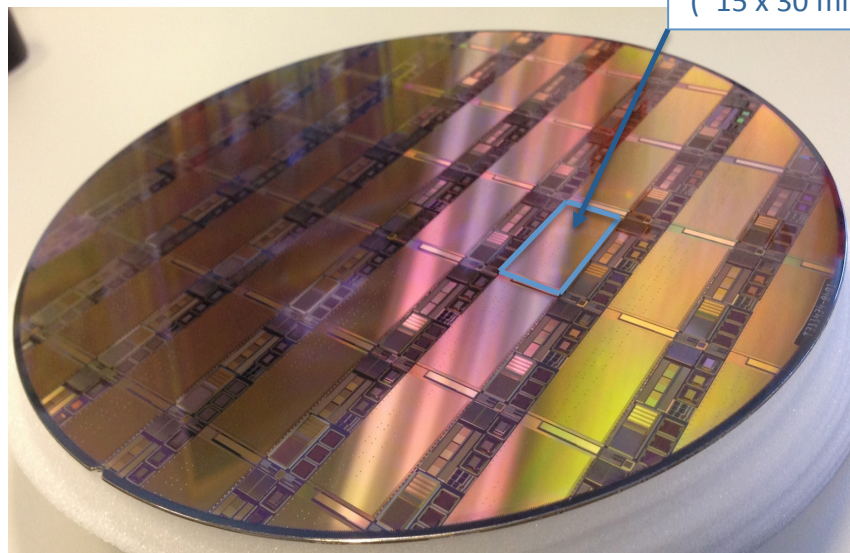
Contact pads are distributed over the matrix
(custom designed)

Pixel chip - thinning & dicing

- Diamond wheel pre-dice before grind (DBG) → extended experience (all types of wafers) with Rockwood (France)

- **Main challenge:** picking of large dies after dicing and grinding (50µm thick chip)
  → **Development of special tools/procedures**

Requirements

- Max. extension from the sealring: 25 µm
- Chipout/cracks contained within 25 µm extension region
- No cracks or chip outs touch the seal ring
- Thickness variation: (50 ± < 5) um

Seal ring

Pixel area
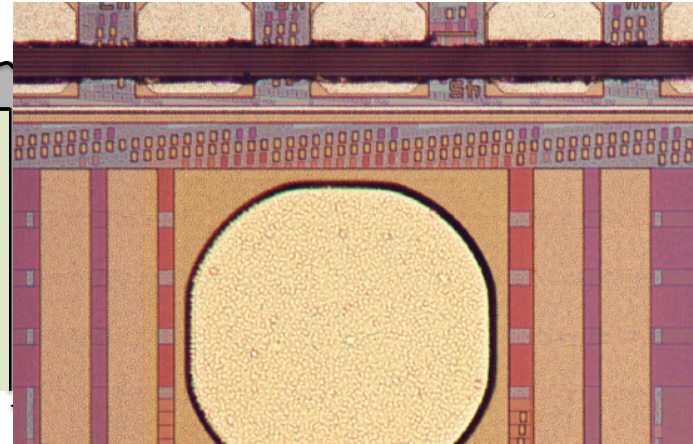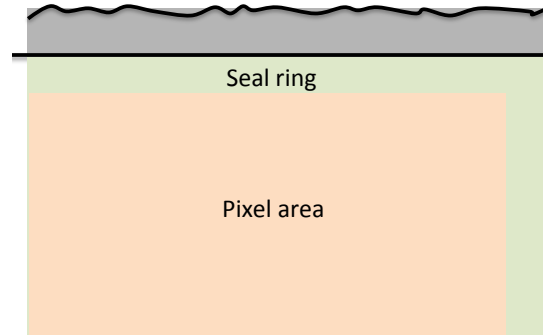
Experience (DBG) **with blanks, pad wafers and fully processed CMOS wafers**

Experience to handle **large dies (pALPIDEfs)**
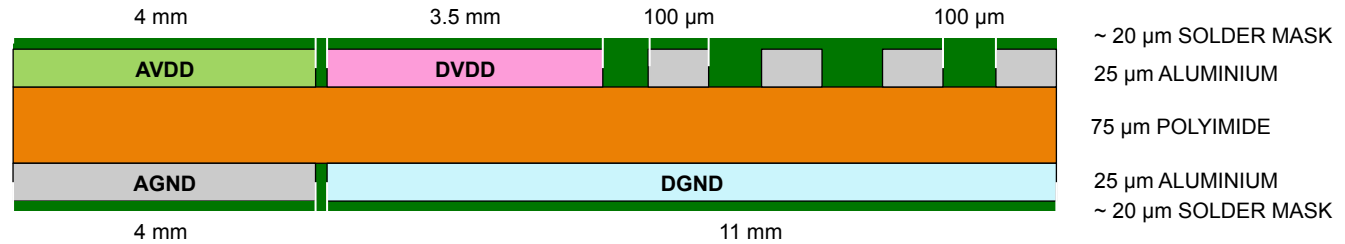
✔ 90 wafers diced and thinned to 50 µm

Status
Market survey in preparation, will be followed by tender in late summer 2015

Inner Barrel Stave – flexible printed circuit

IB Flexible Printed Circuit prototypes (Al power planes and signal tracks)

Metallised vias of
220μm diameter

4 mm	3.5 mm	100 μm	100 μm	
AVDD	DVDD			~ 20 μm SOLDER MASK
				25 μm ALUMINIUM
				75 μm POLYIMIDE
AGND	DGND			25 μm ALUMINIUM
				~ 20 μm SOLDER MASK
4 mm	11 mm			

Status
Two FPC versions (differ for the location of DC-DC converters)
ready to be tested with ALPIDE-2

VERSION (A)

VERSION (B)
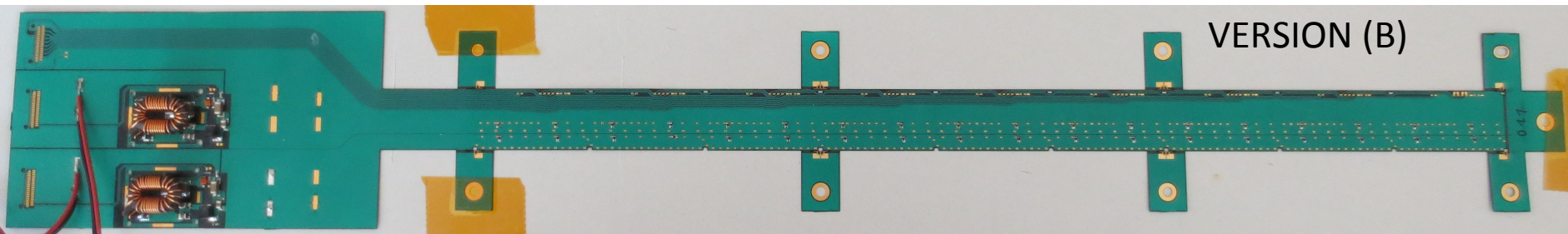
Laser Soldering

- Flux-less soldering of 200 μm diameter Sn/Ag(96.5/3.5) balls (227 ^{o}C melting T) in vacuum (≤10^{-1} mbar)

- IR diode laser, 976 nm, 25 W, 50 mm focal length, 250 μm beam spot size

- Laser power modulated by pyrometer, programmable T profile ensures precise limitation of heating

- Soldering mask (in Macor® or Rubalit ®) used to press FPC on chip and guide soldering balls inside FPC vias

- Solder provides electrical and mechanical connection → no glue
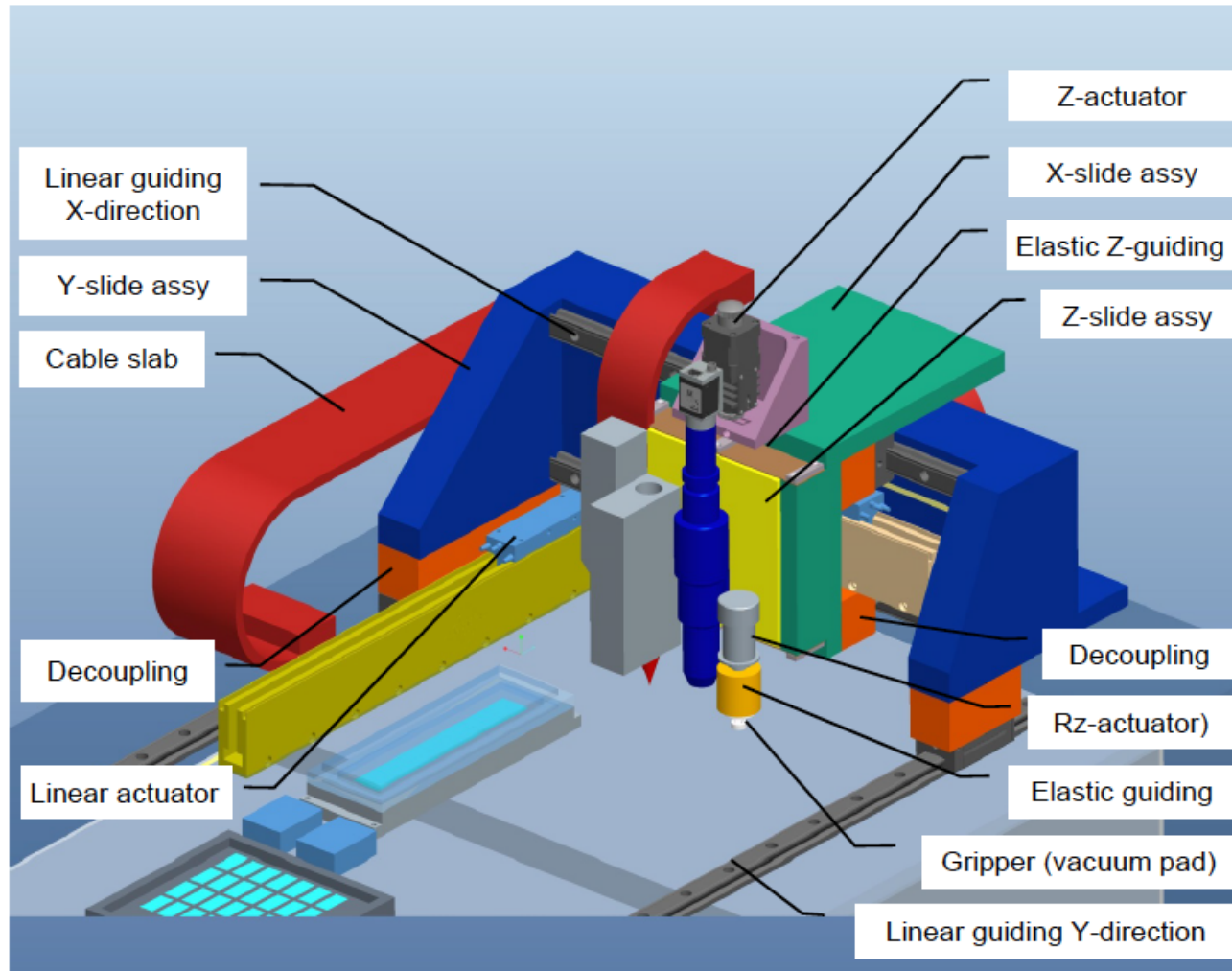

34
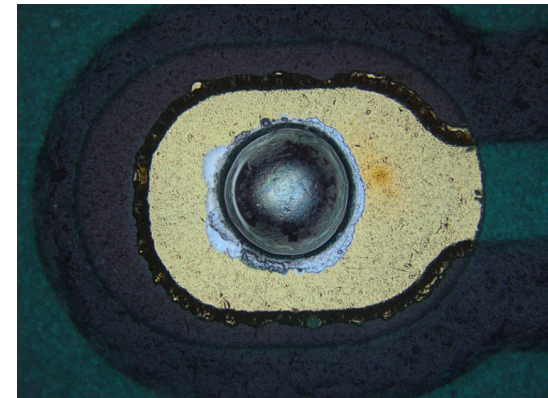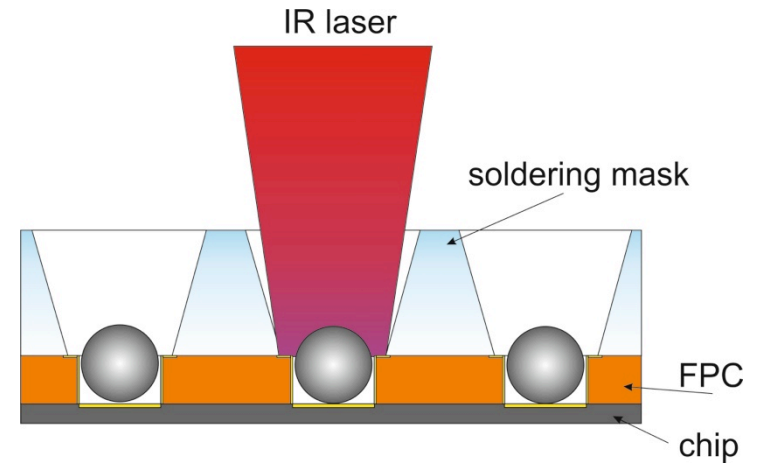
Module Assembly Machine

IB and OB module assembly
- Semi-automatic procedure
- custom machine (specialized company)

Status
- Contract adjudicated to IBS (NL)
- Delivery of first prototype October 15

6 Machines

Inner Barrel & MFT
- CERN

Outer Barrel
- Bari
- Strasbourg
- Liverpool
- Pusan
- Wuhan

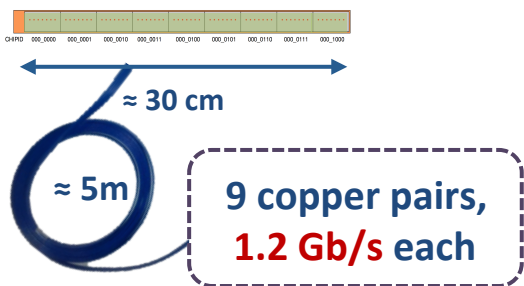#### Same machines used also for chip testing
- CERN
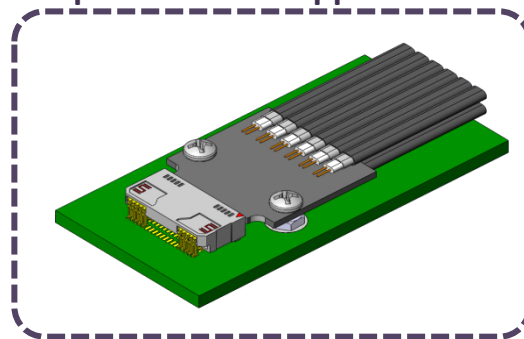- Pusan

Independent machine for chip testing
- Yonsei (Seoul)

Readout Unit – system overview
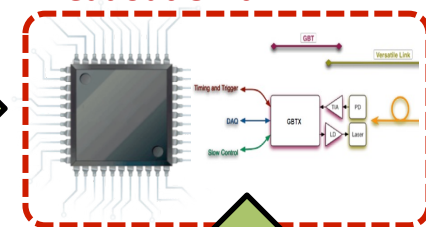
Inner layers (0, 1, 2) staves:
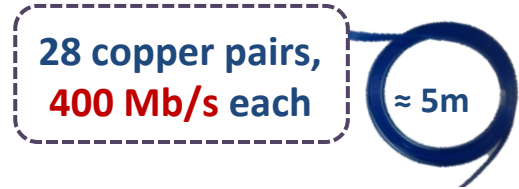9 masters for each stave

12 pairs Twinax copper assembly

Readout Unit
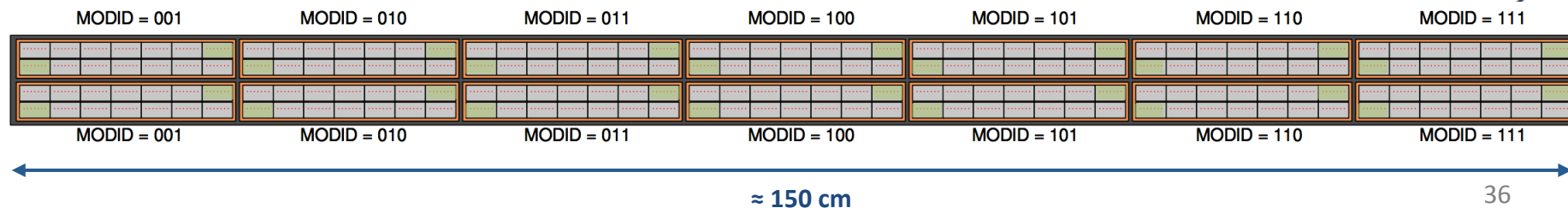
CRU

≈ 30 cm

≈ 5m

9 copper pairs,
1.2 Gb/s each

Mid layers (3, 4) staves: 8 modules per stave, 2 master each

| MODID = 001 | MODID = 010 | MODID = 011 | MODID = 100 |

| MODID = 001 | MODID = 010 | MODID = 011 | MODID = 100 |

16 copper pairs,
400 Mb/s each

≈ 80 cm

≈ 5m

28 copper pairs,
400 Mb/s each

≈ 5m
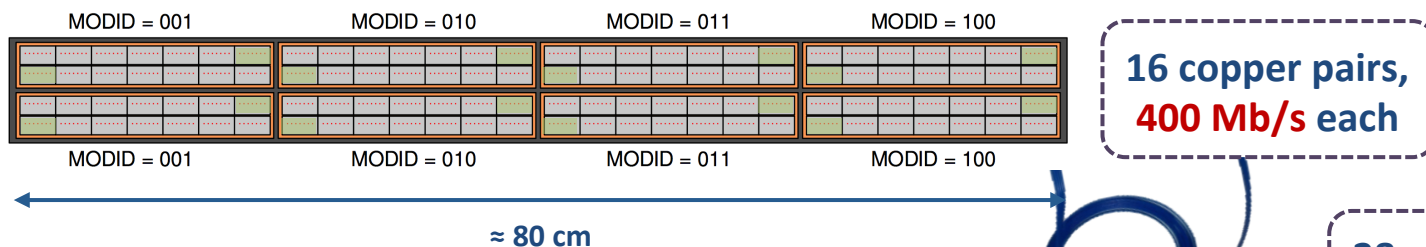
Outer layers (5, 6) staves: 14 modules per stave, 2 master each

| MODID = 001 | MODID = 010 | MODID = 011 | MODID = 100 | MODID = 101 | MODID = 110 | MODID = 111 |

| MODID = 001 | MODID = 010 | MODID = 011 | MODID = 100 | MODID = 101 | MODID = 110 | MODID = 111 |

≈ 150 cm
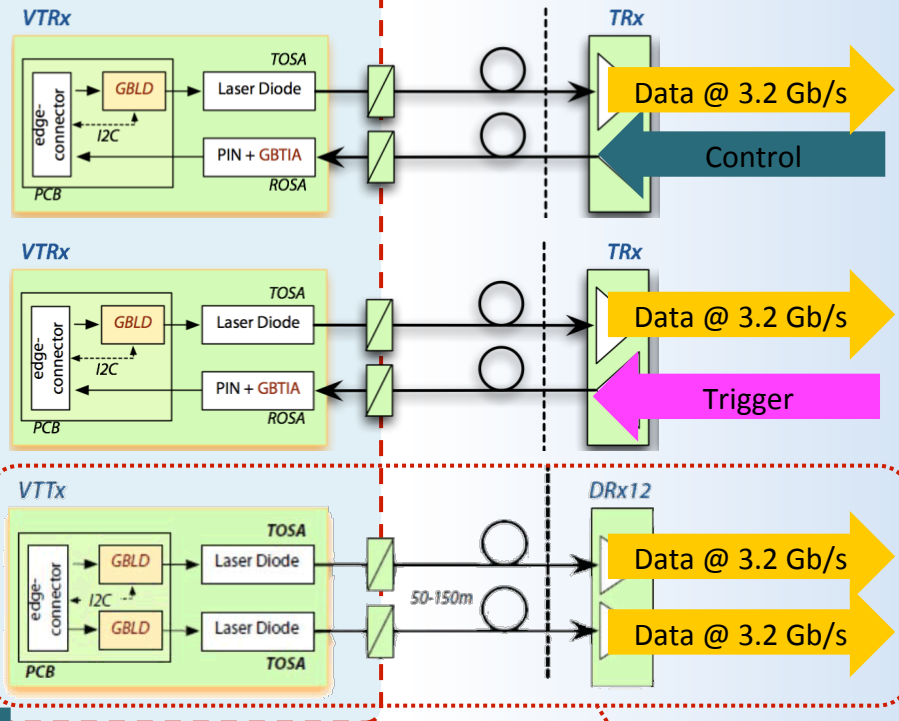
Impact parameter studies (ALICE ITS Upgrade)

(A) radial distance to IP

Legend:
- Current ITS
- L0 at r=3.0cm
- L0 at r=2.6cm
- L0 at r=2.2cm

Axes: R-ϕ Pointing Resolution (μm) vs Transverse Momentum (GeV/c)

(B) Spatial resolution

Legend:
- Current ITS
- L0 with $\sigma_{r\phi,z}$=12μm
- L0 with $\sigma_{r\phi,z}$= 8μm
- L0 with $\sigma_{r\phi,z}$= 4μm

Axes: R-ϕ Pointing Resolution (μm) vs Transverse Momentum (GeV/c)

(C) material budget

Legend:
- Current ITS
- L0 with X/X_0=0.9%
- L0 with X/X_0=0.6%
- L0 with X/X_0=0.3%

Axes: R-ϕ Pointing Resolution (μm) vs Transverse Momentum (GeV/c)

- Current ALICE ITS
  - radial position of first layer: 39mm
  - x/X_0: 1.14% per layer
  - spatial resolution (r-phi): 12 μm

- A) current ITS + L0: x/X0 = 0.3%, res.=4μm;

- B) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

- C) current ITS + L0: r = 22mm, x/X_0 = 0.3%;

ALICE ITS Upgrade CDR, CERN-LHCC-2012-12