Versatile prototyping platform for Data Processing Boards for CBM experiment

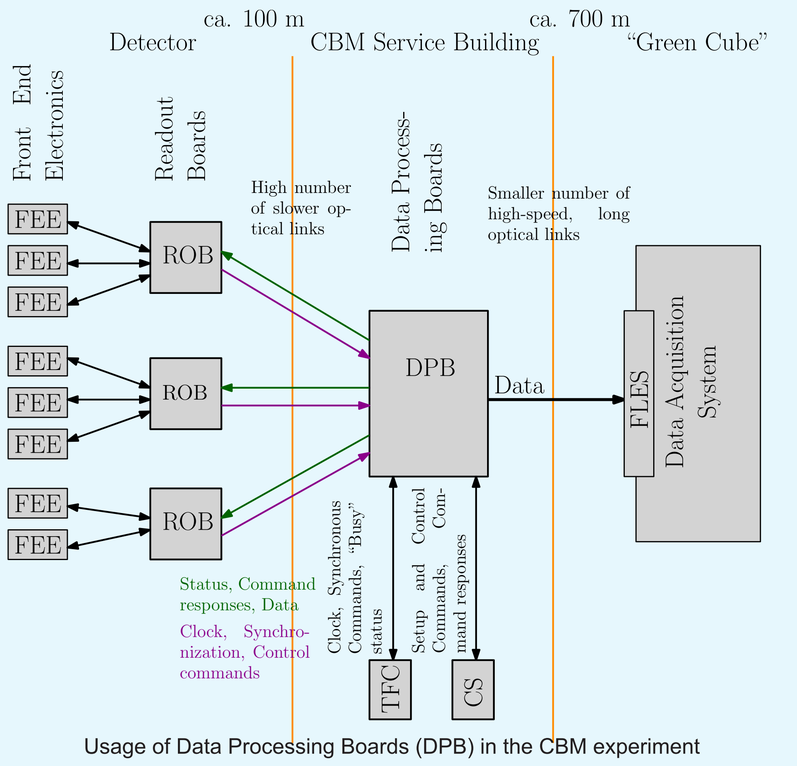
Wojciech M. Zabołotny[1], Grzegorz Kasprowicz[1], Adrian P. Byszuk[1], David Emschermann[2], Marek Gumiński[1], Bartłomiej Juszczyk[1], Jörg Lehnert[2], Walter F.J. Müller[2], Krzysztof Poźniak[1], Ryszard Romaniuk[1]
[1]Institute of Electronic Systems, Warsaw University of Technology, [2]GSI - Helmholtzzentrum fur Schwerionenforschung GmbH

Introduction

The Compressed Baryonic Matter (CBM) experiment is one of the experiments prepared at the FAIR Facility in Darmstadt. Its main aim is the exploration of the QCD phase diagram in the region of high baryon densities during high-energy nucleus-nucleus collisions.
CBM will utilize various detectors equipped with appropriate Front End Electronics (FEE) boards. The important component of the CBM DAQ system necessary to interface the FEE are the Data Processing Boards (DPB) used in three significant applications (see Figure below) [1]

- As the part of the readout chain, they are receiving data from the FEE via multiple short distance and lower speed links. The received data are then preprocessed, concentrated and sent to the First Level Event Selector (FLES) via high-speed long distance links.
- In interaction with the Control System (CS), the DPB boards provide an interface to configure the FEE.
- The DPB boards are connected to the Timing and Fast Control (TFC) system, to ensure transmission of the reference clock and synchronous commands, necessary to synchronize the FEE, and to transmit the flow control related commands and status messages.

Due to relatively high number of DPBs needed in the experiment, it is essential to find optimal (in sense of performance and price) solutions for all described functionalities.
Therefore there was a need to create a versatile hardware platform allowing implementation and verification of possible solutions, and selection of the best ones.



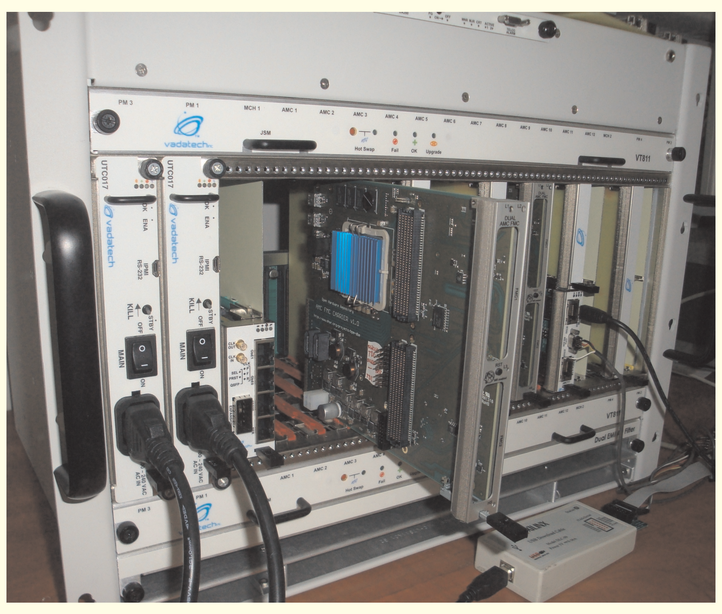
Usage of Data Processing Boards (DPB) in the CBM experiment

Selection of the hardware platform

The DPB boards will be used in the appropriate racks. Therefore an important decision was a choice of the right rack technology.
As a reasonable compromise between the price and offered functions, the MTCA.4 (MicroTCA for Physics) was chosen as the crate technology.
The following MTCA.4 features may be especially useful for DPB prototype implementation:

- Distribution of high-speed low-jitter clock signals between the Advanced Mezzanine Card (AMC) boards
- Broadcasting of signals with up to 100 MHz frequency between the AMC boards via 8 M-LVDS lines
- 1 Gbps Ethernet lines connecting each AMC board with the crate controller (MCH)
- Possibility to connect high speed serial links to the RTM connector

The DPB prototype board is designed as an AMC board, but is equipped with additional functionalities allowing to use it in a stand-alone mode.



The MTCA crate with an AFCK prototype

AFCK board as a proposed prototype

The AMC FMC Carrier Kintex (AFCK) board [1] is designed and published in Open Hardware repository as a versatile prototyping solution for high speed control and data processing applications.
Its resources have been also selected with DPB prototyping in mind:

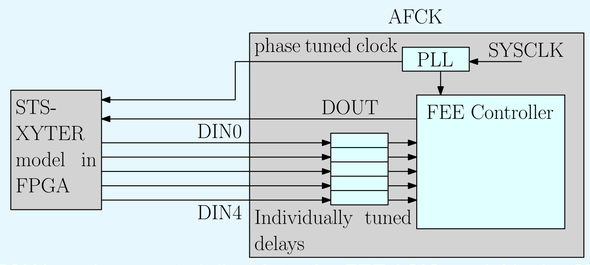
- The board is equipped with a big Kintex-7 325T FFG900 FPGA
- 16 GTX transceivers may be connected to FMC, AMC or RTM connectors by simple resoldering of optional 0201 capacitors (able to operate at data rates between 1 Gbps and 10 Gbps.)

View of the AFCK board

Communication with FEE

AFCK provides different options for communication with FEE boards.

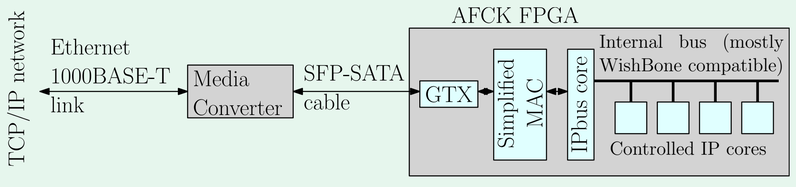
- In most cases there will be an intermediate Readout Board used, equipped with the GBTX ASIC designed in CERN [3]. Communication with GBTX is provided by the dedicated GBT-FPGA core, which has been successfully ported to the AFCK board. The physical link is provided by the GTX transceiver working at 4.8 Gbps bitrate. The links may be routed either to one of the FMC connectors or to the RTM connector, so it is possible to test different optical transceivers without modifying the board itself.
- It is possible to connect the AFCK directly to the FEE Board via a copper LVDS link. This setup has been succesfully tested in STS XYTER protocol tester, prepared in cooperation with AGH University of Science and Technology. In this setup it was necessary to utilize advanced features of the Kintex 7 family, like precise adjustment of delay in input blocks and precise adjustment of clock phase in PLL blocks [4].



The AFCK board connected directly to the FEE ASIC model in the STS-XYTER tester

Communication with the Control System (CS)

Communication with the CS will be provided by the IPbus protocol using the 1 Gbps Ethernet link. In the AFCK board it is possible to configure GTX transceiver to operate in appropriate mode. The IPbus IP core has been successfully ported to AFCK. When used in the MTCA crate, the dedicated AMC port may be used to provide Ethernet connection via MCH controller. In the stand-alone mode it is possible to use the SFP-Ethernet adapter together with SFP equipped FMC board. Another solution for stand-alone operation is usage of SATA connector with SATA-SFP cable and media converter (e.g. TP-Link MC220L).



The AFCK board connected to the TCP/IP network using IPbus protocol. The board works in stand-alone mode and is connected via SATA connector.

Communication with the TFC system

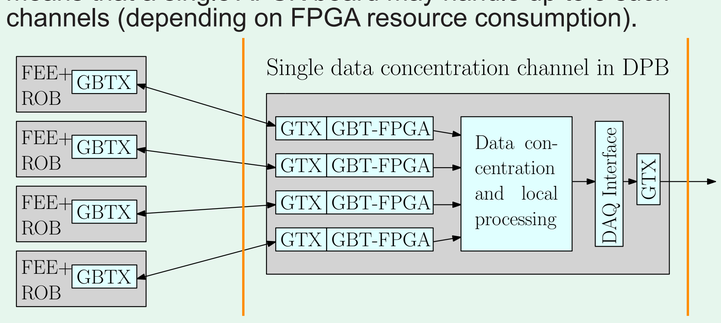
Important function of the DPB board is communication with the Timng and Fast Control system.
The AFCK is able to implement the White Rabbit system, which may be used to transmit precise timing and synchronization messages. Correct operation of the White Rabbit core has been successfully proven in the hardware.
In the final setup it is possible, that only one board in a crate will be used as a TFC receiver/transmitter. In this case the MTCA TCLKA and TCLKB lines may be used to transmit the reference clock and PPS, while M-LVDS lines may be used to transmit busy status and synchronous commands.

Data processing capabilities

The XC7K325T FFG900 FPGA is a relatively big chip, offering significant amount of logic resources (326080 logic cells), DSP blocks (840 DSP slices) and internal block memories (890 18k BRAMs). Therefore after implementation of other necessary subsystems, there will be enough free resources for data processing. Additionally the board is equipped with 2GB of DDR3 SDRAM connected via 32-bit interface, working with 800 MHz clock.
That memory may be used e.g. to store processed data or results, or to buffer data to be transmitted to DAQ.

Data concentration

The AFCK board offers 16 GTX transceivers, grouped into 4 quads. One of the GTX will be used by the IPbus Ethernet interface, so there are 15 GTX blocks available for communication with FEE and transmission of data to DAQ.
For example if a single data concentration channel may aggregate data from four FEE links and send them to a single DAQ link, it means that a single AFCK board may handle up to 3 such channels (depending on FPGA resource consumption).



Concentration of data in a single channel in AFCK

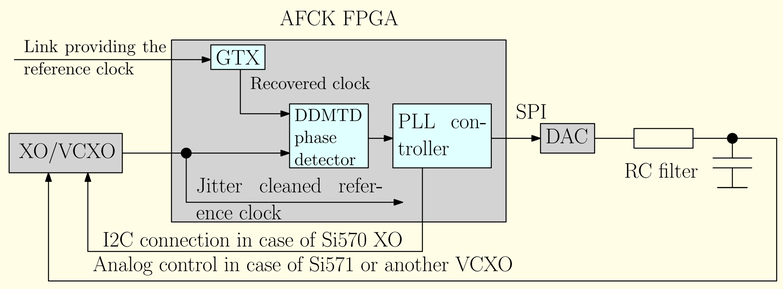
Communication with DAQ

The AFCK board is able to transfer data to DAQ at 10 Gbps bit rate. The preferred solution is to use the FMC card equipped with appropriate SFP+ cages and SFP+ optical transceiver.
The data may be transferred to the dedicated FLIB board, using the special "FLES Interface Module" (FLIM) developed at FIAS [5].
Another possibility is to use a specially developed FADE protocol [6], allowing to transmit data directly to a standard 10 Gbps Ethernet card in a computer system.
For development and testing purposes it is possible to use low bandwidth DAQ connection via IPbus (together with ECS connection) [7].

Flexible clocking

The GBT-FPGA core and the White Rabbit core intensively use the flexible clocking features of the AFCK board.
The AFCK board offers flexible possibilities of configuration of on-board clocks.

- Two crystal based generators (25MHz - used by WR system and 20MHz), which may be slightly tuned using the voltage produced by SPI controlled DAC.
- Programmable Si570 XO produced by Silabs. Except of setting of nominal frequency in broad range, it can be also precisely tuned via I2C (may be replaced with Si571, precisely tuned via SPI controlled DAC). Those tunable generators may be used to create software or firmware controlled PLL based on FPGA implemented DDMTD phase detector. These allow recovery of high quality, jitter-cleaned clock, which may be used to drive GTX transmitters.
- Configurable clock matrix with 16 inputs and 16 outputs



Clock recovery and jitter cleaning features of AFCK

Conclusions

Due to its flexibility and reach resources, the AFCK board may be a good prototyping platform for data concentration and FEE control systems in different experiments.
Its possibility to work both in crate and in stand-alone configurations makes it suitable for development of simple systems (e.g. during test beams) and for integration tests.

References

[1] W.M. Zabołotny, G. Kasprowicz: "Data processing boards design for CBM experiment", Proc. SPIE. 9290, pp. 929023. (November 25, 2014) doi: 10.1117/12.2073377
[2] "AMC FMC Carrier Kintex (AFCK)", http://www.ohwr.org/projects/afck
[3] M. Barros Marin et al.: "The GBT-FPGA core: features and challenges", JINST 10 (2015) 03, C03021
[4] CBM Progress report 2014; https://www-alt.gsi.de/documents/DOC-2015-Apr-43-1.pdf
[5] D.Hutter et al.: "FLES Input Interface", http://tinyurl.com/fles-input-interface
[6] W.M. Zabołotny: "Low latency protocol for transmission of measurement data from FPGA to Linux computer via 10 Gbps Ethernet link", JINST 10 (2015) T07005
[7] P.A. Loizeau, D. Emscherman et al.: "The prototype readout chain for CBM using the AFCK board and its software components ", Proc. SPIE 9662, pp. 96622X (September 11, 2015); doi:10.1117/12.2205820