<TWEPP 2015>

Front end Optimization for the Monolithic Active Pixel Sensor of the ALICE Inner Tracking System Upgrade

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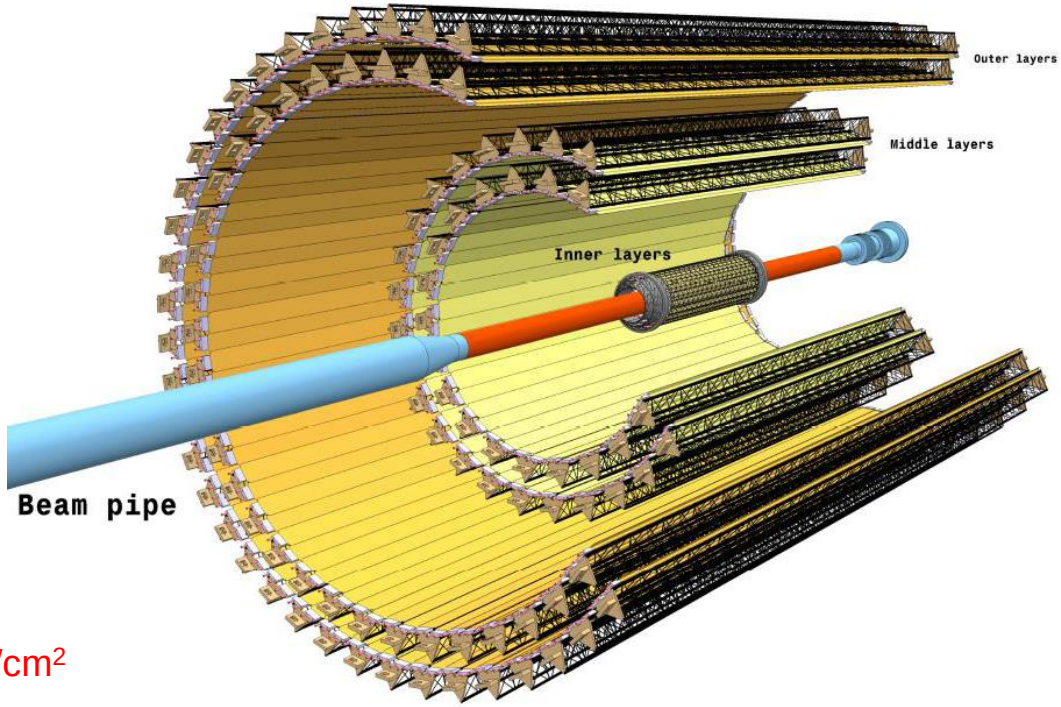
I. Introduction
- ALICE ITS upgrade project

The ALICE ITS will be replaced with an entirely new detector during LS2 (2019)



New Layout for improved resolution

- 7 layers, 12.5 Gpixels in ~ 10 m^2
- Inner layer radius 22 mm
- X/X_0 0.3 % (innermost layers)
- Spatial resolution ~ 5 μm

Requirements

- Chip: 15 mm x 30 mm x 50 μm
- Pixel size: O(30x30) μm^2
- Power density < 100 mW/cm^2
- Integration time < 30 μs
- Required radiation tolerance : TID 2.7 Mrad & NIEL $1.7 \cdot 10^{13}$ 1 MeV n_{eq}/cm^2

Thin sensors, high granularity, large area, moderate radiation

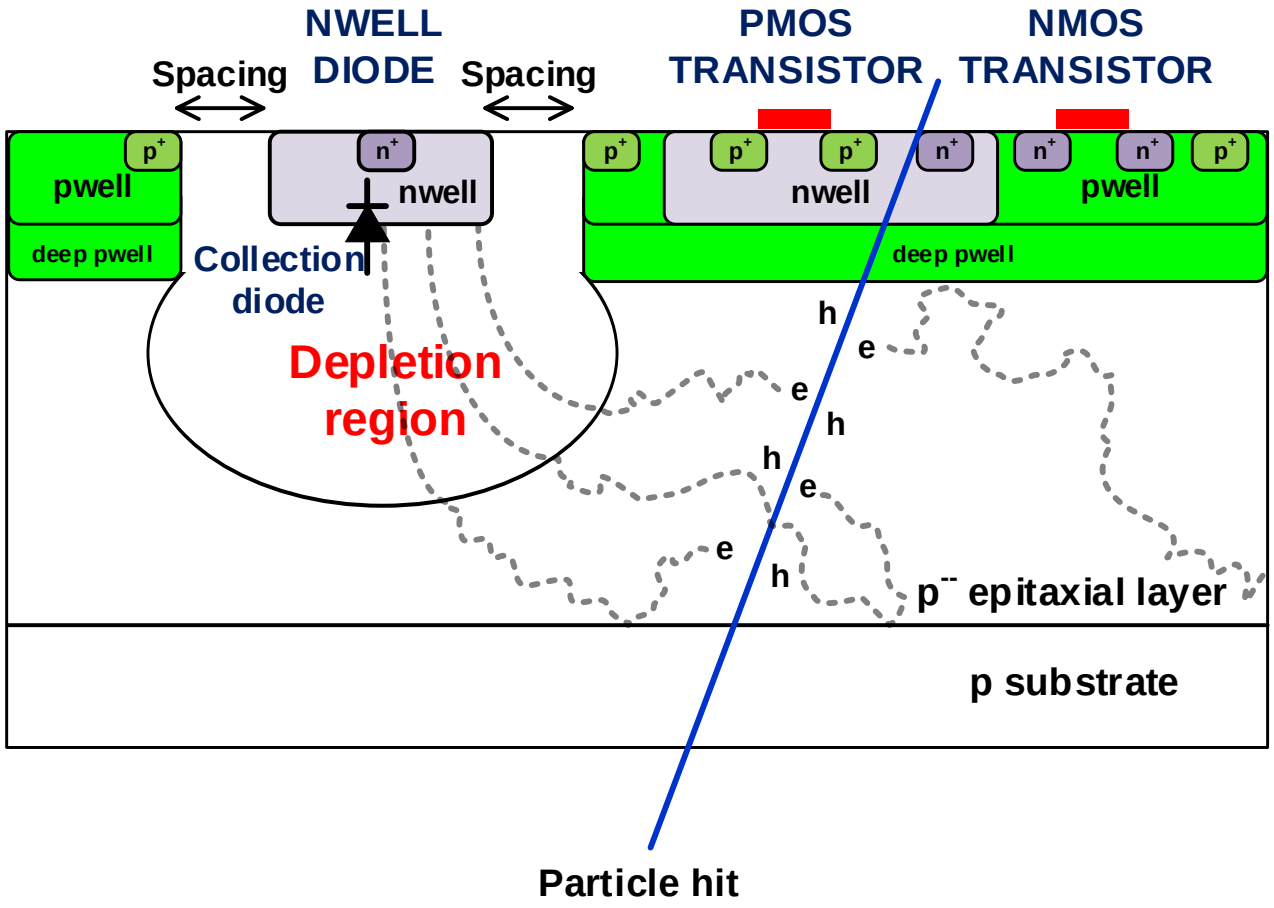
➔ Monolithic silicon pixel sensors

See L. Musa Thursday h.14 plenary talk

I. Introduction
- Technology

TowerJazz 180 nm CMOS imaging process

- Gate oxide 3 nm thick, good for TID tolerance



Deep Pwell

- Allows in pixel PMOS

Epitaxial layer

- Thickness: 18 – 40 μm
- High resistivity: 1 – 8 kΩ·cm

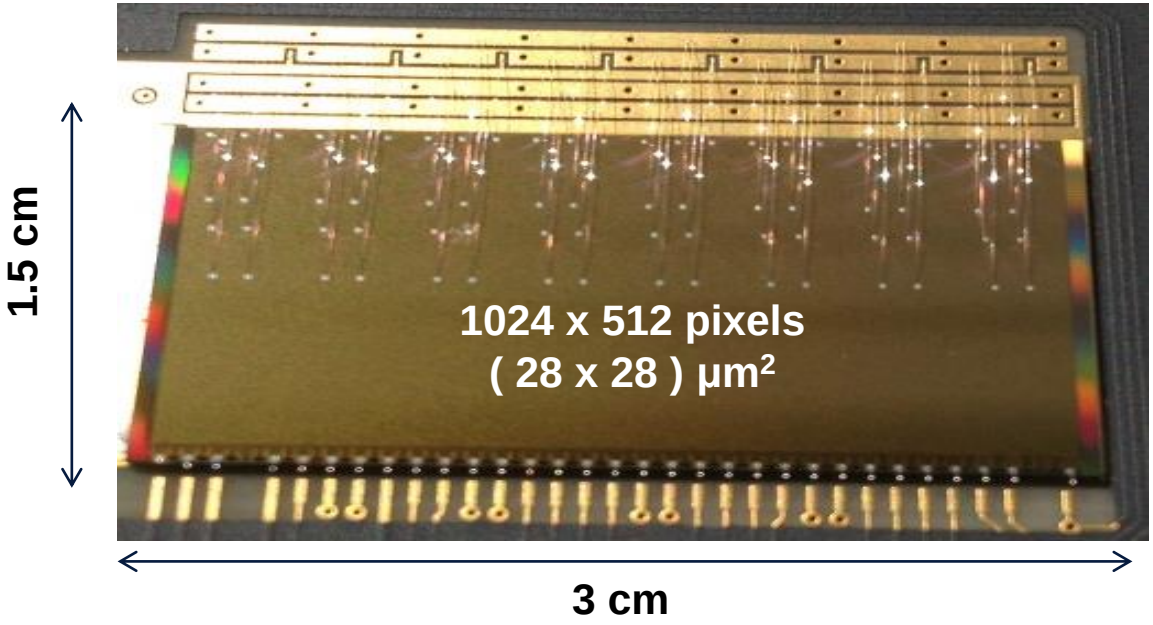
Reverse substrate bias

- Increases Depletion region
- Reduces collection diode capacitance

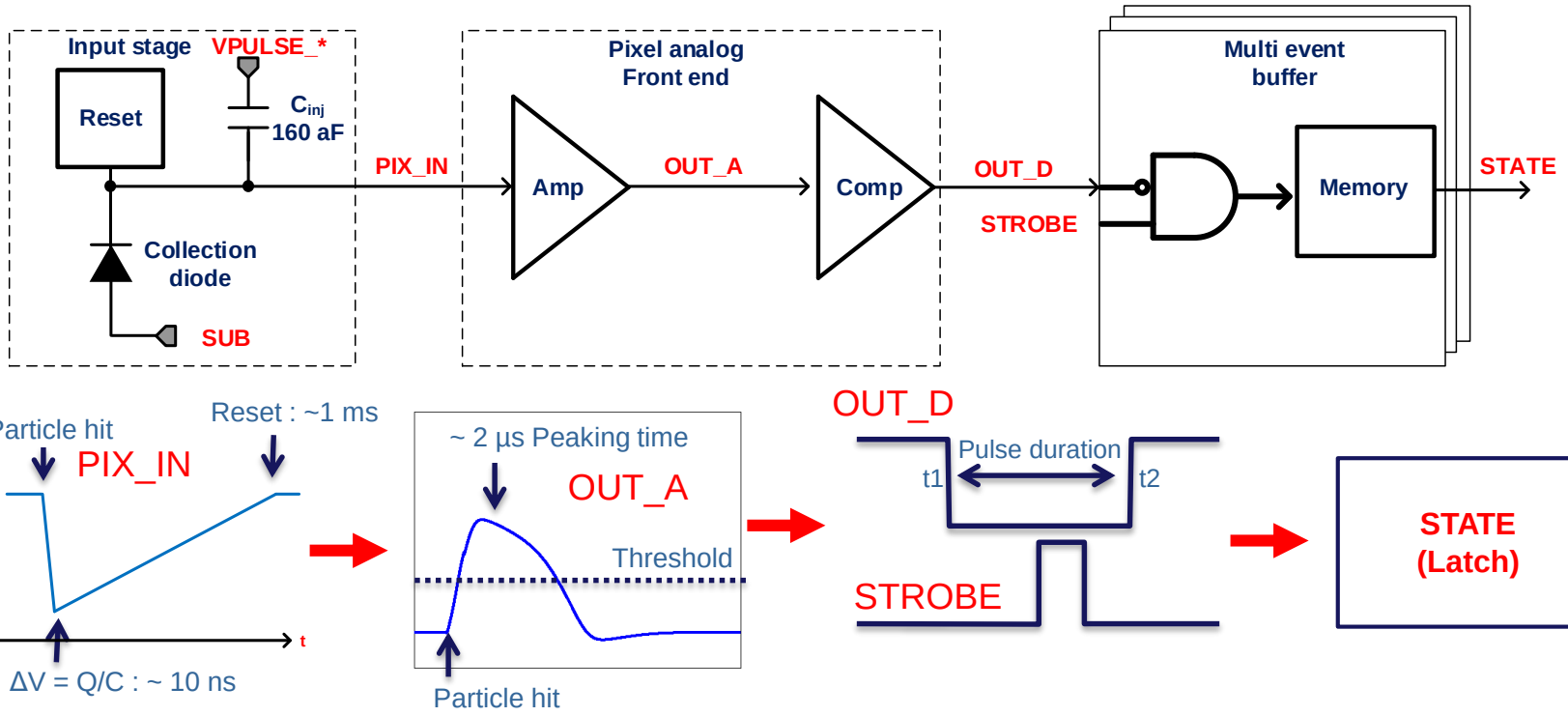
I. Introduction
- Chip development

- Since end 2011, 4 MPWs and 5 engineering runs.
- Small scale prototypes for sensor optimization
- Full scale ALPIDE prototypes (1024 x 512 pixels)
  - ALPIDE-1&2 (lab and beam test)
  - ALPIDE-3 (coming back from foundry in October 2015)
    - Front end optimization and revision from ALPIDE-1&2

< The first full scale prototype : ALPIDE-1 >



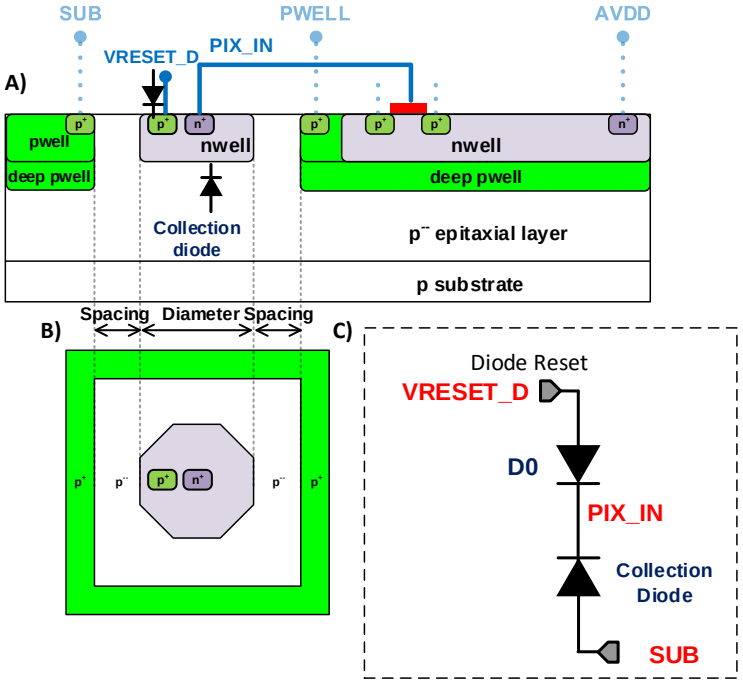
2. ALPIDE principle of operation
- In-pixel hit discrimination



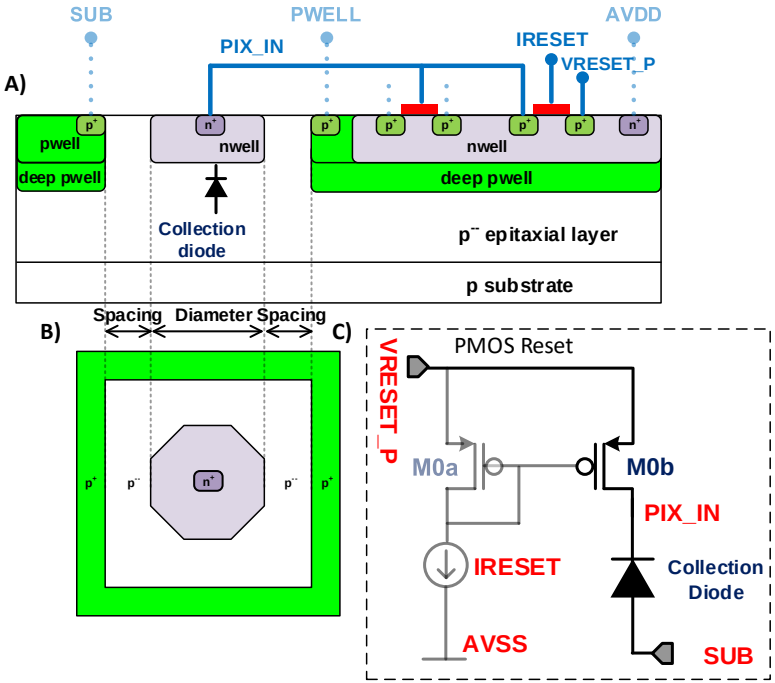
- The front-end acts as an analogue delay line
  - ~2 µs peaking time
- When STROBE is asserted, the front-end binary output is latched into the multi event buffer
- Hit driven architecture
  - Pixel state register readout by a zero suppression circuit based on priority encoding

2. ALPIDE principle of operation
- Sensor configuration and reset

< Diode reset >



< PMOS reset >



- Sensor NWELL collection electrode
  - Octagonal shape with 2 μm diameter
  - Spacing between NWELL and PWELL : 2 μm to 4 μm
- Reset mechanism
  - Diode reset : p+ in NWELL, Reset current depends on the sensor leakage and signal amplitude
  - PMOS reset :
    - Reset current limited by IRESET (> leakage) → control on the reset circuit conductance
    - Additional capacitance on node PIX_IN

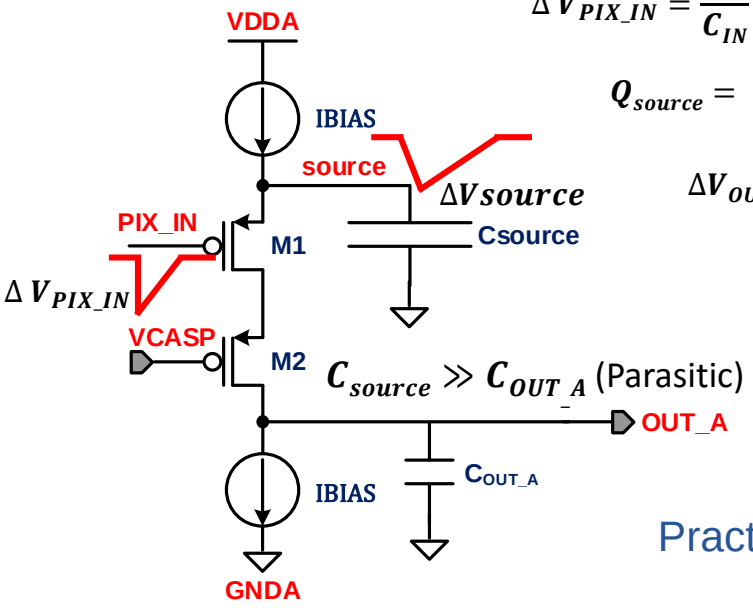
2. ALPIDE principle of operation
- Pixel analog Front end

< Principle >

$$\Delta V_{PIX\_IN} = \frac{Q_{IN}}{C_{IN}}, \qquad \Delta V_{PIX\_IN} \approx \Delta V_{source}$$

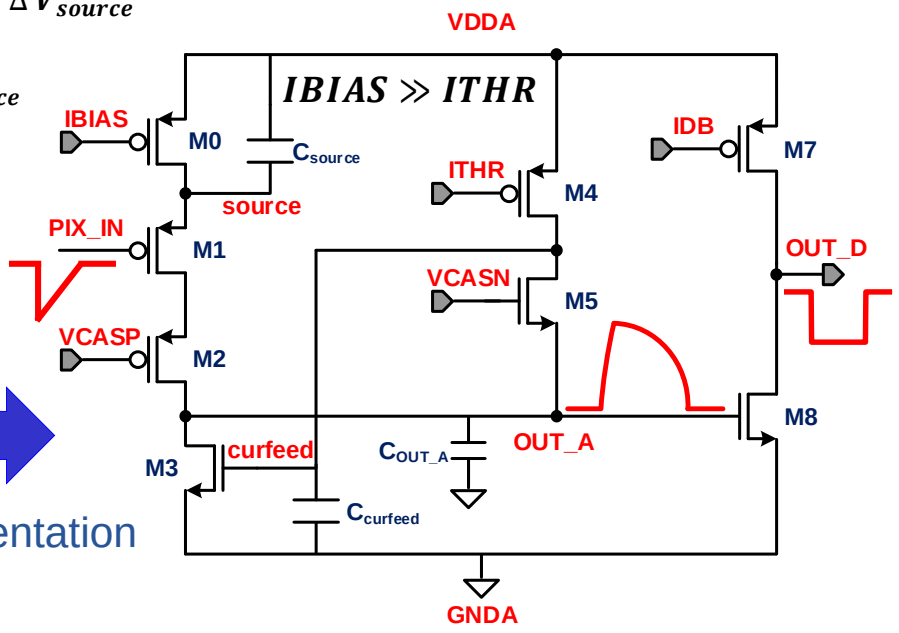
$$Q_{source} = C_{source} \cdot \Delta V_{source}$$

$$\Delta V_{OUT\_A} = \frac{Q_{source}}{C_{OUT\_A}}$$



Practical implementation

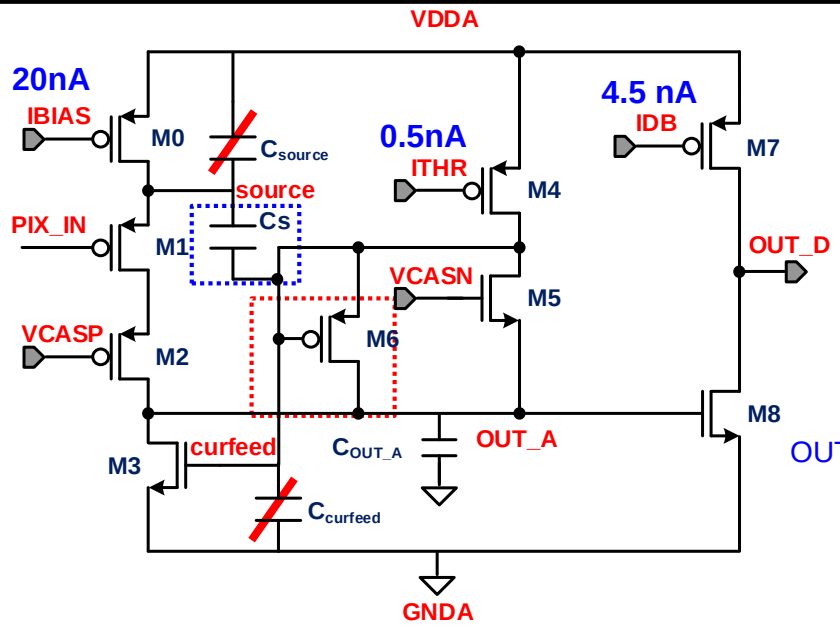
< Front end schematic >



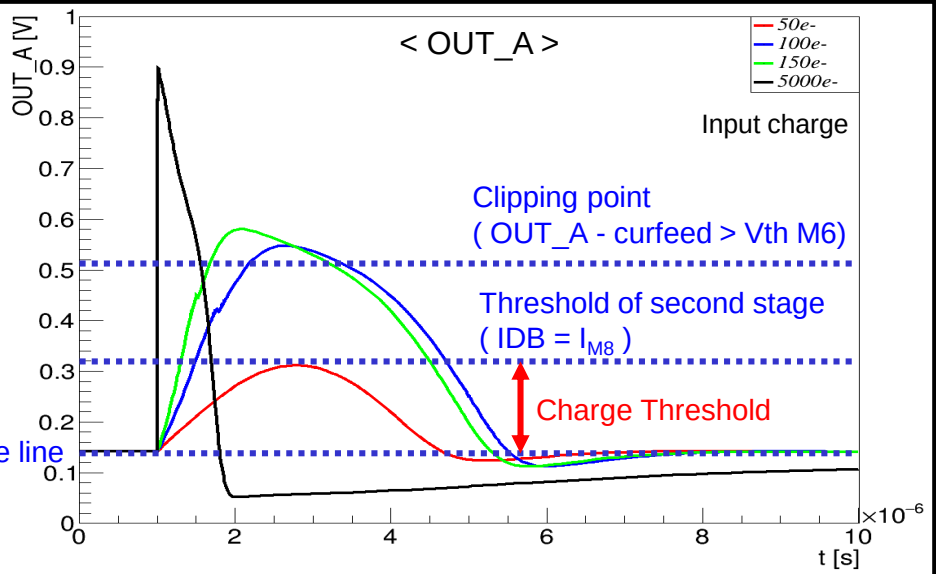
- ITHR, VCASN : To define the OUT_A baseline voltage level
- curfeed net : To set M3 gate voltage level to allow IBIAS+ITHR current
- Active low output (OUT_D) : M8 current (defined by OUT_A) > IDB
- The front-end work on the weak inversion to reduce power consumption
  - IBIAS = 20 nA, ITHR = 0.5 nA → ~40 nW (1.8 V supply voltage)

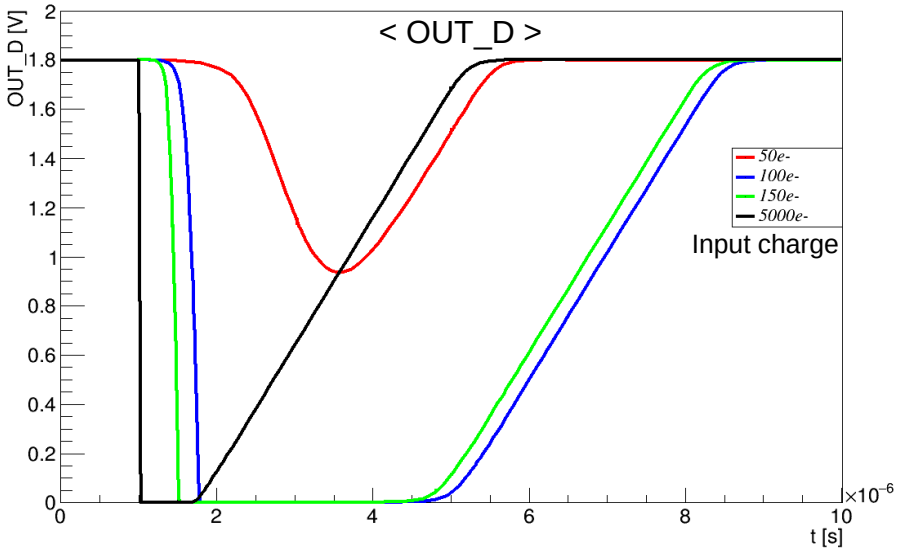
2. ALPIDE principle of operation

- Pixel analog Front end principle



OUT_A base line



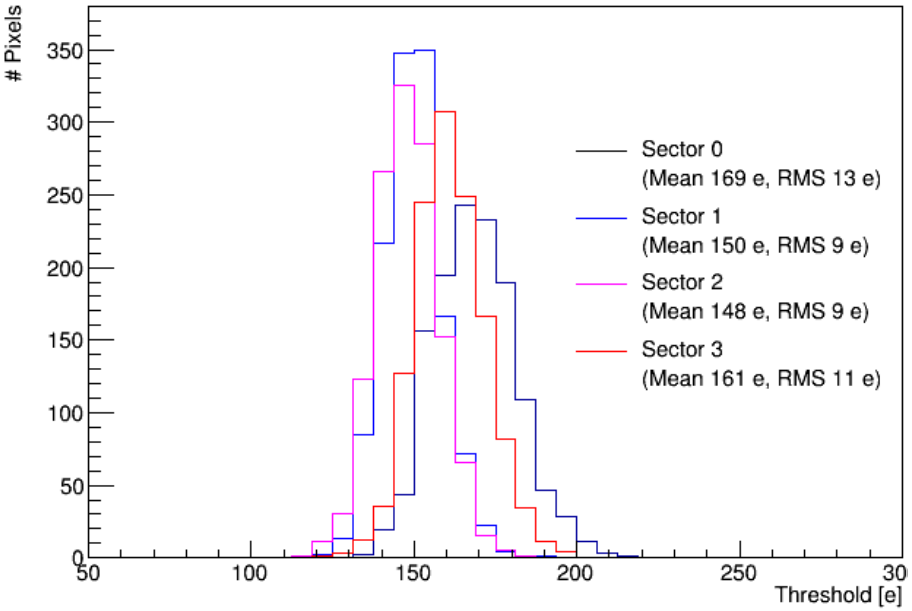


- Combined capacitance to reduce layout area
  - C_{source} and $C_{curfeed}$ → Cs
- Charge threshold parameters
  - OUT_A baseline value : ITHR,VCASN
  - Threshold of second stage : IDB
- Diode connected clipping transistor M6
  - To compress pulse duration for large input

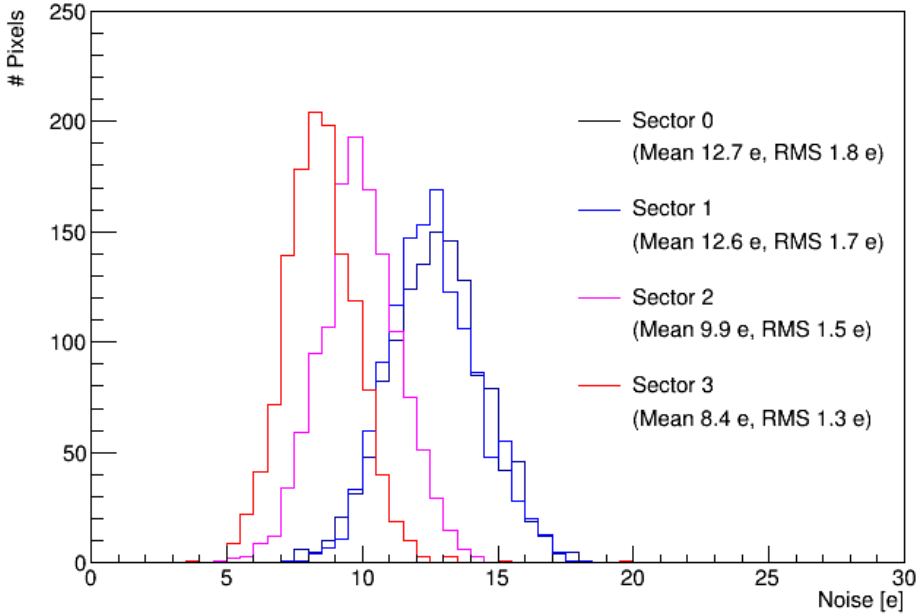
3. Measurement results

- ALPIDE 2 electrical test charge injection results

< Threshold distribution >



< Noise distribution >



Sector	Spacing [μm]	reset	W_{M1} [μm]
0	2	PMOS	0.22
1	2	PMOS	0.92
2	4	PMOS	0.22
3	4	Diode	0.22

- Error function (S-Curve) fit results (substrate voltage : -6 V)
  - Charge threshold : ~155 e^- with 10 e^- rms
  - Noise : ~ 11 e^-

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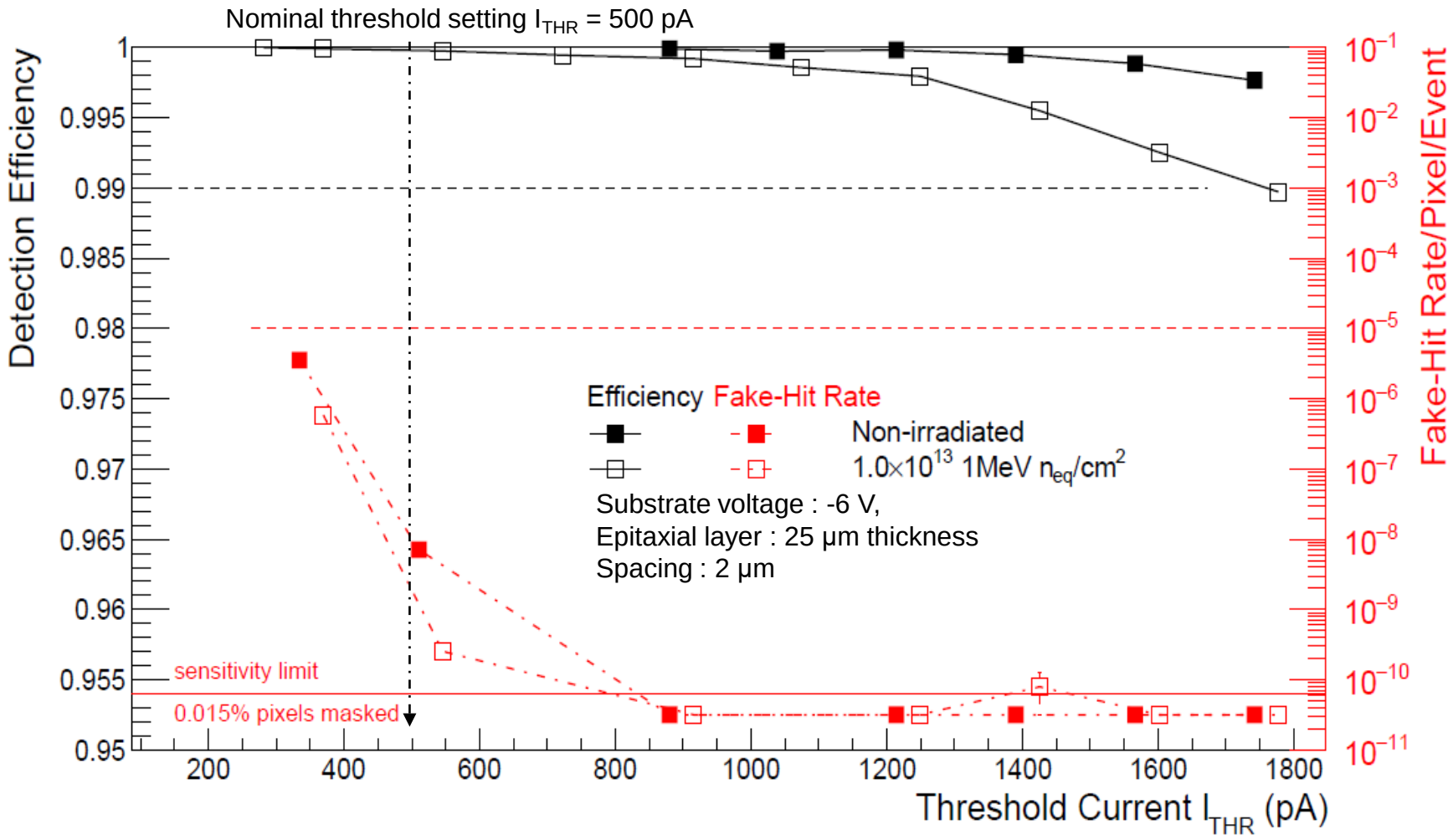
3. Front end Optimization

- ALPIDE 2 beam test results



- ~100% efficiency with fake hit rate of 10^{-8} at the nominal threshold setting

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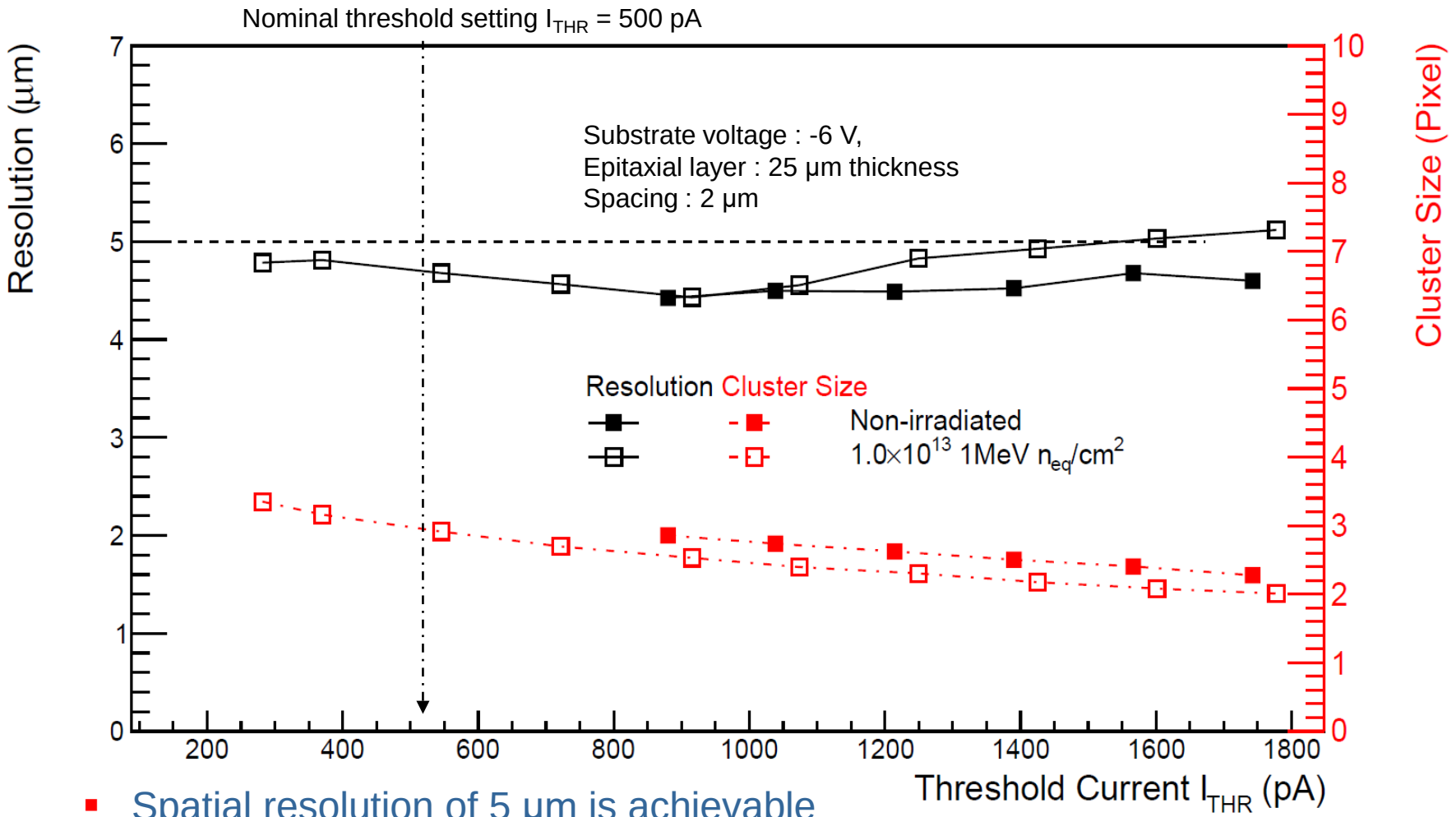
3. Front end Optimization

- ALPIDE 2 beam test results



- Spatial resolution of 5 μm is achievable
- Average cluster size ~2 pixels

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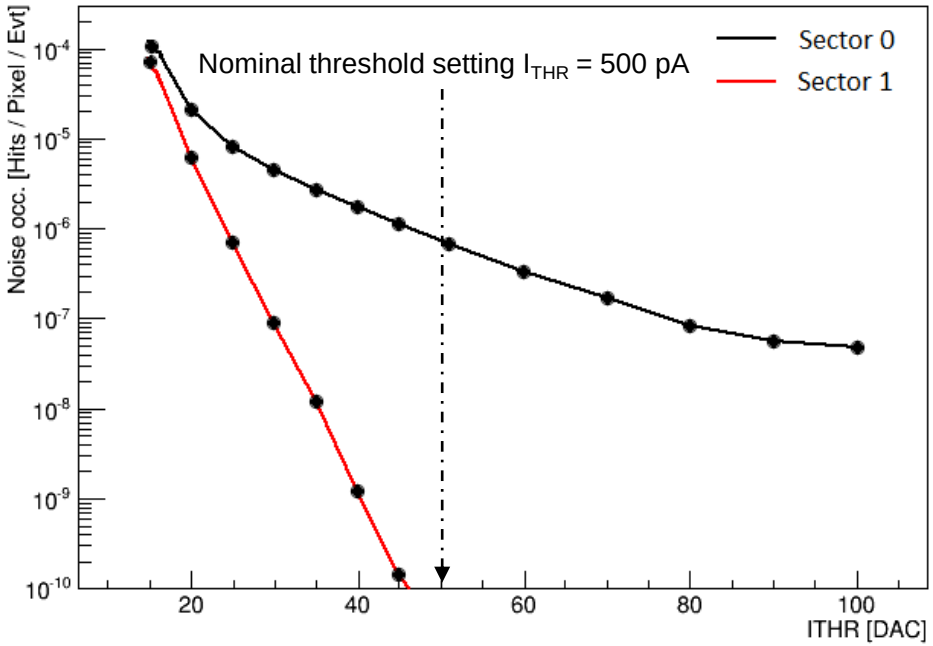
3. Measurement results
- ALPIDE 2 beam test results

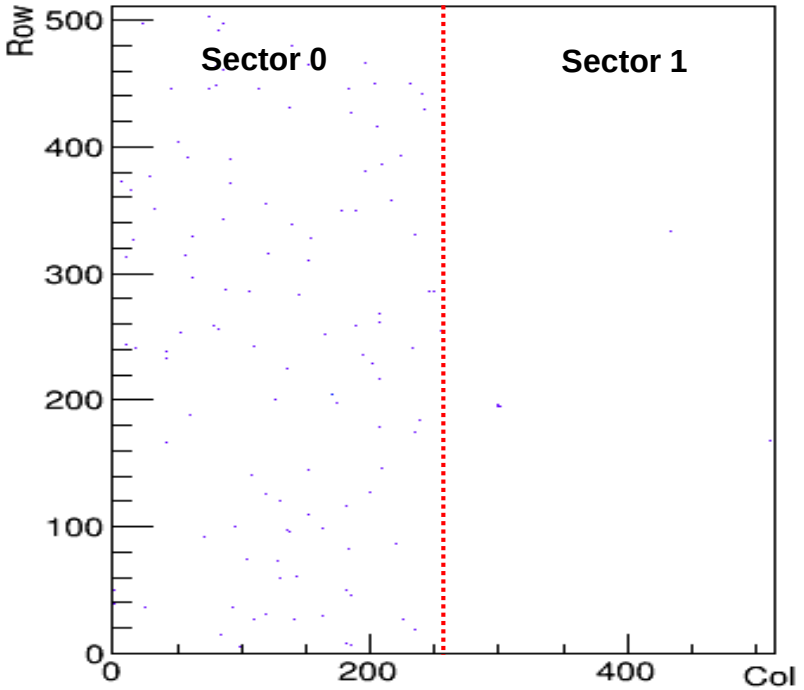
- W_{min} Input transistor (Sector 0) vs. ~ 4 * W_{min} Input transistor (Sector 1)
  - Detection efficiency > 99% (specification) for both Sectors
  - Low threshold setting: Comparable noise level (Gaussian noise)
  - Nominal threshold setting:
    - Sector 1 has lower fake hit rate (lower RTS noise)

Sec.	W_{M1} [μm]	Q_{THR} [e^-]	σQ_{THR} [e^-]	ENC [e^-]
0	0.22	169	13	1.8
1	0.92	150	9	1.7

< Fake hit rate vs ITHR >



< Hit map –random triggers >



Present prototype satisfies ALICE ITS requirements [ALPIDE-1&2]

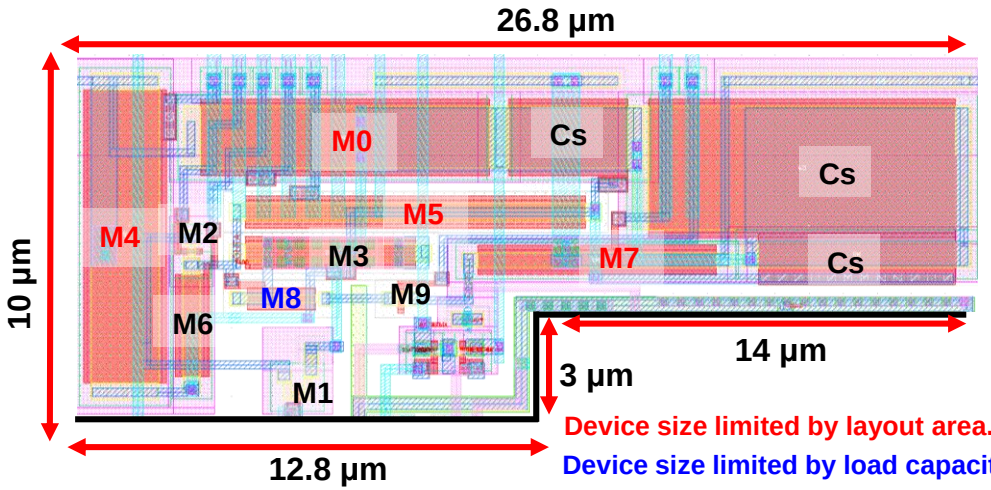
Pixel Optimization for ALPIDE-3

- 3 multi-event buffers
- Charge threshold mismatch
  - Test result : Q_{thr} ~150 e^- with ~10 e^- rms(mismatch)
- Pulse duration variation

  → Very important in trigger mode detector operation

4. Front end Optimization

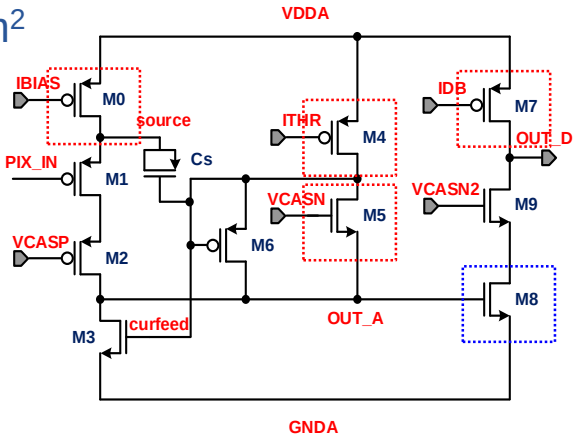
- Device sizing base on Monte-Carlo simulation



~ 220 μm²

Device size limited by layout area.

Device size limited by load capacitance



< Contribution to mismatch by device>

	*rms0 [e-]	W/L [μm/μm]	Area [μm²]	rms [e-]
M0	2.70	1.8/8.5	15.3	0.69
M1	0.06	0.92/0.18	0.16	0.14
M2	0.03	0.22/0.18	0.04	0.14
M3	0.22	0.5/5	2.5	0.14
M4	4.63	2/8.4	16.8	1.13
M5	0.92	0.5/10	5	0.41
M6	0.17	0.5/3	1.5	0.14
M7	0.34	0.42/7	2.94	0.2
M8	0.58	0.22/4	0.88	0.62
M9	0.04	0.42/0.2	0.08	0.14

$$A_{tot} = \sum_{i=0}^{9} A_i$$ → Total area fixed

$$rms = \frac{rms0}{\sqrt{AREA}}$$ → rms0 depends on circuit
→ Large area required

*rms0 : normalized mismatch value for 1 μm² transistor area

$$rms_{tot} = \sqrt{\sum_{i=0}^{9} \frac{(rms0_i)^2}{A_i}}$$ → Weighted sum of squares
→ Area distribution is important

		diode cap. : 2.5 fF	
Monte Carlo	Version	Q_{thr} [e-]	rms [e-]
	ALPIDE-2	94.1	5.0
	ALPIDE-3	**78.3**	**1.7**

- Mismatch reduced by factor 3 from ALPIDE-2

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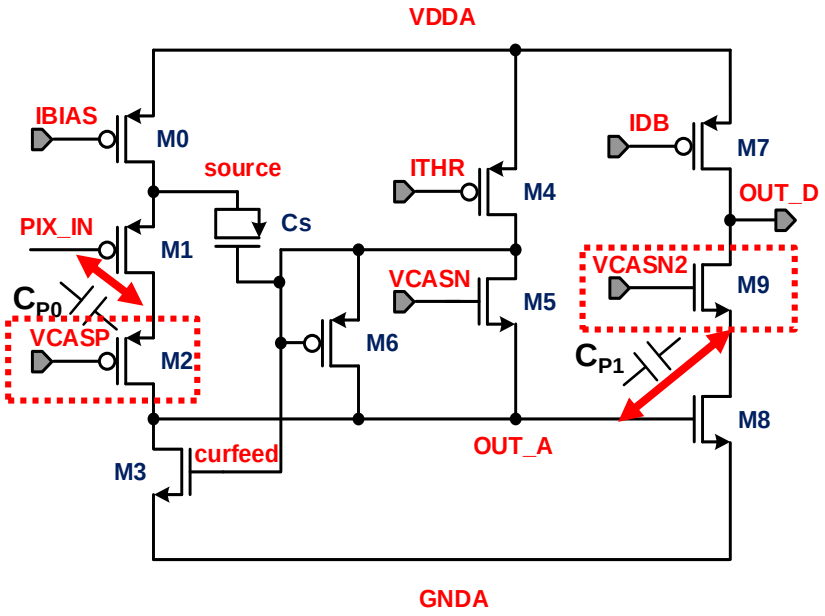
4. Front end Optimization

- Parasitic capacitance impacts charge threshold

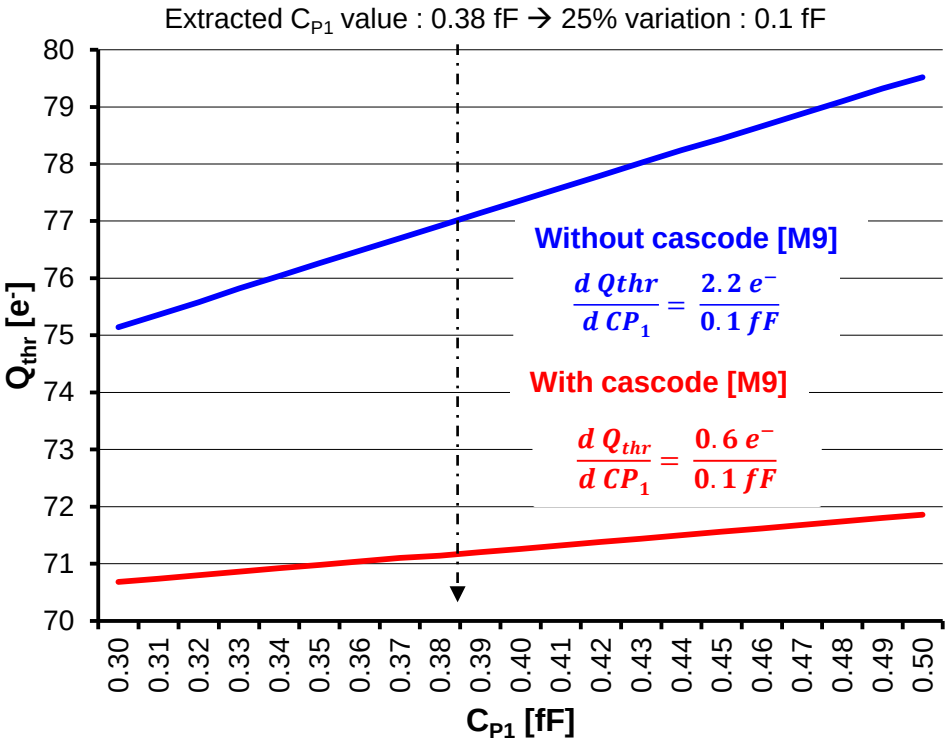
Variation of parasitic capacitance amplified by miller effect

Cascode transistors to avoid Miller effect on parasitic capacitances between high gain nodes

- M2 for C_{P0} : PIX_IN to OUT_A
- M9 for C_{P1} : OUT_A to OUT_D

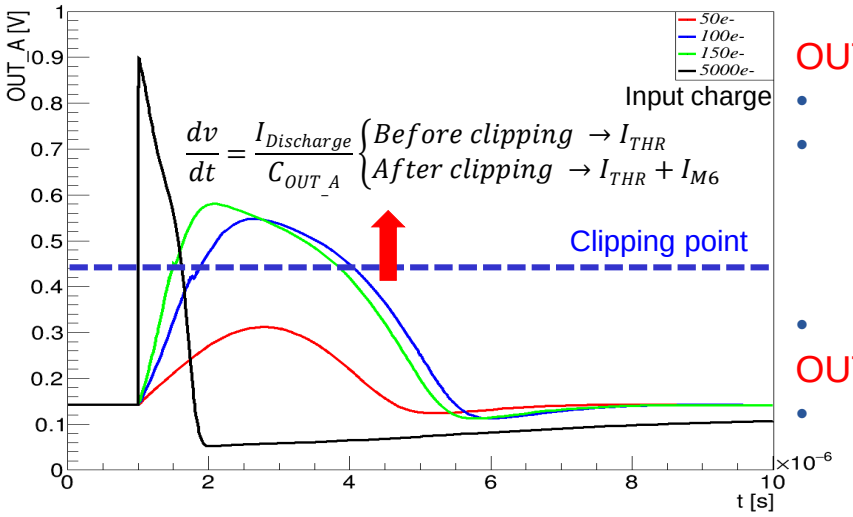


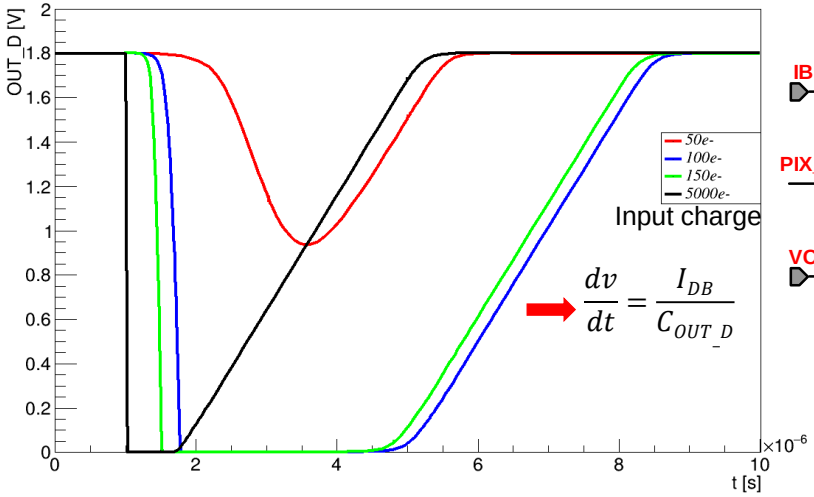
< Sensitivity of the Charge threshold on C_{P1} >



- Effect of C_{P1} mismatch variation on Q_{thr} reduced by factor 4
  (rms from transistor : 1.7 e^- < without cascode : 2.2e^-)

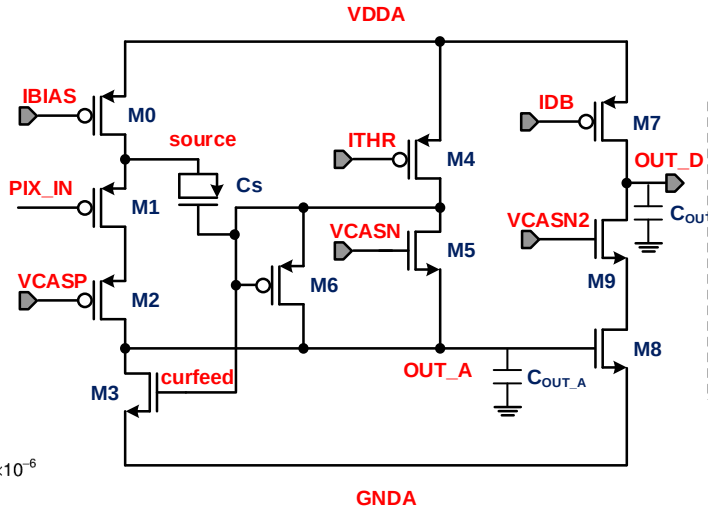
4. Front end Optimization
- Pulse duration uniformity

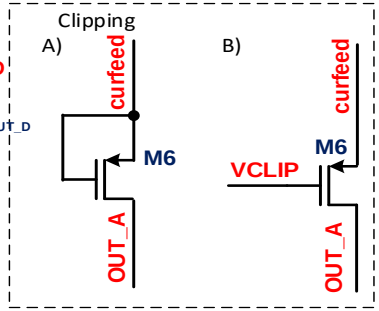




OUT_A
- Larger M4 to reduce I_{THR} variation
- Longer M6 (clipping transistor) to reduce the clipping point variation
  - Diode connection : Fixed clipping point by V_{th} of M6
  - V_{CLIP} : Configurable clipping point by VCLIP voltage
- Cascode transistor[M9] to reduce C_{OUT_A} variation

OUT_D
- Larger M7 to reduce I_{DB} variation





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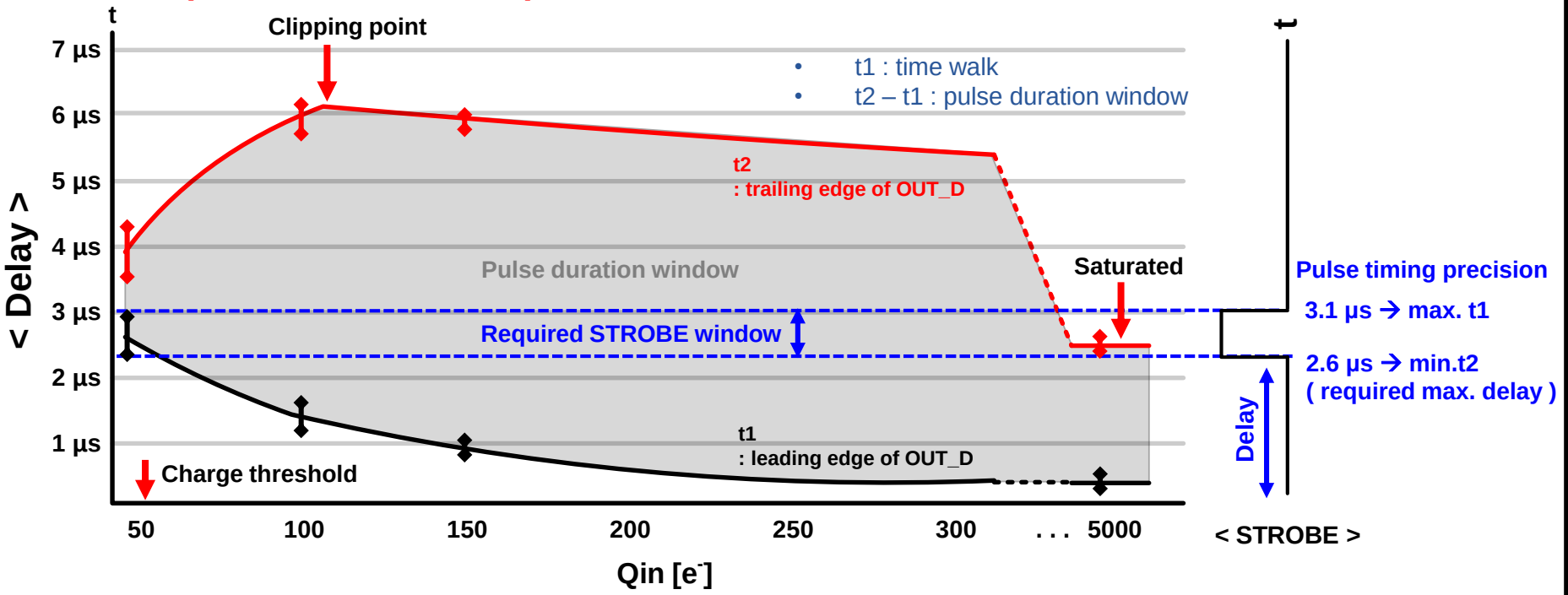
4. Front end Optimization

- Pulse duration vs input charge

- Continuous acquisition mode
- Trigger mode : The front-end is working as an analog memory
  - Keeps hit information up to STROBE arrival



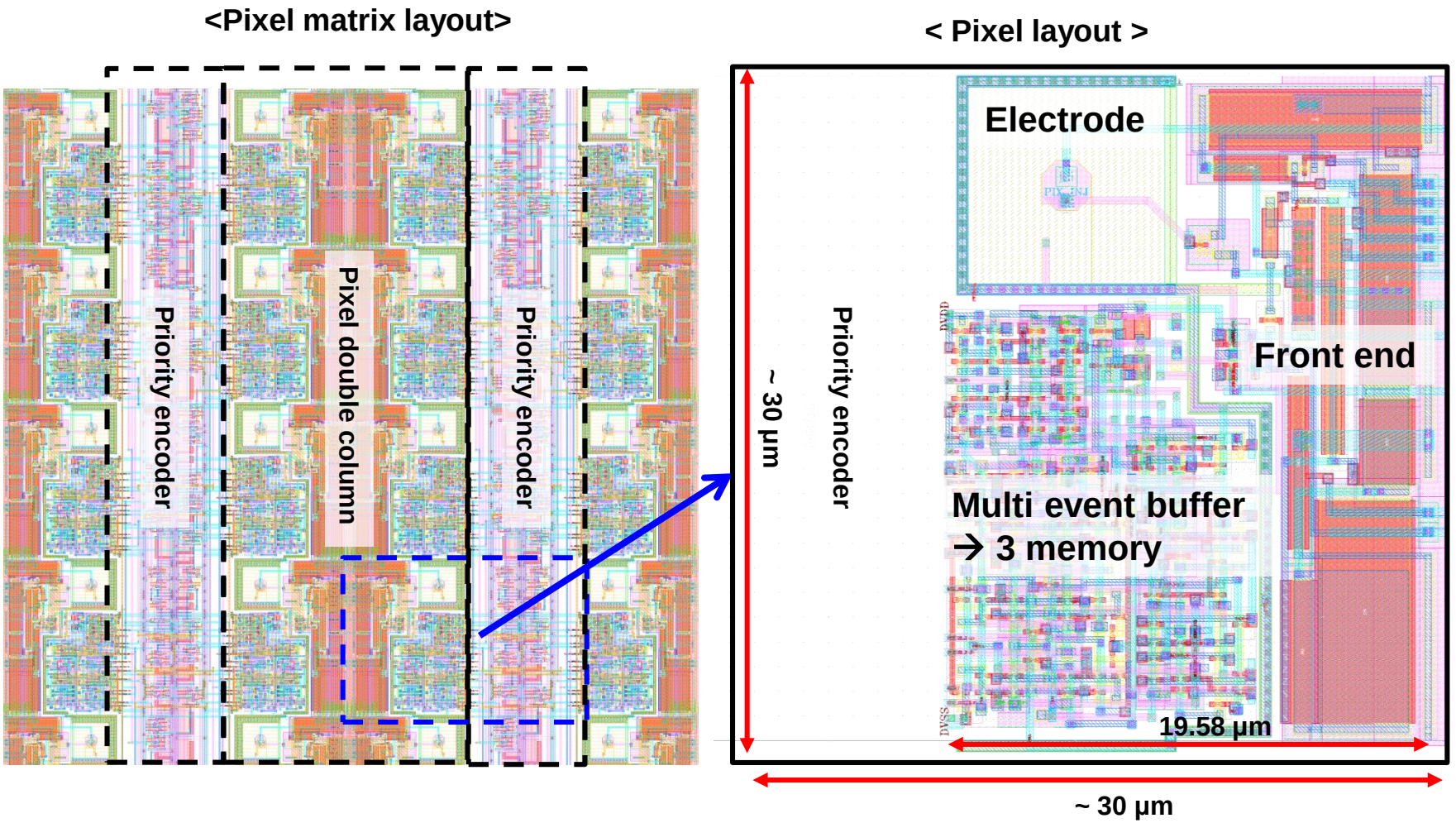
	ALPIDE-2			
	108 e-	118 e-	187 e-	5 ke-
t1 [us]	**2.9 ±0.40**	1.8 ±0.33	0.8 ±0.06	0.5 ±0.01
t2 [us]	**3.6 ±0.92**	6.4 ±0.70	8.16 ±0.28	**1.9 ±0.21**

Reduced variation by factor ~2

	ALPIDE-3			
	50 e-	100 e-	150 e-	5 ke-
t1 [us]	**2.9 ±0.20**	1.5 ±0.16	0.9 ±0.03	0.5 ±0.01
t2 [us]	**3.9 ±0.52**	5.9 ±0.24	5.7 ±0.09	**2.6 ±0.07**

4. Front end Optimization

- Pixel layout picture



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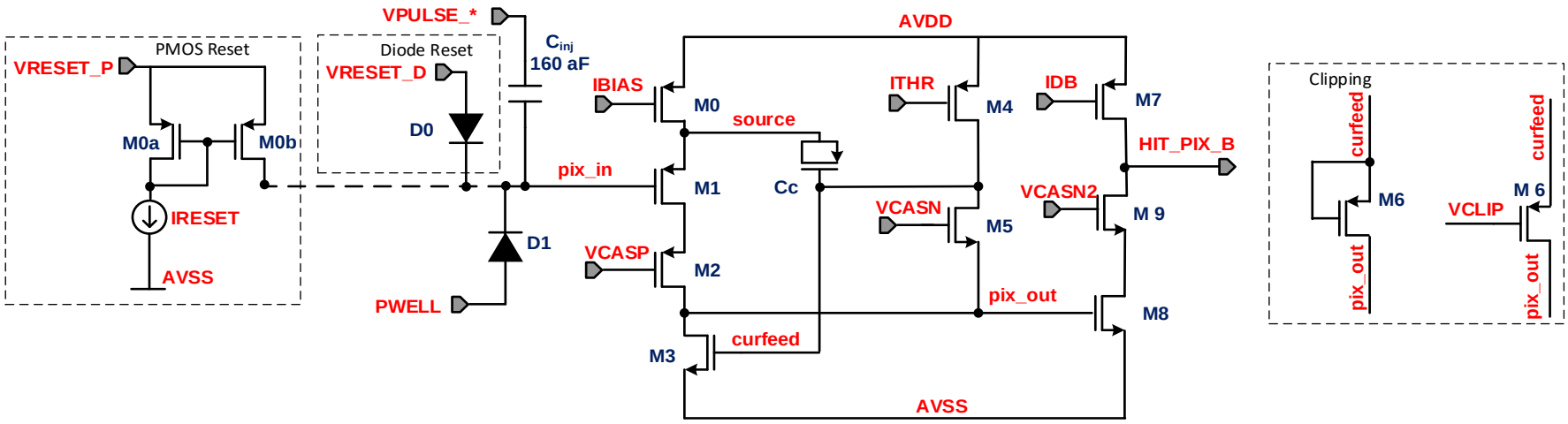
4. Front end Optimization

- 8 different sectors for ALPIDE-3



Sector	M3, M5, M6, M8	VCASN2 (M9)	Clipping M6 gate	M1 bulk	Reset	Spacing
0	optimized size	Yes	diode conn.	AVDD	Diode	2 µm
1	optimized size	No	diode conn.	AVDD	Diode	2 µm
2	as in ALPIDE-1/2	No	diode conn.	AVDD	Diode	2 µm
3	optimized size	Yes	VCLIP	AVDD	Diode	2 µm
4	optimized size	Yes	VCLIP	Source	Diode	2 µm
5	optimized size	Yes	VCLIP	Source	Diode	3 µm
6	as in ALPIDE-1/2	No	diode conn.	AVDD	PMOS	2 µm
7	optimized size	Yes	VCLIP	AVDD	PMOS	2 µm

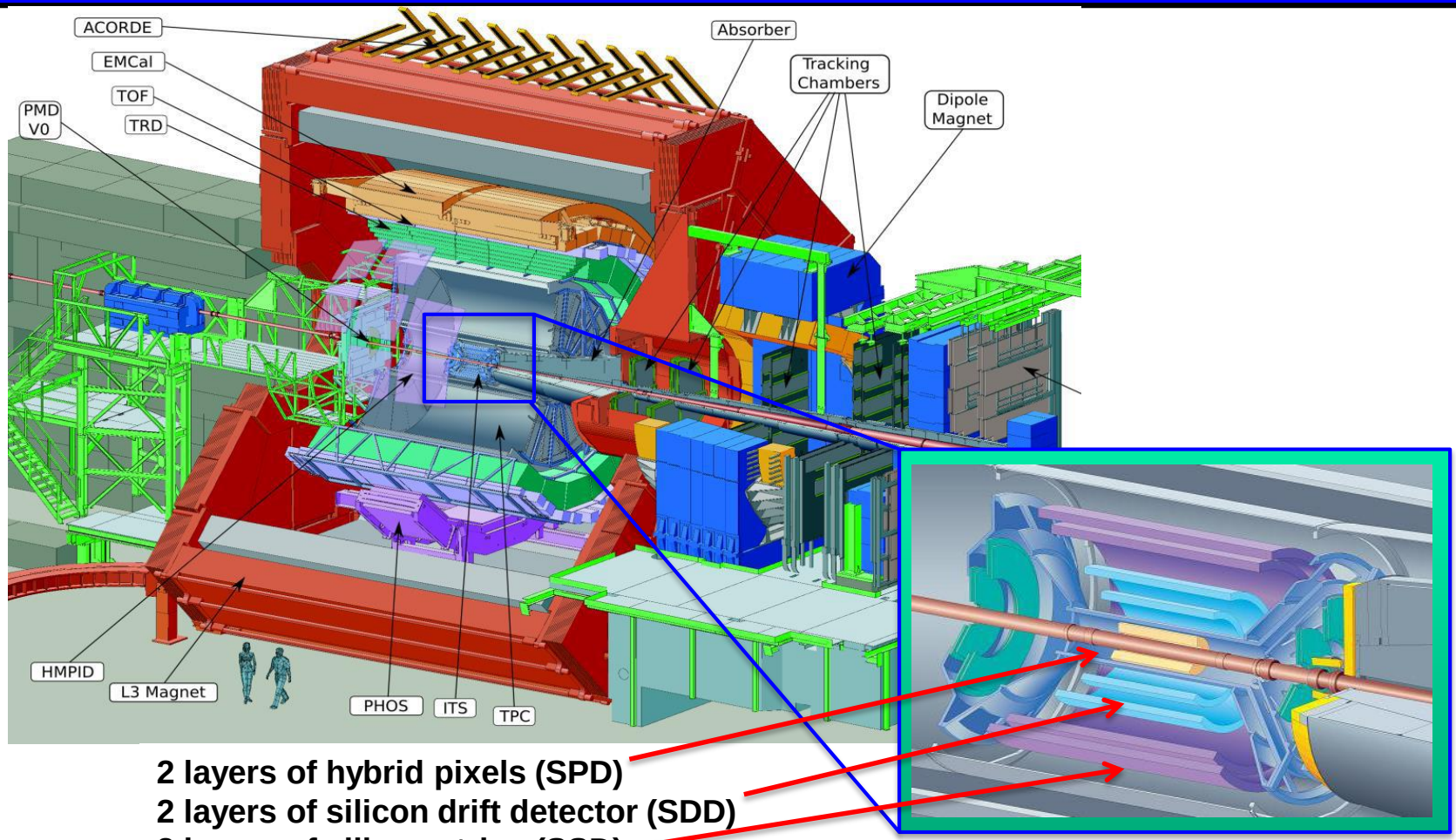
5. Conclusion

- **Sensor performance of present prototype satisfies ALICE ITS requirements [ALPIDE-1&2]**
- **Improvements in ALPIDE-3**
  - **Front end optimization**
    - pixel-to-pixel mismatch reduction based on Monte-Carlo simulation
      - Charge threshold mismatch 3 times lower
        - 2nd stage cascode NMOS (M9)
      - Pulse duration variation reduced by factor 2
        - Resizing of current bias PMOS to reduce discharging variation
      - V_{CLIP} for clipping point control and pulse duration tuning.
  - **Multi event buffer with 3 in-pixel memories**
  - **Contains all final elements for detector**
- **ALPIDE-3 submitted in June 2015 and expected in October 2015**
- **The final chip for ALICE ITS detector will be submitted in February 2016**

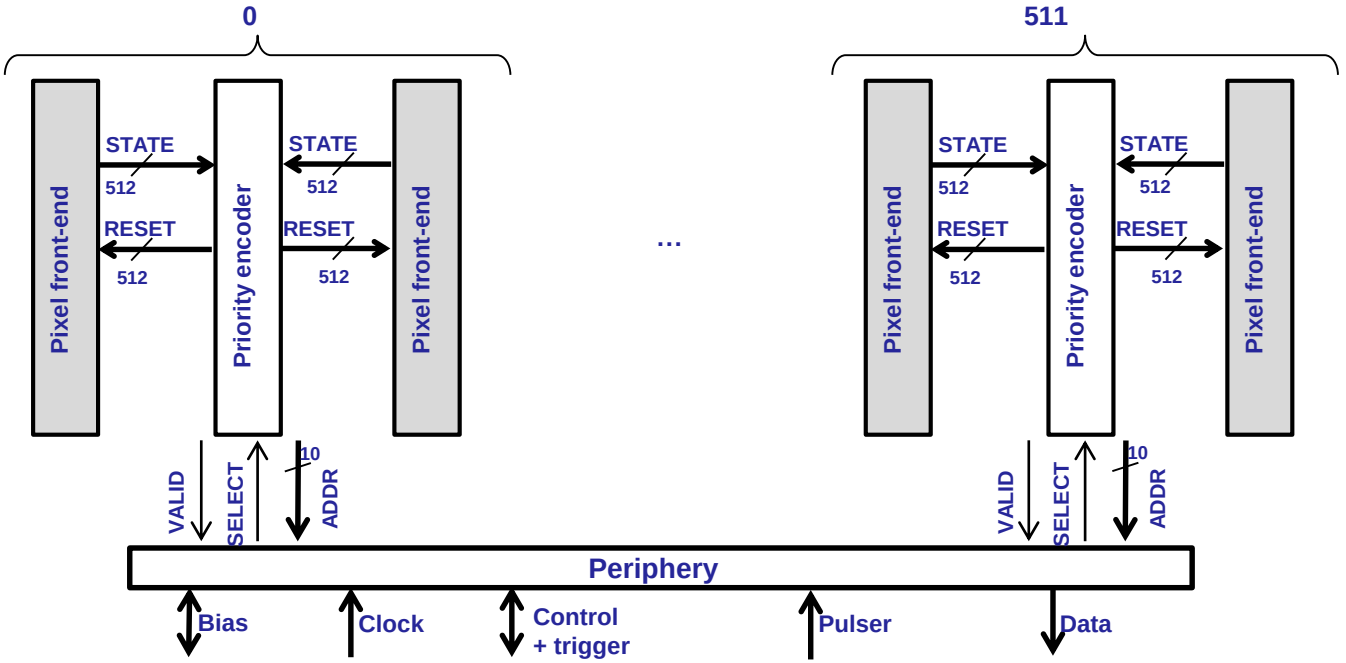
Thank you for your attention

Back up

ALICE Inner Tracking System at present



Hit driven readout



Hit driven architecture:

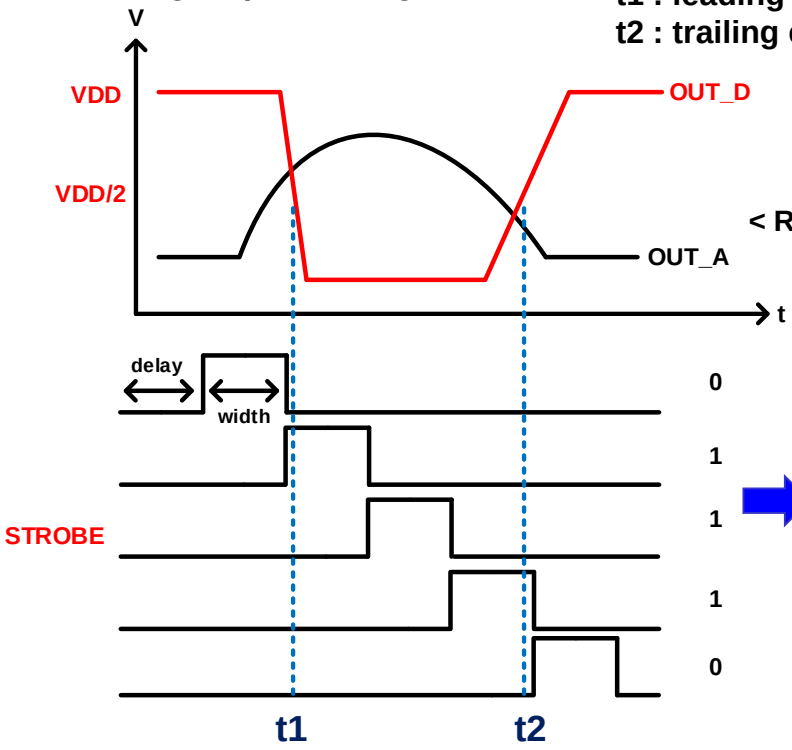
- Priority encoder sequentially provides addresses of all hit pixels present in double column
- No activity if no hit

Principle of the pulse duration

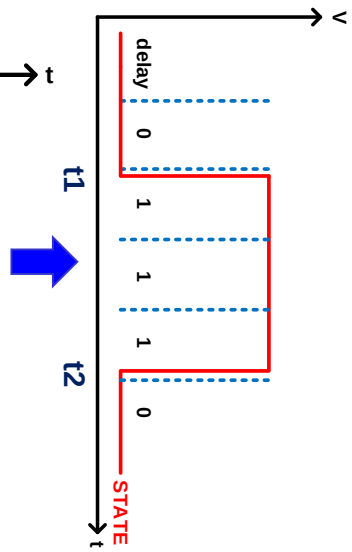
When Strobe is asserted, the front-end binary output is latched into the pixel state register.

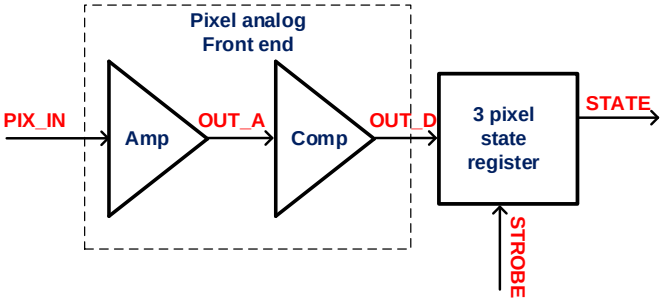
*** Pulse duration = t1 ~ t2**
t1 : leading edge of OUT_D
t2 : trailing edge of OUT_D

< Pulse signal processing >

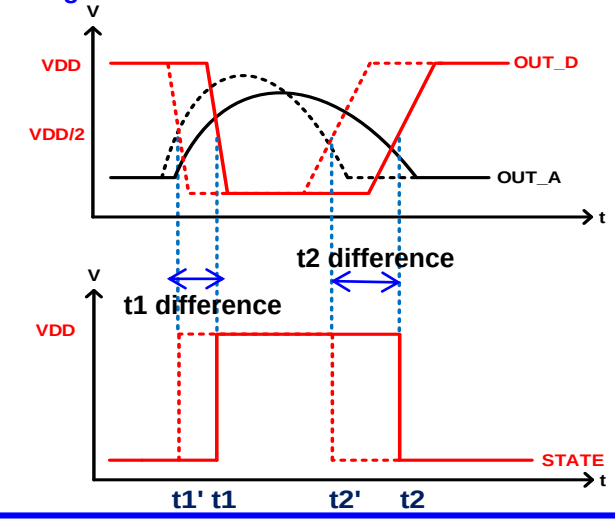


< Reconstructed pulse >



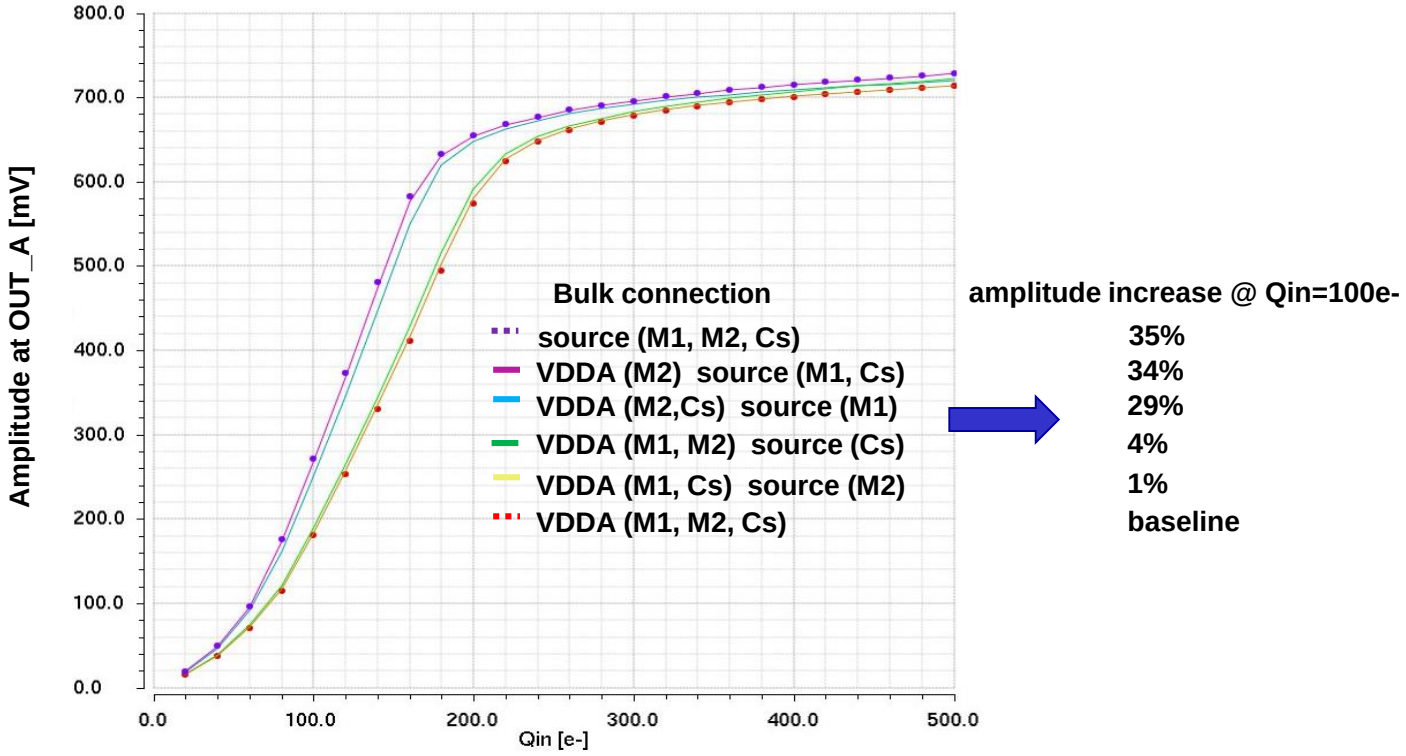


*Pulse duration difference according to input charge difference

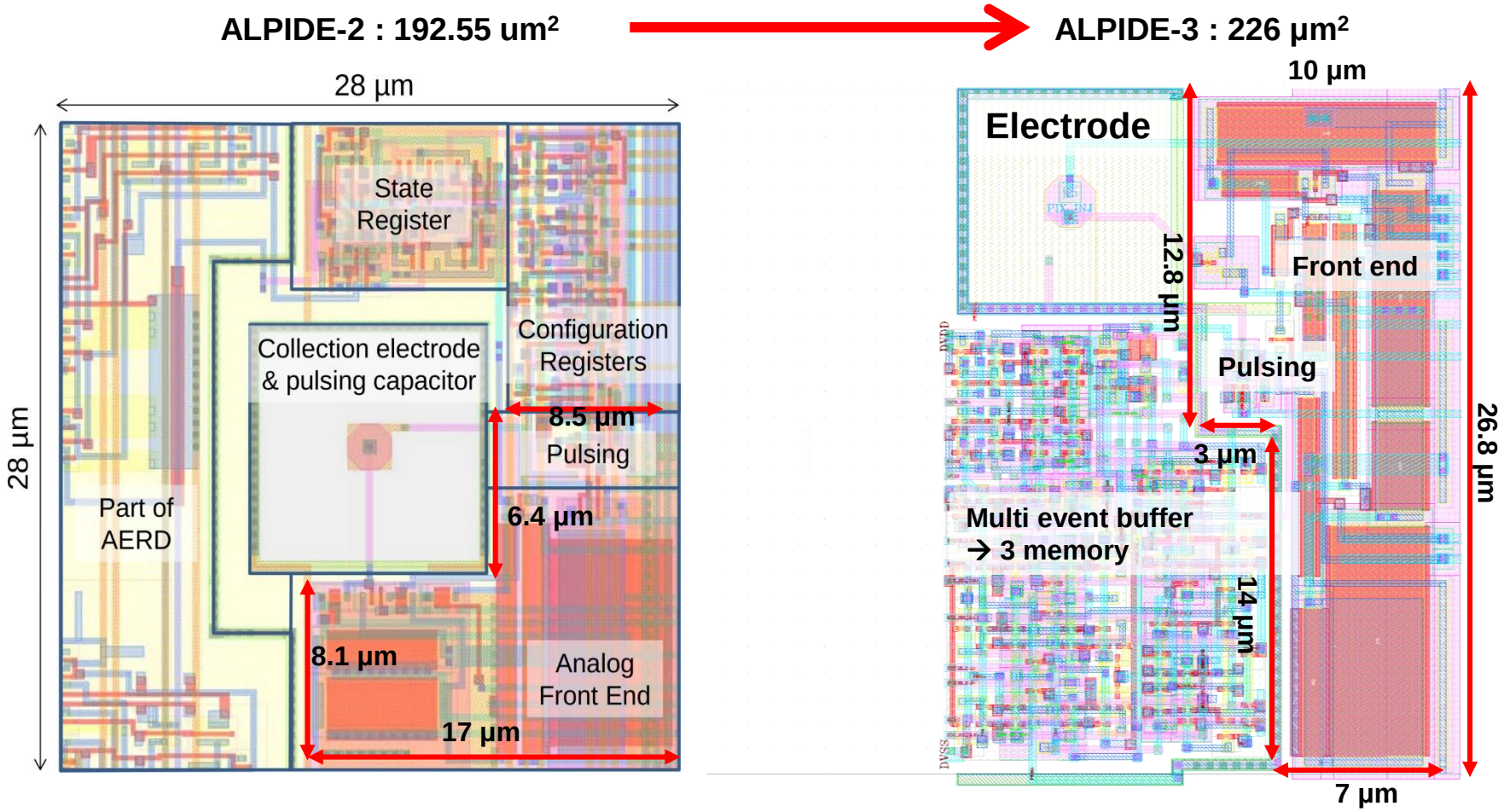


Bulk connection

- The gain increases around 29% if the bulk of the input transistor M1 connected to the sour ce net.
- The gain increases around 1% and 4% if the bulk of the cascode p-type transistor M2 and the capacitor Cs connect to source net, respectively.



Comparison of front end layout area



Device sizing example

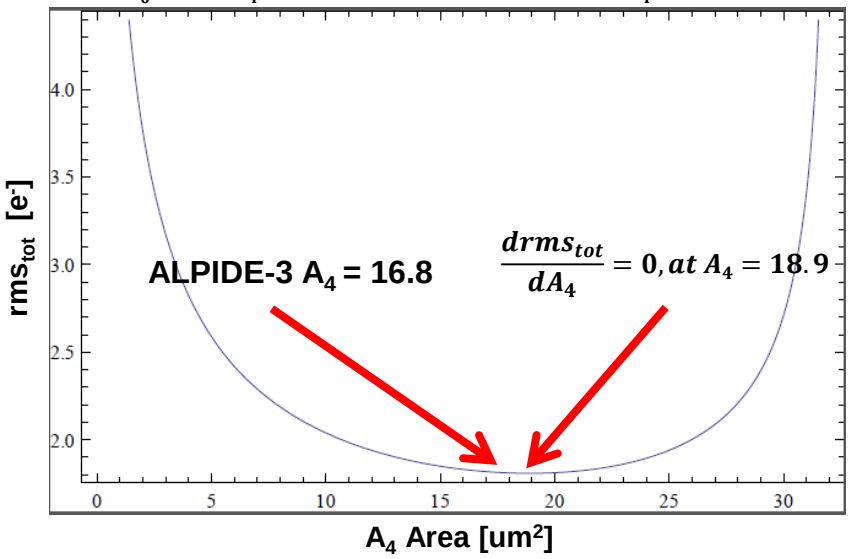
∗rms0 : normalized mismatch value, circuit parameter

$$A_{tot} = \sum_{i=0}^{9} A_i, \qquad rms = \frac{rms0}{\sqrt{AREA}} \qquad rms_{tot} = \sqrt{\sum_{i=0}^{9} \frac{(rms0_i)^2}{A_i}}$$

When A_{tot} is fixed, A_i equation for minimum rms → $\frac{drms_{tot}}{dA_i} = 0$

→ Example :
when M0 and M4 area fixed by 32.1 μm², which is two main contributor

$$rms_{tot} = \frac{rms0_0{}^2}{A_0} + \frac{rms0_4{}^2}{A_4} \text{ ,for minimum rms} \rightarrow \frac{drms_{tot}}{dA_4} = 0$$



< Contribution to mismatch by device >

		Monte Carlo [diode cap. : 2.5 fF]	
Sim.	version	Q_{thr} [e-]	rms(mismatch) [e-]
	ALPIDE1	94.1	4.95
	ALPIDE3	**78.3**	**1.69**

	*rms0 [e-]	W/L [μm/μm]	Area [μm²]	rms [e-]
M0	2.70	1.8/8.5	15.3	0.69
M1	0.06	0.92/0.18	0.16	0.14
M2	0.03	0.22/0.18	0.04	0.14
M3	0.22	0.5/5	2.5	0.14
M4	4.63	2/8.4	16.8	1.13
M5	0.92	0.5/10	5	0.41
M6	0.17	0.5/3	1.5	0.14
M7	0.34	0.42/7	2.94	0.2
M8	0.58	0.22/4	0.88	0.62
M9	0.04	0.42/0.2	0.08	0.14