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## Front end Optimization for the Monolithic Active Pixel Sensor of the ALICE Inner Tracking System Upgrade

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ALICE plans to replace its Inner Tracking System in 2018 with a new 10 m<sup>2</sup> tracker constructed entirely with monolithic active pixel sensors. The TowerJazz 180 nm CMOS imaging Sensor process has been selected to produce the sensor as it offers a deep pwell allowing full CMOS in-pixel circuitry and different starting materials. First full-scale prototypes have been fabricated and tested. Radiation tolerance has also been verified. In this paper the development of the charge sensitive front end and in particular its optimization for uniformity of charge threshold and time response will be presented.

### Summary

A monolithic active pixel sensor for the upgrade of the ALICE Inner Tracking System [1] is being developed in the TowerJazz 180 nm CMOS imaging Sensor process [2] which offers a deep pwell allowing full CMOS in-pixel circuitry and different starting materials.

To limit material budget, power consumption should not exceed 100 mW/cm<sup>2</sup>. The collected charge over input capacitance (Q/C) ratio determines analog power consumption. Varying sensor geometry and applying reverse bias yields an input capacitance of around 2.5 fF [3] and a Q/C for an 18  $\mu$ m epitaxial layer of about 80 mV distributed over a few pixels in a cluster. This allowed the implementation of a  $\sim$ 40nW open-loop binary charge sensitive front end with minimum charge threshold below 100 electrons. A front end peaking time of a few  $\mu$ s allows it to function as a memory: a strobe or trigger with this latency can be applied to latch hit information. A first large-scale prototype fully satisfies ALICE requirements [4]. Measurements revealed an ENC of only a few electrons, but a threshold spread of 18 electrons RMS much larger than simulations predicted. Better channel-to-channel uniformity of charge threshold and time response, intimately related, would further improve operating margins. An in-depth optimization of the front end was carried out: 8 different sectors of 65536 pixels each are equipped with a different version of the pixel gradually introducing various changes to the front end and sensor expected to improve uniformity. These include resizing certain transistors, modification of the circuit including the part to clip large signals, and the introduction of local protection diodes for gates of bias transistors as this was observed to improve matching in other projects [5] even if antenna rules were respected without them.

This third full-scale ALPIDE prototype is being submitted for fabrication now. It is also the first one to include a 1.2 Gb/s data transmission unit. With the 40nW front end, analog power consumption on the full chip is about 5 mW/cm<sup>2</sup>. Total power consumption is expected to be about 40 mW/cm<sup>2</sup>, dominated by digital circuitry and the data transmission unit. Further power optimization is planned as part of the R&D towards a production-ready prototype at the end of this year. The paper will present relevant measurement results on the present prototypes, the front-end design optimization, and hopefully first measurement results on the new full-scale prototype.

### References

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