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Track Finding in CMS for the Level-1 Trigger at the HL-LHC

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The High Luminosity LHC (HL-LHC) will deliver luminosities of up to 5x10ˆ34 cmˆ2/s, with an average of about 140 overlapping proton-proton collisions per bunch crossing. These extreme pileup conditions place stringent requirements on the trigger system to be able to cope with the resulting event rates. A key component of the CMS upgrade for HL-LHC is a track trigger system which would identify tracks with transverse momentum above 2 GeV already at the first-level trigger. This talk presents the status of proposals for implementing the L1 tracking in conjunction with the planned upgrade for the silicon tracker of the CMS experiment. The expected performance and the use of L1 tracks for triggering is discussed.

Summary

The High Luminosity LHC (HL-LHC) will deliver luminosities of up to 5x10ˆ34 cmˆ2/s, with an average of about 140 overlapping proton-proton collisions per bunch crossing. These extreme pileup conditions place stringent requirements on the trigger system to be able to cope with the resulting event rates. One of the goals of CMS for the high luminosity upgrade is to maintain the physics performance achieved during Run 1 in 2012. While the Level-1 (L1) trigger will be upgraded to provide a maximum trigger rate of around 750 kHz (compared to <100 kHz in Run1), even with this increase in rate the thresholds for basic objects (muons, electrons, jets etc) will have to be tightened if no new information can be provided towards the L1 trigger making decision. Therefore a L1 trigger that can make use of reconstructed data from the silicon strip tracker is desirable, thanks to its superior momentum and spatial resolution for charged particles.

The tracking trigger task is to deliver track objects to the L1 trigger within about 5 μs, in order to allow this information to be merged with that from other sub-detectors. Given that a 40 MHz silicon-based tracking trigger on the scale of the CMS detector has never been built, it is essential to demonstrate the feasibility of such system. This presentation will present the status of three different approaches with state of the art technologies: two using a fully FPGA-based approach, and another using a combination of FPGAs and ASICs to perform real time pattern recognition. All three approaches provide full coverage of the Tracker detector, segmenting it into several trigger towers in pseudo-rapidity and azimuth, optimized to provide full coverage and minimal amount of redundancy. In addition, all three approaches have a first stage of off-detector electronics to format the data and time-multiplex them out to a second stage of processor cards, over the course of the time-multiplexing period.

The first approach uses a powerful FPGA to form track seeds, also called tracklets, from pairs of hits in adjacent layers of the tracker. The tracklets then provide a road where consistent stubs are included to form a track candidate. A linearized chi2 fit is used to determine the final track parameters. This presentation will show results of the implementation of the algorithm on a Virtex 7 FPGA with optical fiber communication to neighboring boards. We will also discuss the developments of the hardware demonstrator and further plans for dedicated board prototypes, using CPT7 boards, developed by Wisconsin, using a Virtex-7 FPGA and MiniPOD optical links, hosted in a μTCA crate.

In the second approach a concept for an FPGA-based track finder using a fully time-multiplexed spatially pipelined architecture is presented. The tracker would be segmented into five independent trigger regions in η. Additionally, by fully time-multiplexing, each main processor card receives the data from a single event across a full trigger region, eliminating the need for inter-communication between processor cards, or a final

duplicate removal hardware stage. An implementation of a track finder operating under high luminosity conditions, using an r-ϕ Hough Transform has been developed and tested in FPGAs. A hardware demonstrator using MP7 processing boards, developed by Imperial College, featuring Xilinx Virtex-7 FPGAs and Avago MiniPOD optics, is described.

The third approach profits from the use of a dedicated ASIC, known as an Associative Memory (AM) chip using content addressable memories (CAM), to perform a first pattern recognition, followed by an FPGA track fitter. The AM chip finds track candidates in coarse resolution patterns, i.e., roads, by performing real time matching of the hits in several detector layers to pre-calculated patterns stored in the AM. The high resolution hit data belonging to the matched pattern are then retrieved and a second step of track reconstruction is performed on a FPGA, thus dealing with a smaller combinatorial problem. The hardware demonstrator is based on 40G+ ATCA crates, hosting special boards for data formatting (Pulsar IIb, developed by FNAL) and special FMC mezzanines (developed by INFN and FNAL) loaded with last generation AM chips.

Authors: RYD, Anders (Cornell University (US)); PALLA, Fabrizio (Universita di Pisa & INFN (IT)); PESARESI, Mark (Imperial College Sci., Tech. & Med. (GB))

Presenter: PESARESI, Mark (Imperial College Sci., Tech. & Med. (GB))

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