The Calorimeter Trigger Processor Card: The Next Generation of High Speed Algorithmic Data Processing at CMS

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Overview

The first layer of the CMS Level-1 upgraded calorimeter trigger requires a powerful, flexible and compact processing card. The Calorimeter Trigger Processor Card (CTP7) uses the Virtex-7 FPGA as its primary data processor and is the first in CMS to employ the ZYNQ SoC running embedded Linux to provide TCP/IP communication and board support functions. The CTP7 was built from the ground up to support AXI infrastructure to provide flexible and modular designs with minimal time from project conception to final implementation.

CTP7 key designs points:
- Virtex-7 690T FPGA
- ZYNQ SoC FPGA with dual ARM Cortex-A9 CPU
- Embedded Linux Operating System running on the ZYNQ
- 80 RX and 61 TX GTH I/O links, multi-rate, LHC-synchronous or asynchronous link operation
- Heavy duty power and cooling infrastructure

CMS Calorimeter Stage-2 Layer-1 Trigger
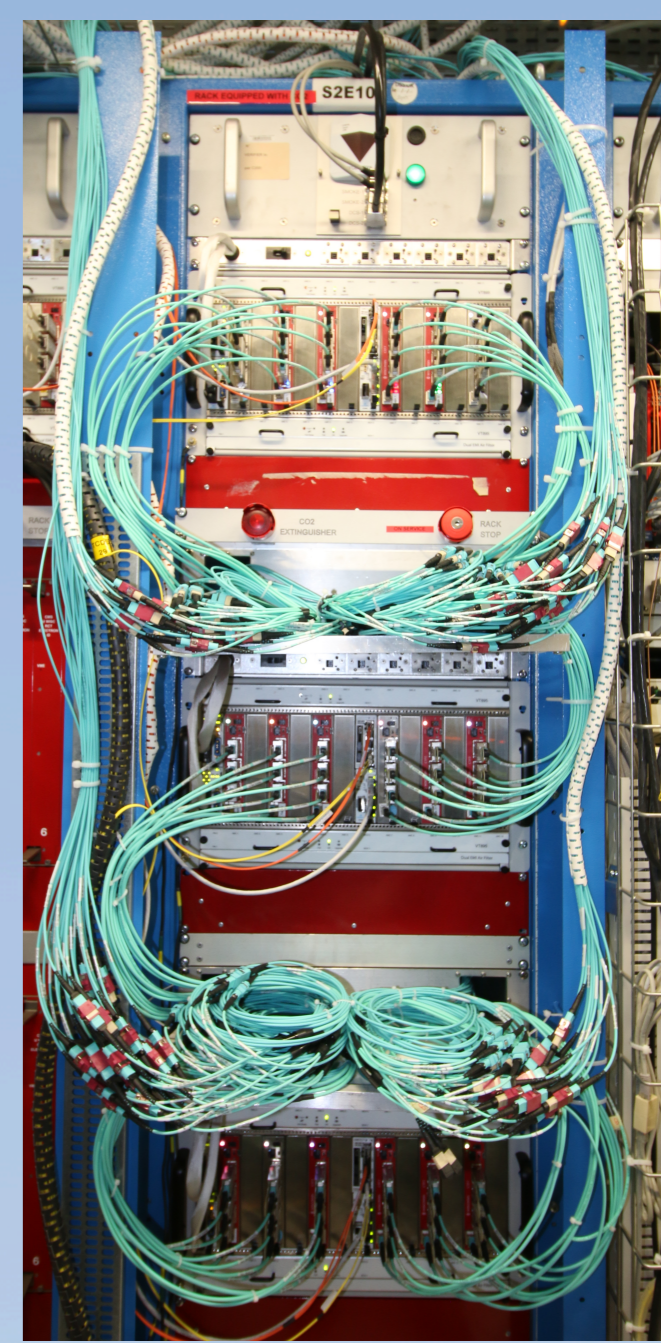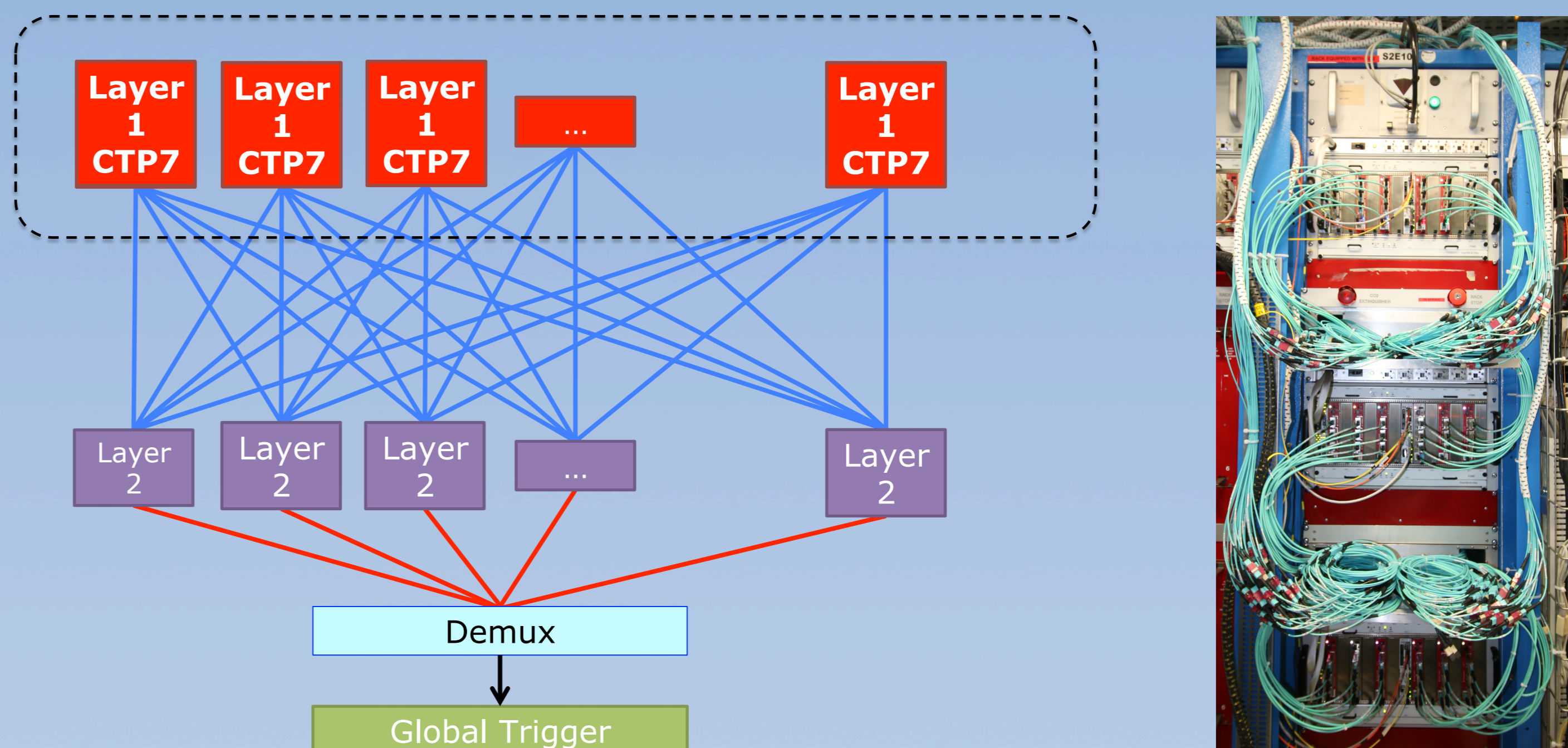
(Above) CMS Calorimeter Stage-2 Layer-1 Trigger, implemented using CTP7 cards.
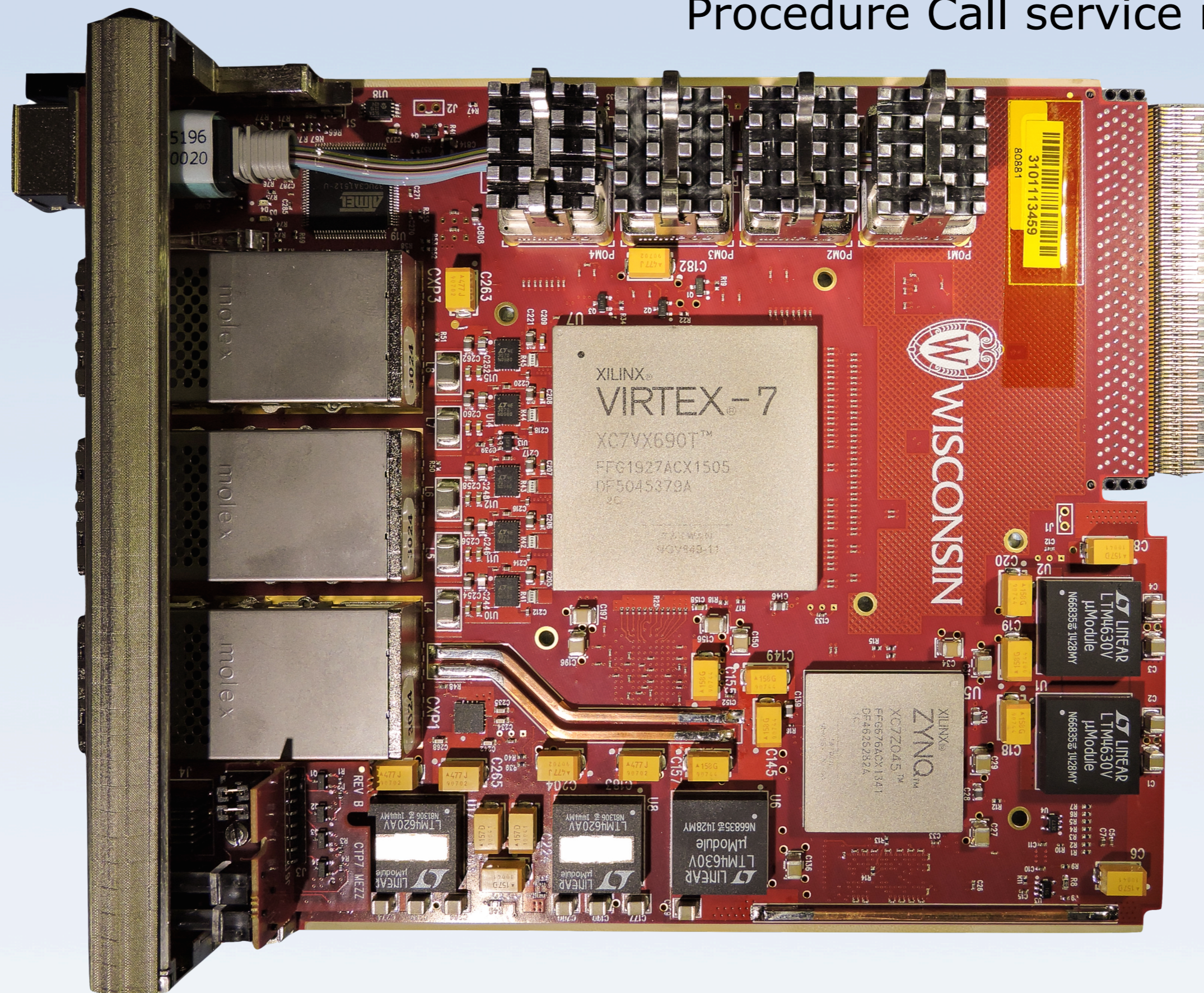
Functionality:
- True triple-rate card: mixing 4.8/6.4/10 Gbps and synchronous/asynchronous links in the same MGT blocks
- Combines 3 different calorimeter subsystems: ECAL, HCAL, and HF
- Aligns and decodes input data from the calorimeters
- Applies tower-level calibration in lookup tables
- Builds combined trigger tower words, streaming them to Layer-2
- Event-by-event DAQ readout for data quality monitoring
- Captures inputs and outputs at reduced rate by means of Remote Procedure Call service running on the ZYNQ

CTP7 Firmware Design Concept

The combination of ZYNQ, Virtex-7 and AXI infrastructure gives the CTP7 the richest possible combination of hard and soft peripherals and industry-proven IP cores available anywhere.

- Modular firmware environment allows existing firmware blocks (including MGT links) to be quickly configured to support new applications.
- AXI (Advanced eXtensible Interface) interconnect protocol family is the most recent generation of industry standard Advanced Microcontroller Bus Architecture (AMBA) interfaces.
- AXI Chip-to-Chip Xilinx IP core is employed to seamlessly extend the memory space of the ZYNQ FPGA to the Virtex-7 FPGA.

(Above) A selection of readily available standard AXI IP cores in Xilinx Vivado Toolset

CTP7 Link I/O Summary

Optical Links: 67 RX + 48 TX
- Avago MicroPOD engine in front pluggable CXP and MiniPOD form factor
- Virtex-7 690T Front Side: 40 RX, 36 TX Optical Links
- Virtex-7 690T Back Side: 27 RX, 12 TX Optical Links

Backplane Links: 14 TX+RX
- Virtex-7 690T Back Side Connections
- 8 TX+RX Pairs: VT894/VT895 Backplane Fabric
- 4 TX+RX Pairs: MCH1 Fat Pipe
- DAQ TX+RX Pair to AMC13 in MCH2 Slot
- GbE TX+RX Pair to MCH1 GbE Switch (from ZYNQ)

Flexible clocking infrastructure is provided by dual SI5324 clock synthesizer/fanout and cross-point circuitry.

ZYNQ System-on-Chip and the Embedded Linux Advantage

The ZYNQ FPGA runs embedded Linux which is automatically loaded from a microSD card and is responsible for GbE TCP/IP communication and ancillary functions on the CTP7. The embedded Linux brings a full file system, peripheral device drivers, and functional shell to the card which streamlines debug and offers a platform for low-latency operations on the card. A set of specialized Linux-based software was also developed: **Integrated Eye Scan Engine**, **Xilinx Virtual Cable Service, dedicated Memory Service**, **Remote Procedure Call Service**, and **IPMI-Integrated Initialization Agent**.

ZYNQ-based Xilinx Virtual Cable (XVC)

This service replaces a physical cable with a TCP/IP connection to Xilinx toolset. This is useful where JTAG cables are not easily employed; it does not require JTAG infrastructure in the uTCA crate.

CTP7 Implementation:
- ZYNQ connects to Virtex-7 JTAG pins through programmable logic
- Cable Server runs on ZYNQ embedded CTP7 Linux system
- Allows remote debug of Virtex-7 firmware via LAN connection to ZYNQ
- Allows an active JTAG connection per card, unlike methods that use crate-based JTAG solutions

ZYNQ-based XVC   Support PC   Xilinx JTAG Cable
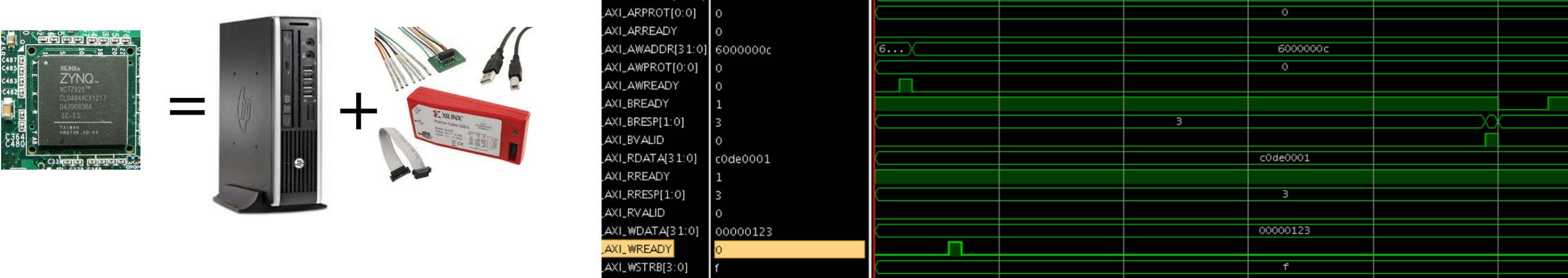
ZYNQ-based Integrated Eye Scan (IES)

- Eye Scan Capability of IBERT ported to ZYNQ
- Non-invasive scans taken on live operational data (not PRBS test patterns)
- Parallel multi-channel capability for faster results
- **Programmable engine can be used for a wide range of applications**
  - Quantitative link characterization and parameter optimization
  - Operational troubleshooting
  - Trend analysis and forecasting for preventive maintenance

Eyescans taken at CMS during physics fill with stable beams in the LHC

ECAL link @ 4.8 Gbps   HCAL link @ 6.4 Gbps