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65 nm CMOS analog front-end for pixel detectors at the HL-LHC

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This work is concerned with the design and the experimental characterization of analog front-end electronics conceived for experiments with unprecedented particle rates and radiation levels at future high-energy physics colliders.
A prototype chip integrating different test structures has been submitted in the framework of the CHIPIX65 project. These structures are standalone channels for the readout of hybrid pixels, featuring a charge sensitive preamplifier as the first stage of the readout chain, a high-speed comparator and a circuit for fine threshold tuning.
The full characterization of the analog front-end will be discussed in the conference paper.

Summary

Next generation pixel chips at the HL-LHC will be exposed to extremely high levels of radiation and particle rates. In the so-called Phase2 upgrade ATLAS and CMS will need a completely new tracker detector, complying with the very-demanding operating conditions and the delivered luminosity (up to 5x10ˆ34 cmˆ-2sˆ-1 in the next decade).
The 65nm CMOS technology exhibits a high degree of radiation tolerance and appears to be suitable for the design of rad-hard electronics in harsh radiation environments.
The INFN CHIPIX65 project is meant to explore the 65nm CMOS technology for the design of the pixel front-end electronics for these environments. It is focused on the development of core elements in analog and digital electronics and on the chip integration issues, particularly important when complex digital circuits, with a huge amount of transistors, have to be integrated with the analog front-end electronics. Most of the research units of CHIPIX65 are member of the international collaboration RD53 that is developing readout chips for the innermost pixel layers of ATLAS and CMS at the HL-LHC.
In the framework of CHIPIX65, a prototype chip called CHIPIX-VFE-1, including different test structures, has been submitted and a comprehensive characterization activity is ongoing. CHIPIX-VFE-1 includes two small matrices with different front-end designs both using a common digital configuration and readout architecture, and standalone analog channels.
This work describes the design and the experimental characterization of the CHIPIX-VFE-1 standalone channels, which represent fundamental building blocks for the development of an innovative pixel front-end chip for the HL-LHC. These channels include a charge sensitive preamplifier and a high-speed comparator with local trimming DAC.
The charge sensitive preamplifier (CSA) implements a folded cascode scheme in its forward gain stage and is responsible for most of the power consumption in the analog section (about 5 uW). The CSA features a Krummenacher feedback network able to compensate for detector leakage current up to tens of nanoamps. Noise simulations on the analog channel show an ENC close to 115 e- r.m.s.
The tests carried out on the channels are mainly focused on the CSA and on its different possible configurations. In particular, the CSA can be operated in two gain modes and with different capacitance, emulating the detector, connected to the preamplifier input. The recovery current in the Krummenacher feedback network can be set to two different values.

The signal from the CSA is fed to a high-speed threshold discriminator, featuring a current comparison architecture. The comparator, combined with a digital counter, can be exploited for amplitude measurements by means of the time-over-threshold technique.
A circuit for fine threshold tuning, featuring a 4-bit binary weighted DAC, has been integrated in the analog channel in order to improve the threshold dispersion performance.
The conference paper will report the full experimental characterization of the analog front-end, including results relevant to the CSA, comparator and threshold tuning system.

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