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SAMPA Chip: a New ASIC for the ALICE TPC and MCH Upgrades

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This paper presents the SAMPA ASIC that will be used in the ALICE upgrade for time projection chamber (TPC) and muon chamber (MCH) read-out frontend electronics.
The SAMPA ASIC is being designed in 130nm CMOS technology with 1.2V nominal voltage supply. The SAMPA ASIC includes 32 channels, with selectable input polarity, and five possible combinations of shaping time and sensitivity. Each channel comprises a Charge Sensitive Amplifier, a semi-Gaussian shaper and a 10-bit ADC, followed by a DSP block. Experimental results for 18.5pF detector capacitance show an ENC of about 600e- and 20mV/fC sensitivity.

Summary

Operating the ALICE TPC (Time Projection Chamber) at a Pb-Pb collision rate of 50kHz requires to replace the present MWPC based read-out by GEM detectors, which feature intrinsic ion blocking without additional gating and exhibit excellent rate capabilities. As the drift time is higher than the average time between interactions, a trigger-less continuous read-out is required. For the Muon Chambers (MCH), the present front-end electronics installation does not cope with the increased interaction rate and needs to be replaced. Thus, the new read-out ASIC, named SAMPA, is developed for both the TPC and Muon Chamber.

The SAMPA ASIC integrates 32 channels of the full data processing chain, designed in TSMC 130nm CMOS technology with nominal voltage supply of 1.2V and supports continuous and triggered read-out. The SAMPA chip will occupy an area of about 80mm^2.
It comprises positive/negative polarity Charge Sensitive Amplifiers (CSA), which transform the charge signal into a differential semi-Gaussian voltage signal, that is then digitized by a 10-bit 10Msamples/s ADC. After the ADC, a digital signal processor allows baseline shifts correction and zero suppression. The data read-out takes place either continuously or triggered at a speed of up to 1.28Gbps by four 320Mb/s e-links. In continuous mode the read-out of a programmable number of samples is performed trigger-less if the input signal exceeds the programmable threshold value.

The CSA shaping time can be configured to operate at 80ns or 160ns, with a sensitivity of 20 or 30mV/fC for the TPC case. Similarly, for the MCH operation the shaping time can be set to 300ns and the sensitivity to 4mV/fC. The maximum amplitude of the output pulse is 2V differential. The power consumption of the analog frontend is 9mW per channel.
The ENC specifications are 540e- at 160ns peaking time, 30mV/fC sensitivity, 18.5pF of detector capacitance, and 950e- at 300ns peaking time, 4mV/fC sensitivity, 40pF of detector capacitance. Non-linearity lower than 1% and cross-talk lower than 0.3% complete the requirements.

Results of the extensive test performed on prototypes from the first ASIC submission will be presented, in comparison with the simulation. The chip performance and specification will be fully discussed.

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