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Versatile prototyping platform for Data Processing Boards for CBM experiment

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The Data Processing Boards (DPB) are an important component of the CBM readout chain.

Before the final, production versions of DPB may be designed, it is important to create a prototyping platform, to test and select appropriate hardware and firmware solutions.

The Kintex based AMC FMC Carrier (AFCK) board is a versatile and open solution fulfilling those requirements, offering configurable high speed (up to 10 Gbps) connectivity.

The paper describes the AFCK hardware, the firmware architecture, and the IP cores developed for different DPB prototyping tasks.
Due to its versatility and openness the AFCK may be reused in other experiments.

Summary

In the CBM experiment the Data Processing Boards (DPB) are the components used in three important subsystems.

As the part of the readout chain, they are receiving data from the front-end electronics (FE) via multiple short distance and lower speed links.
The received data are then preprocessed, concentrated and sent to the first block of the Data Acquisition System (DAQ) -
the First Level Event Selector (FLES) via high-speed long distance links.
In interaction with the Experiment Control System, the DPB boards provide an interface to configure the FE.
Finally, they are connected to the Timing and Flow Control (TFC) system, to ensure
transmission of the reference clock and synchronous commands, necessary to synchronize
the FE, and to transmit the flow control related commands and status messages.

As multiple solutions are possible to implement the described functionalities,
the dedicated, versatile Kintex based AMC FMC Carrier (AFCK) board in MTCA.4 standard was developed to allow verification of possible solutions and selection
of the most appropriate ones.

The AFCK board is based on the XC7K325T FFG900 Kintex chip, and offers 16 Multi Gigabit
Transceivers (MGT) with speed up to 10 Gbps. Due to flexible clocking scheme, various

transmission rates are achievable, and due to availability of the jitter cleaner circuit,
it is possible to produce usable MGT clock from the clock delivered by the MGT receiver.

The MGT signals may be routed to various connectors available in the AFCK board:
the FMC connectors and SATA connectors are available, when working in stand-alone mode,
and additionally MTCA backplane and RTM connectors may be used, when board is placed
in the MTCA crate.

Availability of HPC FMC connectors allows to adjust the board functionality to different
use scenarios, by relatively cheap implementation of specialized FMC boards.
E.g. the dedicated FMC board was developed to allow usage of the AFCK for testing
of the STS-XYTER (readout ASIC) communication protocol.

The AFCK board has been successfully used to implement various IP cores needed for prototyping
of the CBM readout chain like:

- implementation of the tester of the STS XYTER protocol,
- implementation of the White Rabbit core, which is one of possible solutions to distribute timing and synchronization messages,
- implementation of the GBT-FPGA core, which will be used to communicate with FE, implementation of the Ethernet based high speed data transfer protocol.

Additionally the skeletons of firmware for different DPB usage scenarios have been created,
both for testing of other readout and DAQ components and for development of final DPB firmware.

Due to its flexibility and reach resources, the AFCK board may be a good prototyping platform for
data concentration and FE control systems in different experiments.

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