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A High Frame Rate Pixel Chip Design for Synchrotron Radiation Applications

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A hybrid pixel detector working in the single photon counting mode was designed for the High Energy Photon Source (HEPS) in China. The pixel readout chip contains an array of 104 × 72 pixels with a pixel size of 150μm×150μm, each with a counting depth of 20bit. The measurement showed 118e- equivalent noise after bump bonding and non-uniformity less than 55e- after threshold equalization. All functionalities were proved to be normal at a frame rate of 1.2kHz with a dead-time less than 175ns/frame, which are greatly improved compared with the existing pixel system.

Summary

The introduced pixel readout chip was designed for the High Energy Photon Source, which will be the next generation of light source in China. Aiming for diffraction experiments, it works in single photon counting mode in each pixel, coped with a 300um thick PIN sensor through indium bumps. The constant current feedback was set at the feedback loop of the charge amplifier in each pixel, in order to shorten the output width while still keep the noise relatively small, aiming for a higher luminosity without counting saturation. At the meanwhile, a TOT triangle pulse can be thus obtained so as to keep the possibilities for functionality extension. After amplified by a shaper, a discriminator will convert the pulse into digital level, with a 5bit DAC for the threshold trimming. The discriminated pulses will then be counted by a 20bit counter in each pixel.

The readout is not implemented based on the conventional linear feedback shift register, which reuse the counter during readout and thus leading to long dead-time and low frame rate. An independent shift-register chain is taking charge of the readout, while the counter in each pixel can still work, only when a frame synchronization signal is coming, then the counting data will be loaded into the shift chain, and all counters will be reset, following a new round of counting. In this way, a 20MHz readout clock can simply make the frame rate to be more than 1kHz, which is already more than 10 times of the existing pixel system.

Thanks to the independent shift chain, the configuration data for each pixel are also shifted into the array while data readout through the same shift chain, then the latches storing the configuration data in each pixel are refreshed at the frame synchronization pulse. In this way, the SEU events at the latches will never sustain to the next frame, thus also simplifies the design, compared with the conventional triple redundancy scheme.

The chip contains an array of 104×72 pixels with a pixel size of 150um×150um. It is designed with SMIC 0.13um technology, and a single-sized sensor was bump-bonded with the ASIC as the prototype. All the three key processes, including ASIC, sensor production and indium bonding, were fully done within China mainland.

The bare die test on ATE showed a yield of 60%. All qualified dies were measured with total power dissipation less than 280mW, or 37.3uW for every pixel. The bonded prototype was measured with X-ray tube and the synchrotron light. The measurement results showed an equivalent noise of 118e- after bump bonding and non-uniformity less than 55e- after threshold equalization. A non-saturation counting rate more than 1.5MHz was observed for each pixel. All functionalities were proved to be normal running at the system clock frequency of 20MHz, guaranteeing a frame rate of 1.2kHz and a deadtime less than 175ns/frame, which are greatly improved compared with the existing pixel system.

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