# Development of a sub-nanosecond time-to-digital converter based on field-programmable gate array

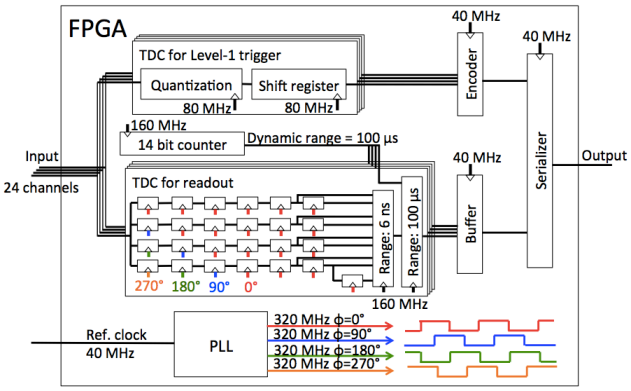
Yuta Sano,[1] Makoto Tomoto,[1] Yasuyuki Horii,[1] Osamu Sasaki,[2] Tomohisa Uchida,[2] and Masahiro Ikeno[2]
[1]Nagoya University, Nagoya
[2]High Energy Accelerator Research Organization (KEK), Tsukuba

## 1. Introduction

The High-Luminosity LHC is expected to begin operations in 2026, with a nominal leveled instantaneous luminosity of 5 x $10^{34}$ $cm^{-2}s^{-1}$. The present time-to-digital converter (TDC) chips for the monitored drift tube chambers at the ATLAS experiment will be replaced by new ones to fully exploit the rate capabilities at Level-1 trigger rates beyond 200 kHz and Level-1 latencies beyond 30 μs [1].
In this study, TDC based on field-programmable gate array (FPGA) is developed, and the performance is evaluated.

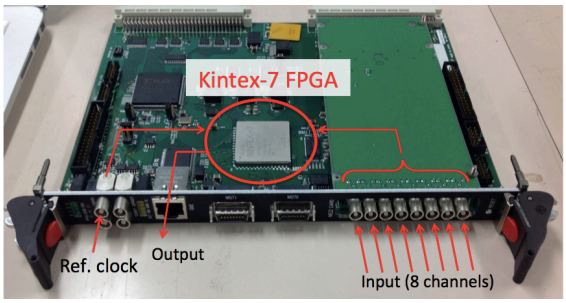
## 2. Block diagram of TDC

- TDC for readout: 0.78 ns binning, multi-sampling scheme using quad-phase clocks.
- TDC for Level-1 trigger: 12.5 ns binning.
- Reference clock with frequency of 40 MHz.




## 3. Demonstrator

The TDC is implemented in Xilinx Kintex-7 FPGA.
Test is performed with reference clock frequency of 40-110 MHz, which provides useful information about capabilities of TDC development using FPGA.




## 4. Parameters evaluated in this study

- Differential nonlinearity (DNL)

$$\mathrm{DNL}_i[\mathrm{LSB}] = \frac{T_i - T_{\mathrm{LSB}}}{T_{\mathrm{LSB}}} \quad (i:\ \mathrm{Count})$$

$T_{LSB}$: ideal time binning, $T_i$: measured time binning

- Integral nonlinearity (INL)

$$\mathrm{INL}[\mathrm{LSB}] = \frac{\langle T_{\mathrm{measured}} \rangle - T_{\mathrm{ideal}}}{T_{\mathrm{LSB}}} \qquad T_{\mathrm{ideal}} >> T_{\mathrm{LSB}} \text{ assumed}$$

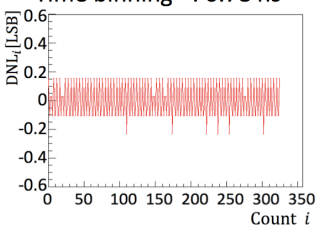
$T_{ideal}$: ideal time, $\langle T_{measured} \rangle$: mean of measured time

## 5. Linearity measurements

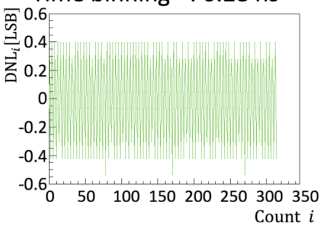
Linearity measurements for the TDC for readout are reported.

- DNL

Ref. clock : 40 MHz
Time binning : 0.78 ns

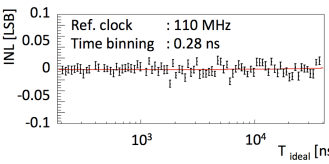



Ref. clock : 110 MHz
Time binning : 0.28 ns




Measured $DNL_i$ is < 0.5 LSB for all counts up to ~300.
Performance is affected by the time differences between signal paths, which are 100-200 ps in the demonstrator.

- INL



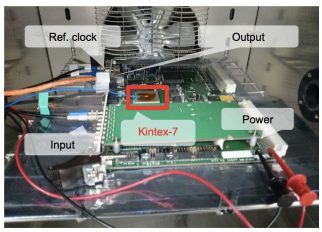

Results of fitting with y=Ax+B

| Ref. clock | A | B |
|---|---|---|
| 40MHz | (0.7±2.5)×10$^{-8}$ | (-3.5 ± 7.5)×10$^{-4}$ |
| 110MHz | (-6.9±7.3)×10$^{-8}$ | (-1.6 ± 0.9)×10$^{-3}$ |

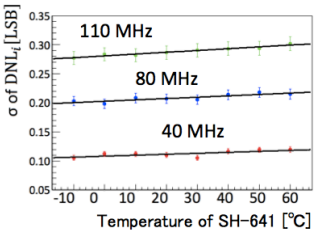
Measured INL is consistent with zero up to 100 μs.

## 6. Temperature dependence

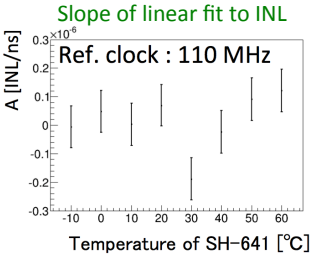
Temperature dependence on the linearity is evaluated using thermostat chamber ESPEC SH-641.




Standard deviation of DNL




Slope of linear fit to INL




Temperature dependence is obtained to be small for both DNL and INL from -10 deg C to 60 deg C.

## 7. Conclusion

A sub-nanosecond time-to-digital convertor has been developed based on Xilinx Kintex-7 FPGA. The differential/integral nonlinearity is measured to be small in -10-60 deg C for the time binning of 0.78-0.28 ns.

## Reference

[1] ATLAS Collaboration, "Letter of Intent for the Phase-II Upgrade of the ATLAS Experiment," CERN-2012-022, LHCC-I-023, https://cds.cern.ch/record/1502664.