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Development of a sub-nanosecond time-to-digital converter based on field-programmable gate array

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We present the design and the performance of a 24 channel time-to-digital converter with a variable time binning of down to 0.39 nsec based on a Xilinx Kintex-7 field-programmable gate array. The time measurement is provided by a multisampling scheme with quad phase clocks synchronized with external reference clock. The differential and integral nonlinearities have been measured to be less than the half of the time binning. The obtained performance of the time measurement is sufficiently high for various detectors in high energy physics, e.g. the monitored drift tube chambers at the ATLAS experiment.

Summary

Time-to-digital converters (TDCs) are largely used at the experiments in high energy physics. For example, the monitored drift tube chambers at the ATLAS experiment provide a muon momentum measurement based on TDCs implemented in application-specific integrated circuits which have a time binning of 0.78 nsec. Recent moderate field-programmable gate arrays (FPGAs) enable an implementation of sub-nanosecond TDCs, providing a flexibility of the modification during experiments. In this study, we have developed a 24 channel TDC with a variable time binning of down to 0.39 nsec on a Xilinx Kintex-7 FPGA.

The 24 channel TDC is designed to measure the timing of both the leading and trailing edges of the input signal. The time measurement is based on free-running counters with a variable frequency of up to 2.6 GHz. The counters are designed by a multisampling scheme with quad phase clocks, each of which has a frequency of one fourth of the one of counters. The quad phase clocks are produced from an external reference clock using highly reliable phase-locked loop circuit implemented in the Xilinx Kintex-7 FPGA. An external clock of 80 MHz (40 MHz) corresponds to the time binning of TDC of 0.39 nsec (0.78 nsec). The values of the counters are transferred to the ring buffer block and are stored.

The differential nonlinearity could generally be affected by the variation of the delays between different signal and clock paths. For the TDC implemented in this study, the root mean square of the differential nonlinearity is measured to be less than the half of the time difference between the neighboring lowest significant bits. The root mean square of the integral nonlinearity is also measured to be less than that. No significant difference has been observed in the measurements between the leading and trailing edges. Similar results have been obtained between 24 channels. The dependence on the temperature and the supply voltage has also been measured.

In conclusion, we have developed a 24 channel TDC with a variable time binning of down to 0.39 nsec on a Xilinx Kintex-7 FPGA. The time measurement is based on a multisampling scheme with highly reliable clocks synchronized with an external reference clock. The differential and integral nonlinearities have been measured to be less than the half of the time binning. The obtained performance of the time measurement is sufficiently high for various detectors of the experiments in high energy physics. This work encourages the implementation of multi-channel sub-nanosecond TDCs in the FPGAs with high radiation tolerance for the use in the environment with high particle rate.

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