Trigger and readout electronics for the STEREO experiment.

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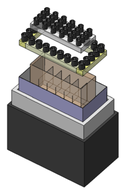
Overview

STEREO experiment

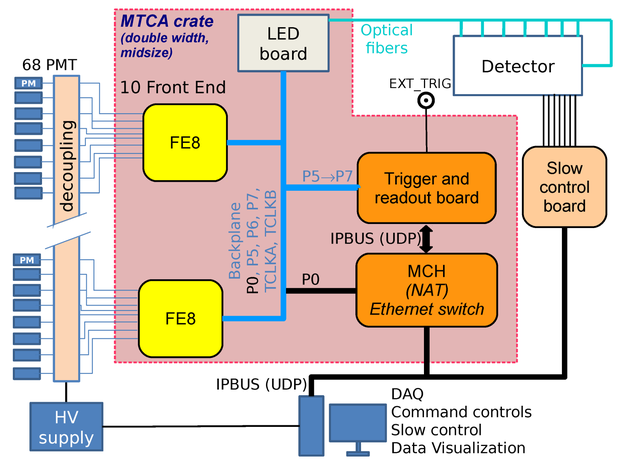
- STEREO experiment is a search for a sterile neutrino (dimension: $3m \times 1m \times 1.5m$)
- Measures the anti-neutrino energy spectrum as a function of the distance from the source (ILL nuclear reactor).



General requirements

- Monitor 68 channels, trigger required in 3 classes:
  - 24 PMT for target (gadolinium-loaded liquid scintillator)
  - 24 PMT for Gamma catcher (liquid scintillator)
  - 20 PMT for muon veto (Cerenkov detector)
- Withstand a **mean** first level trigger rate of 1 kHz
- Have no dead-time (pile-up excepted)
- Manage various trigger schemes and conditions (coincidence and anti-coincidence)
- Process signals on board: compute $\mathbf{Q_{tot}}$ and $\mathbf{Q_{tail}}$ for *Pulse Shape discrimination (PSD)*

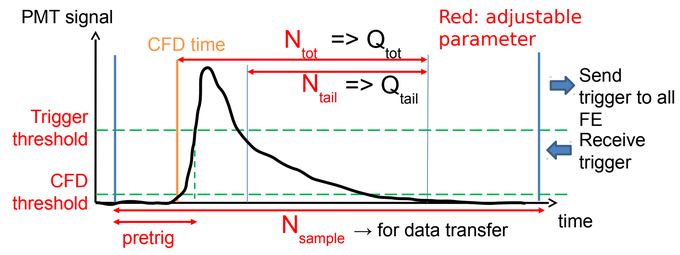
Electronics



- Trigger board used for: triggering, FE readout and LED control
- Communication FE ↔ Trig Board with custom protocol
- Readout and slow control via IPBus (Secured UDP from CERN)

Required first level triggering and processing

1. FE emits a trigger when at least one PMT signal > trig threshold
2. Confirmed trigger (by trig board) reception initiate PSD processing



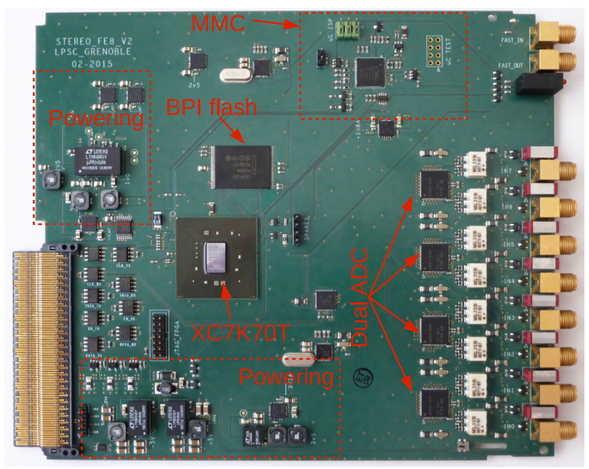
- Beginning of signal is to be found with a *Constant Fraction Discriminator (CFD)* having its own threshold (above noise)
- Adjustable parameters defined prior to run
- $\mathbf{N_{tot}}$ represents typical pulse duration
- $\mathbf{N_{sample}}$ time window for analysis and samples to record in debug mode
- $\mathbf{N_{tail}}$ is the signal integration duration for PSD

Front-end 8 (FE8)

Specifications

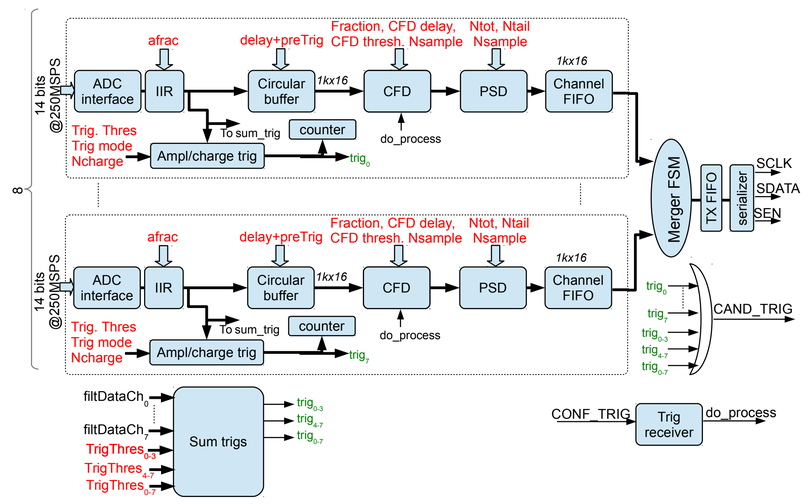
- 8 channels board (14 bit ADC @250 MSPS, dyn. range 2.0 V)
- Readout by custom serial protocol, slow control by IPBus
- Preamplifier with 2 selectable gains, e.g x1 and x20
- The ADC input feature anti-aliasing filter (80 MHz)
- First level trigger on amplitude OR charge, selectable by mask :
  - Individual channel
  - sum of first 4 channels
  - sum of last 4 channels
  - sum of 8 channels
- Trigger bit inserted in the data flow
- Each channel has a high pass IIR to suppress pedestal
- Scalers for individual PMT monitoring
- Each channel CFD and PSD $\mathbf{Q_{tot}}$ and $\mathbf{Q_{tail}}$ computed on board
- Transfer of $\mathbf{Q_{tot}} \times \mathbf{8}$, $\mathbf{Q_{tail}} \times \mathbf{8}$, zero crossing $\times \mathbf{8}$
- Optional debug mode to readout the $\mathbf{N_{samples}}$ used to compute CFD and PSD

Hardware



- Main FPGA: XC7K70-2TFBG676,
- ADC: Texas Instrument ADS42LB49 (AC coupled, f_c >30 kHz)
- Improved IPbus (DHCP, flash programming)

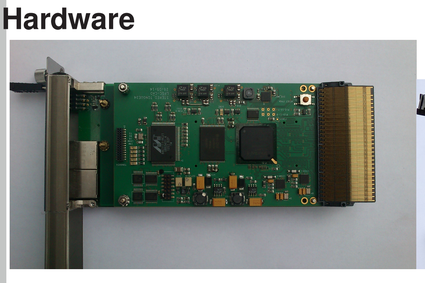
Firmware

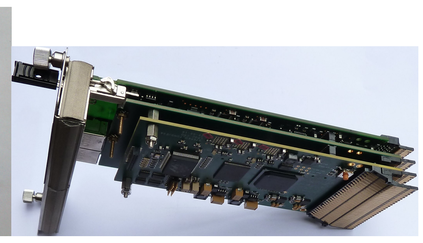


- Parameters are in red
- Pipelined processing: $\mathbf{1^{st}}$ CFD, then PSD, then data concentrated and finally serialized

Trigger and readout (TRB)

Hardware



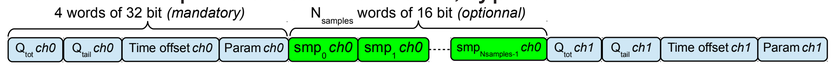


NAT-MCH and custom extensions (2 boards)

- T1: NAT-MCH featuring an Ethernet switch
- T2: Clock trees (FCLKA, TCLKA), clock reception (TCLKB)
- T3: Main board with FPGA (XC6SLX45T-FGG484), power, Ethernet (GTP and spare phy)
- T4: Fast SMA inputs, RJ45 (spare Ethernet, LED box control)

Link FE8 ↔ trigger mezz. board

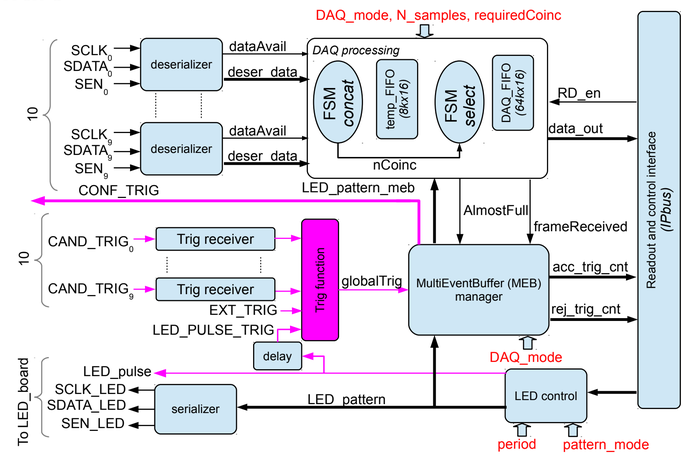
- Serial data link + trigger link, 5 signals:
  - SDATA : OUT (FE), IN (Trig board)
  - SEN : OUT (FE), IN (Trig board)
  - SCLK : OUT (FE), IN (Trig board)
  - CANDIDATE_TRIG : OUT (FE), IN (Trig board)
  - CONFIRMED_TRIG : IN (FE), OUT (Trig board)
- Serial link operated at 125 Mbit/s, typical frame content:



- In normal mode, rate limited at 125MHz/(4x32x8)=122 kHz.
- In debug mode, rate limited at 13.5 kHz (worst case, 64 samples).
- Trigger path at 250 MHz (to be sample accurate)

⇒ Delay from candidate trigger to confirmed trigger, a **circular buffer** is used for compensation in the front-end (about 120 ns or 30 samples)

Firmware



- MEB is implemented: up to 84 (normal)/6 (debug) consecutive triggers can be accepted (if separated by *N_samples* x 4 ns)
- Low level and high level trig function(s) can evolve.
- In calibration mode (LED) several pattern sequences are possible.

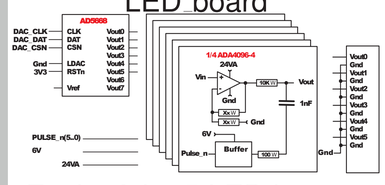
LED board

Requirements

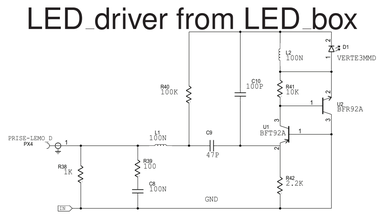
- LED is used to calibrate the detector.
- LED light is injected in the detector by optical fibers.

LED box driver and led box

LED_box_driver from LED_board

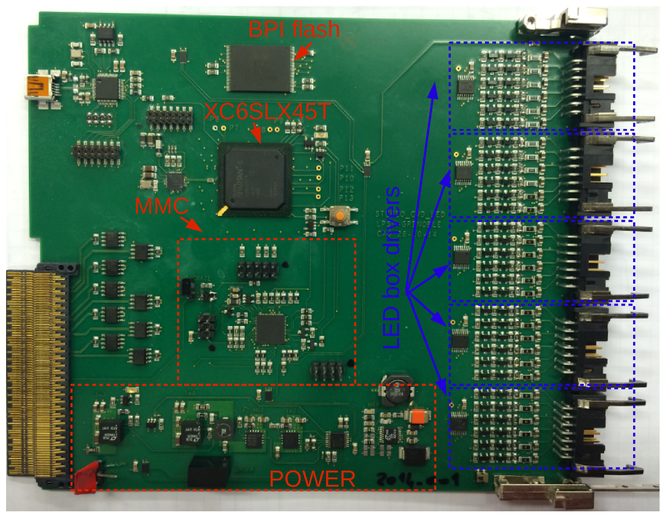


LED_driver from LED_box



- Each of the 5 LED box contains 6 LED and a discrete LED driver.
- LED light driver supplied and driven via a single coax cable:
  1. LED light level set by mean voltage (DAC setting via IPBus)
  2. Square pulse > **2 *V*** fires the LED (generated by FPGA)

Hardware



- Control by IPBus (LED voltage level and BPI programming)
- LED pattern and timing are selected/driven by the TRB.

MTCA port allocation

Ports allocation for slot 1-10 (containing FE8)

- Port 0: for IPbus (Ethernet)
- Port 5-7, trigger and acq serial protocol :
  - Port 5: unidirectional serial data FE8→MCH (125 Mbps)
  - Port 6: unidirectional serial enable FE8→MCH
  - Port 7: bidir, candidate trigger FE8→MCH, confirmed trigger to MCH→FE8 (4 ns pulses)
- TCLKB: used as serial link reference clock to MCH.
- TCLKA: system reference clock

Ports allocation for slot 11-12 (containing LED_board)

- Port 0: for IPbus (Ethernet)
- Port 5-7:
  - Port 5: unidirectional serial data MCH→LED_board (125 Mbps)
  - Port 6: unidirectional serial enable MCH→LED_board
  - Port 7: unidirectional LED pulse MCH→LED_board (4 ns pulses)
- FCLKB: used as LED serial link reference clock to LED_boards
- TCLKA: system reference clock