Contribution ID: **4** Type: **Poster**

Trigger and readout electronics for the STEREO experiment.

Tuesday, 29 September 2015 16:53 (1 minute)

The STEREO experiment will search for a sterile neutrino by measuring the anti-neutrino energy spectrum as a function of the distance from the source, the ILL nuclear reactor.
A dedicated electronic, hosted in a single µTCA crate, was designed for this experiment. It performs triggering in two stages with various selectable conditions, processing and readout via UDP/IPBUS on 68 photomultiplier signals continuously digitized at 250 MSPS. Additionally, for detector performance monitoring, the electronics allow online calibration by driving LED synchronously with the data acquisition.
This paper will describe the electronics requirements, architecture and the performances achieved.

Summary

The STEREO experiment will search for a sterile neutrino by measuring the anti-neutrino energy spectrum as a function of the distance from the source, the ILL nuclear reactor. A dedicated electronic, hosted in a single µTCA crate, was designed for this experiment. It serves several purposes : triggering, processing, readout and on-line calibration.

For the first purpose, 68 photomultiplier signals provided by the detector are continuously digitized at 250MSPS by 10 8-channels front-end electronics (FE8). Using the digitized signals, each FE8 can generate a candidate trigger (or a veto) that is used by the trigger and readout mezzanine boards (TRB) installed on a commercial MCH from NAT to build, depending on the selected trigger conditions, a first level accepted trigger (L1a). The TRB also provides the system clock (250MHz) to all AMC. The trigger signals are transported by the port 7 and the reference clock by TCLKA of the µTCA backplane.

Upon L1a reception, the FE8 perform signal processing on a tunable time frame, defined in number of samples (Nsample, up to 64). Each channel data frame is analyzed to determine the time of the threshold crossing with digital constant fraction discriminator (CFD), the CFD threshold being usually significantly lower than the trigger threshold. The CFD parameters (delay, fraction, threshold) can be adjusted channel by channel. The times found are used as parameters for dual digital integrators that compute the pulse total and the pulse tail charges to allow Pulse Shape Discrimination (PSD). The total charge integrator being started at the beginning of the pulse total charge (Qtot) and of the tail charge (Qtail) after a tunable number of samples. As previously, the two sample count parameters (Ntot/Ntail) for total/tail charge can be adjusted. The CFD and PSD processing are done in a pipeline, hence no dead time is generated by these processing and every Nsample clock cycles a new trigger can be fired.
Finally, the data are sent by each FE8 to the TRB via a custom serial protocol carried by the µTCA backplane (port 5,6 and TCLKB). The TRB performs a second level selection (coincidence, charge selection, ⋯) before writing the event in the output buffer. It must be noticed that for verification purpose, the original Nsamples samples used for the processing can be read-out along with the event data (Qtot, Qtail, CFD results) for validation and debugging purpose. After triggering and processing, the event readout rate for the whole detector is required to be higher than 1 kHz.

A LED control board (LCB) able to control 5 boxes of 6 LED is inserted in the µTCA crate, the generation of LED flashes is controlled directly by the TRB via the backplane (port 7). The LED pattern applied on each generated trigger is recorded along with the corresponding event. By regularly performing LED runs, the

detector performance can be monitored in time. The LED pattern for each box and each LED voltage can be adjusted.

For control and readout, the TRB, FE and LCB are accessed by a rewritten version of IPBUS featuring a DHCP capability to allow for an easier experiment setup. The IPBUS communication also carried by the μTCA backplane (port 0), allows to withstand a readout rate higher than 4 kHz, which is sufficient for the experiment requirement. Finally, it must be noted that each FPGA carried by these electronic boards are programmed at startup by an associated flash memory via Boot Parallel Interface, and that their contents can be updated via IPBUS, hence allowing fast field firmware upgrades.

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Session Classification: Poster

Track Classification: Systems