Topical Workshop on Electronics for Particle Physics TWEPP-2015. Lisbon, Portugal, 28 September – 2 October, 2015

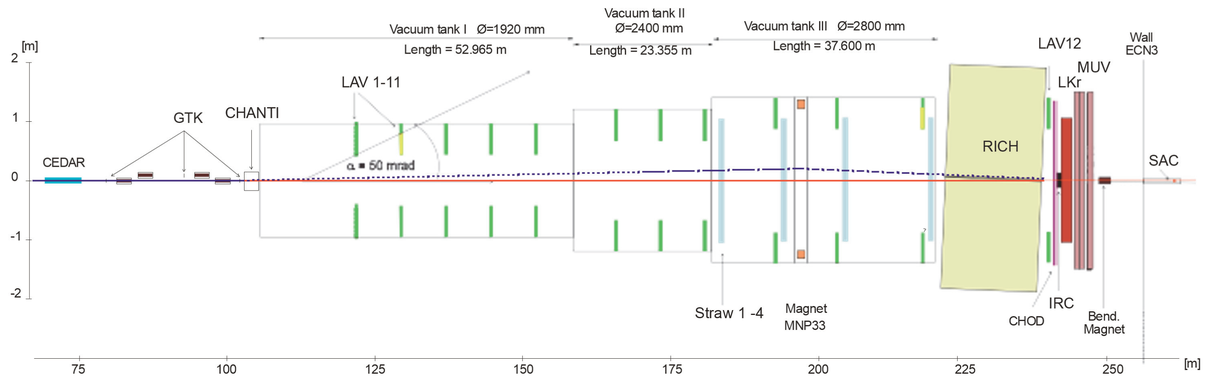
NA62 Liquid Krypton Calorimeter Readout System

Augusto Ceccucci[a], Riccardo Fantechi[a,b], Philippe Farthouat[a] , Nicola De Simone[a], *Vladimir Ryjov*[a]*, Stefano Venditti[a]

[a]CERN, Geneva, Switzerland, [b]INFN sez. Di Pisa, Pisa, Italy

NA62 Experiment

The NA62 experiment [1] is focused on precision tests of the Standard Model via studies of ultra-rare decays of charged kaons. The system is composed of several detectors.



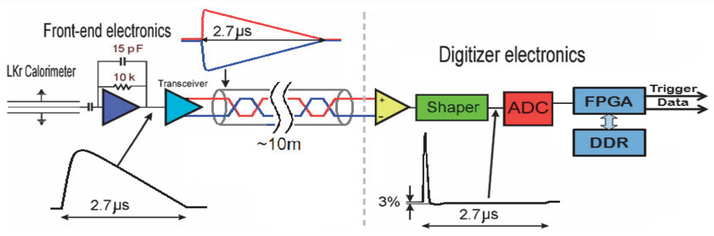
The high resolution Liquid Krypton (LKr) calorimeter of the former NA48 experiment [2], together with other detectors, provides a photon-veto with hermetic coverage from zero out to large angles from the decay region.

The study of an upgraded LKr readout system began in 2009.

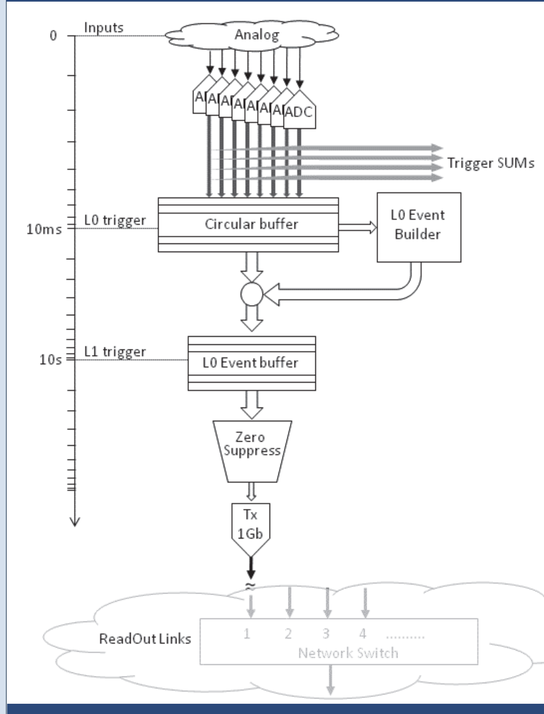
LKr calorimeter readout electronics

The calorimeter: ~10 m^3 of liquid krypton at 120 K -> 13248 readout cells (2×2cm^2).

- **Preamplifiers – in the cryostat;**
- **Transceivers – on the feed-throughs;**
- **BackEnd – 4m away (10m cables).**



Calorimeter REAdout Module (CREAM) processing flow

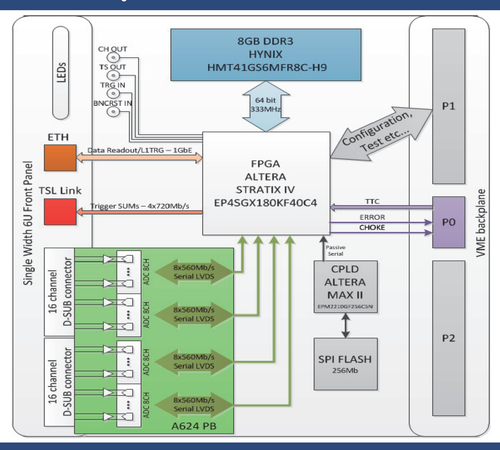


CREAM is 6U VME64x module, its data processing flow with multiple levels of triggering is illustrated here and can be summarised as follows:

- **32 analog inputs, after proper shaping, are continuously digitised by a 14-bit ADC at 40MHz;**
- **Trigger sums are continuously formed in digital form and sent to the L0 trigger logic;**
- **One 8 GB SODIMM module is shared by two-level data storage buffers:**
  - **data are continuously written in a circular buffer waiting for the L0 decision;**
  - **when the CREAM receives a L0 trigger signal, the related data (i.e. the data stored a fixed latency time before L0) are extracted from the circular buffer and stored into another buffer called L0 event buffer, waiting for a possible L1 trigger;**
- **Upon receipt of a L1 trigger, the corresponding data are sent to a PC farm through a gigabit Ethernet port.**

CREAM main components and parameters

- **FPGA - Altera Stratix-IV EP4SGX180KF40C4**
- **Memory – 8GB DDR3 SODIMM HMT41GS6MFR8C-H9**
- **ADC – Analog Devices, AD9257 octal, 14-bit, 50 MSPS**
- **Default Sampling Frequency 40.08 MHz**
- **Resolution 14 bit**
- **Differential Nonlinearity (DNL) ≤ 2 LSB**
- **Integral Nonlinearity (INL) ≤ 5 LSB**
- **Inter-Channel Crosstalk ≤ -70 dB**
- **Signal-to-Noise Ratio (SNR), fin = 5MHz ≥ 63 dB**
- **Effective Number Of Bits (ENOB), fin = 5MHz ≥ 10 bit**
- **Non-coherent noise < 2 LSB**
- **Coherent/non-coherent noise ratio < 10 %**

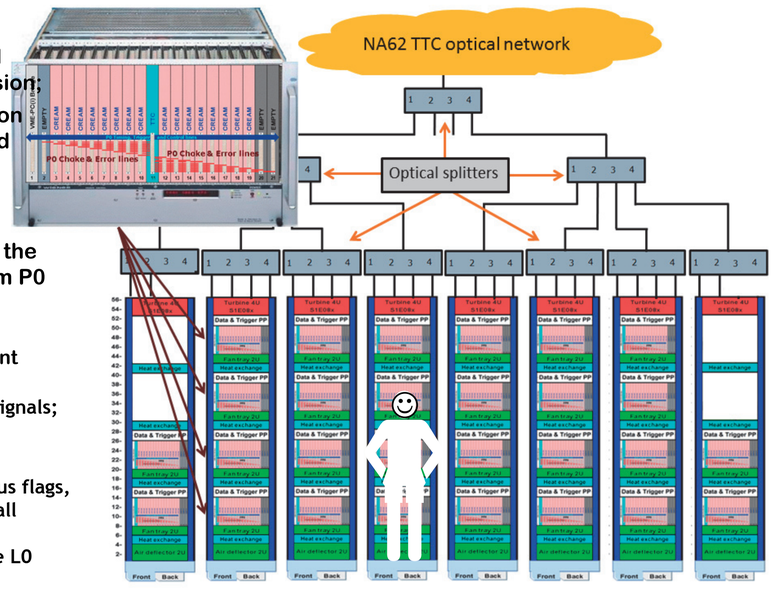


LKr Timing Trigger and Control (TTC) distribution

The data taking sequence is entirely driven by the TTC system that was developed for the LHC experiments and is used by all NA62 sub-detectors.

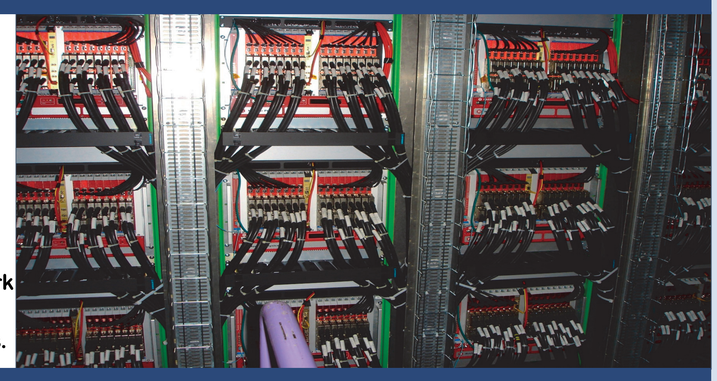
The LKr-specific TTC-LKr module receives all timing signals via optical distribution network, converts, decodes and delivers these signals to the calorimeter data acquisition electronics by means of a custom P0 backplane.

- **6U VME64x module**
- **Unidirectional optical fibre based transmission;**
- **160 Mbps Time Division Multiplexed (TDM) and Bi-Phase Mark (BPM) encoded channels;**
- **One TTC-LKr module serves all CREAMs in the same crate via custom P0 backplane:**
  - **crate ID number;**
  - **40.08 MHz Experiment reference clock;**
  - **SPS Cycle and Burst signals;**
  - **L0 trigger;**
  - **trigger type;**
  - **collects memory status flags, Choke & Error, from all active modules and transmits them to the L0 trigger processor.**



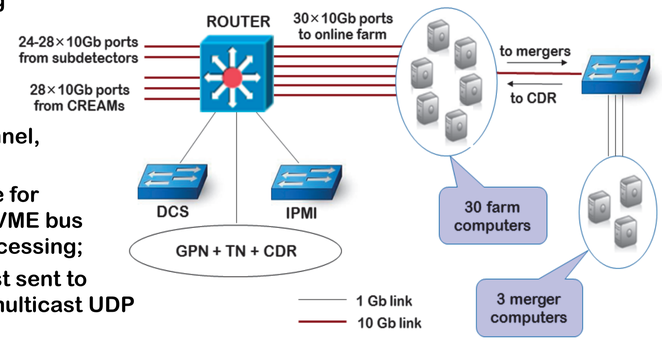
Complete LKr Back-End electronics

- **14 thousand 14-bit ADC acquisition channels;**
- **432 32-channel Calorimeter REAdout Module digitisers (CREAM);**
- **28 TTC-LKr interfaces – one per readout crate;**
- **10 TTC optical splitters;**
- **28 6U VME64 readout crates;**
- **28 24×1Gbit/2×10Gbit HP-2920-24G network routers – one per readout crate;**
- **All hardware is arranged in eight 58U racks.**



LKr data flow

- **Acquisition mode is started by setting the Run Start/Stop bit in one of the CR/CSR;**
- **Data streams from all enabled inputs are stored in the circular buffer;**
- **Depth of this buffer must be sufficient to cover max L0 trigger latency (10ms = 800kB/Ch);**
- **Upon receipt of the L0 signal, the corresponding data samples are extracted from the circular buffer and stored in the L0 event buffer;**
- **L0 event buffer is able to accommodate a 1MHz L0 average rate during 10s when 8 samples per L0 event are kept - this requires 160MB per channel, 8GB DDR3 SODIMM per board (32 channels);**
- **Events written in the L0 buffer, become available for readout via the Gigabit Ethernet link and/or the VME bus interface, with an optional zero suppression processing;**
- **Data readout is initiated by the L1 trigger request sent to the CREAMs through the Ethernet interface as multicast UDP protocol packets;**
- **Data packets are addressed to the requesting PC by automatically retrieving its IP in the request packet.**



The LKr readout network and PC farms layout

Header	0x24			Event number			
	Reserved			Event length			
	Timestamp						
	Reserved				Source-ID		
					CrateID[5:0]		GA[4:0]
Event data	Detector data						
Bit	31	24	23	16	15	8	7 0

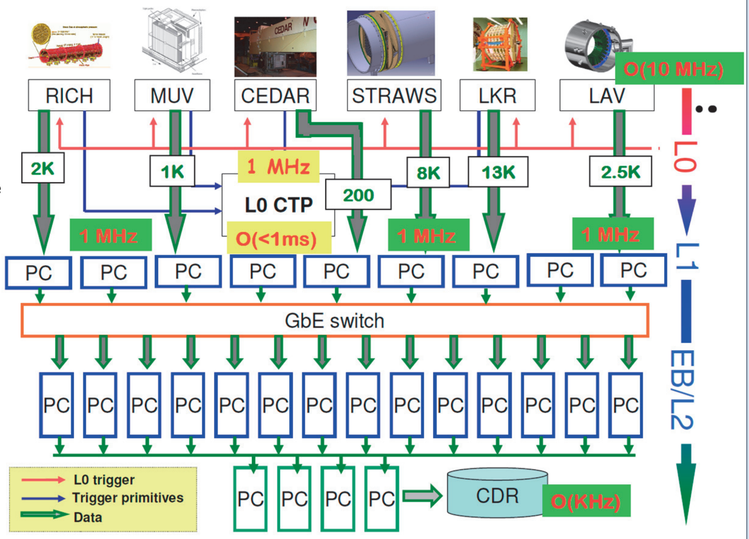
The L1 Event and detector data formats

L Z	#Samples	Data length
Ch0 sample 1		Ch0 sample 0
Ch0 sample 3		Ch0 sample 2
Ch0 sample 5		Ch0 sample 4
Ch0 sample 7		Ch0 sample 6
Ch1 sample 1		Ch1 sample 0
----------		----------
Ch31 sample 7		Ch31 sample 6
Checksum		
31 24	23 16	15 8 7 0

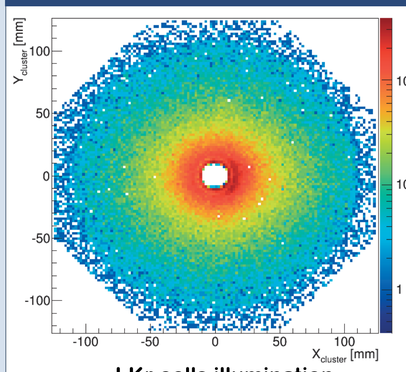
Experiment Trigger-DAQ system

The NA62 TDAQ system is based on 3 trigger levels

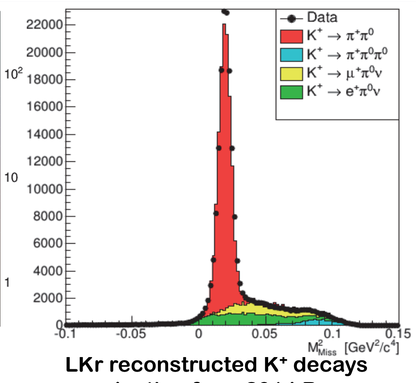
- **L0: based on "trigger primitives" from a configurable number of detectors**
  - **fixed latency (~1 ms);**
  - **FPGA based;**
  - **L0 Trigger Processor (L0TP) receives the primitives and generates the L0 signal;**
  - **Reduction factor: 10 MHz →1 MHz;**
- **L1: data from most detectors acquired by L1 PCs and used to take the L1 decision**
  - **Whole event analysed by L1 PCs;**
  - **LKr data not sent @ L1 level;**
  - **Max latency: ~1 s;**
  - **Reduction factor: 1 MHz →100 KHz;**
- **L2: final decision taken with data from all detectors**
  - **Max latency ~ spill length (up to 10 s);**
  - **Reduction factor: 100 KHz →20 KHz.**



Status



LKr cells illumination 2014 Run



LKr reconstructed K⁺ decays selection from 2014 Run

- **2009-2010 → LKr BackEnd requirements and architecture definition;**
- **2010 → new digitiser - CREAM specification;**
- **2011 → CREAM development and production tender and contract award to CAEN;**
- **2012-2013 → TTC-LKr design and production at CERN;**
- **2013 → CREAM prototype delivery and thorough characterisation;**
- **2013-2014 → LKr BackEnd infrastructure installation;**
- **Spring 2014 → CREAM production delivery – 440 pcs;**
- **Summer 2014 → LKr BackEnd deployment - commissioning;**
- **Fall 2014 → NA62 Pilot Run at 5% of nominal intensity;**
- **Summer/Autumn 2015 → NA62 data-taking at nominal intensity.**

References

[1] NA62 Technical Design, *http://na62.web.cern.ch/NA62/Documents/TD_Full_doc_v10.pdf*.

[2] NA48 Collaboration (V. Fanti *et al.*), *The Beam and detector for the NA48 neutral kaon CP violations experiment at CERN,* Nucl.Instrum.Meth. A574 (2007) 433-471.