



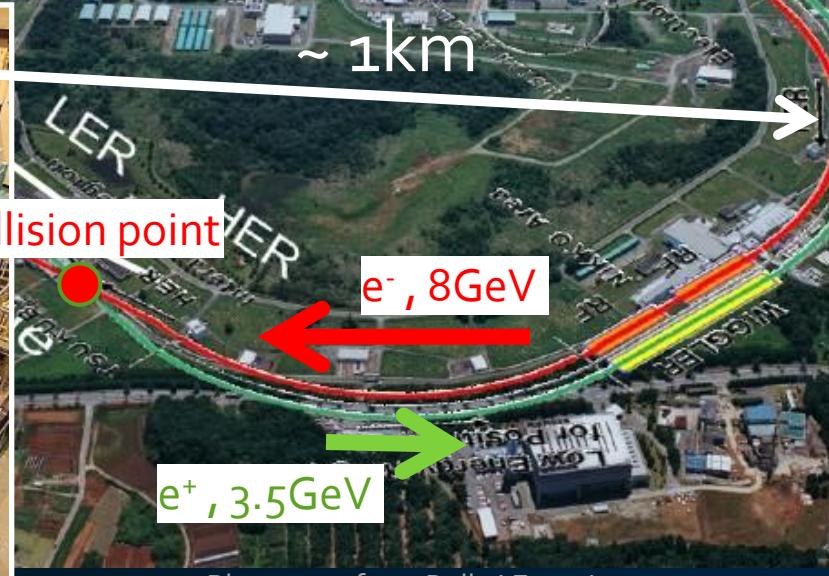
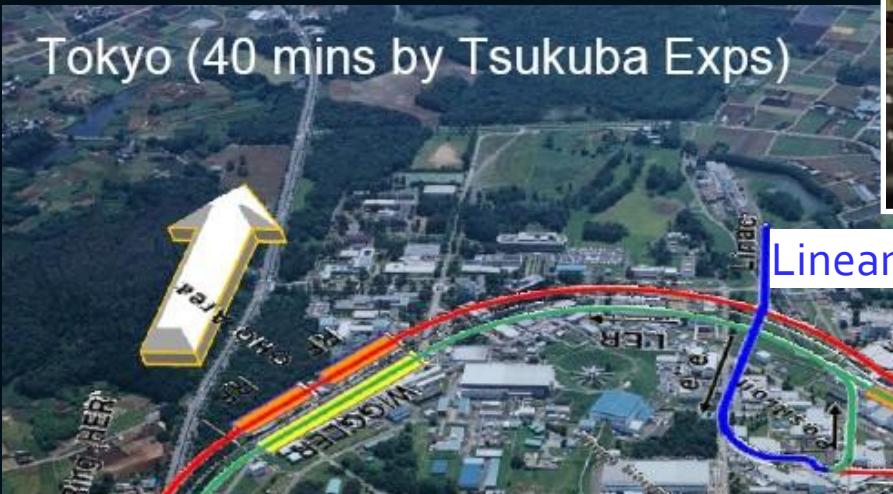
TWEPP-15 Lisbon,
2015-09-29

EMC Studies for the Vertex Detector of the Belle II Experiment

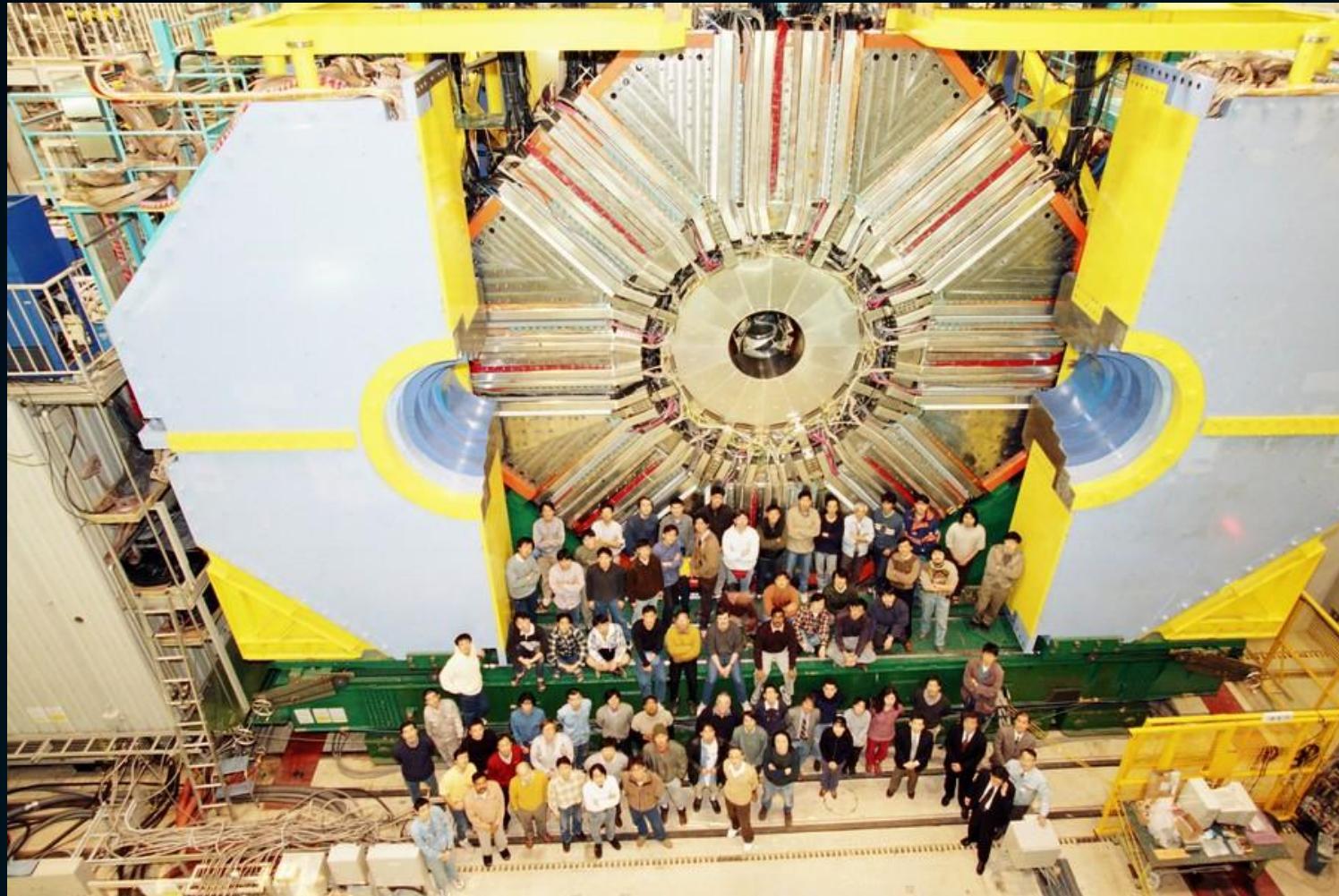
Richard Thalmeier (HEPHY Vienna)

- **Belle II - Introduction**
- **SVD EMC Tests**
- **PXD Power Cable Studies**
- **Conclusions and Outlook**

Future Belle II @ KEK

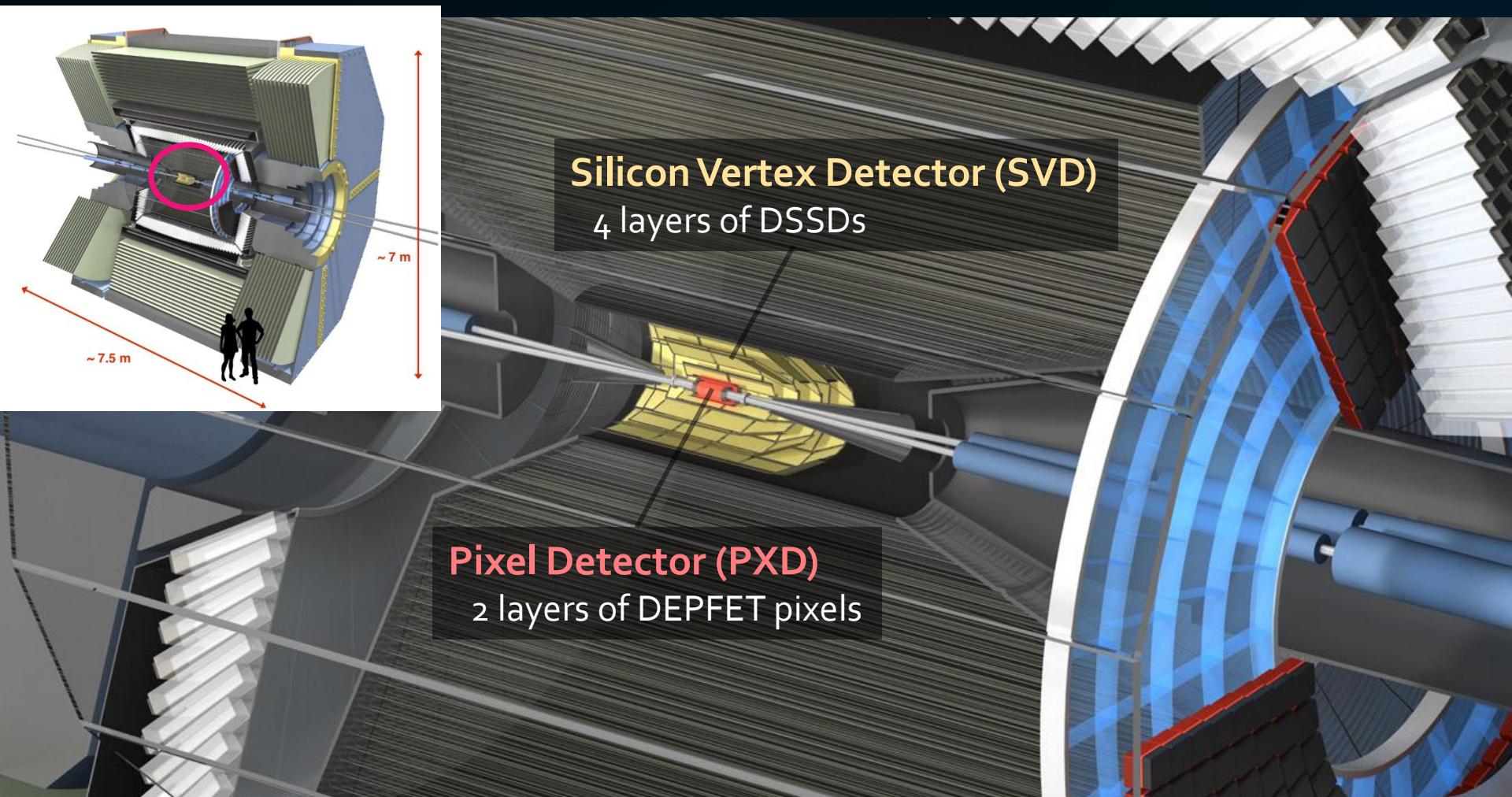


The Belle I Detector (Collision point)



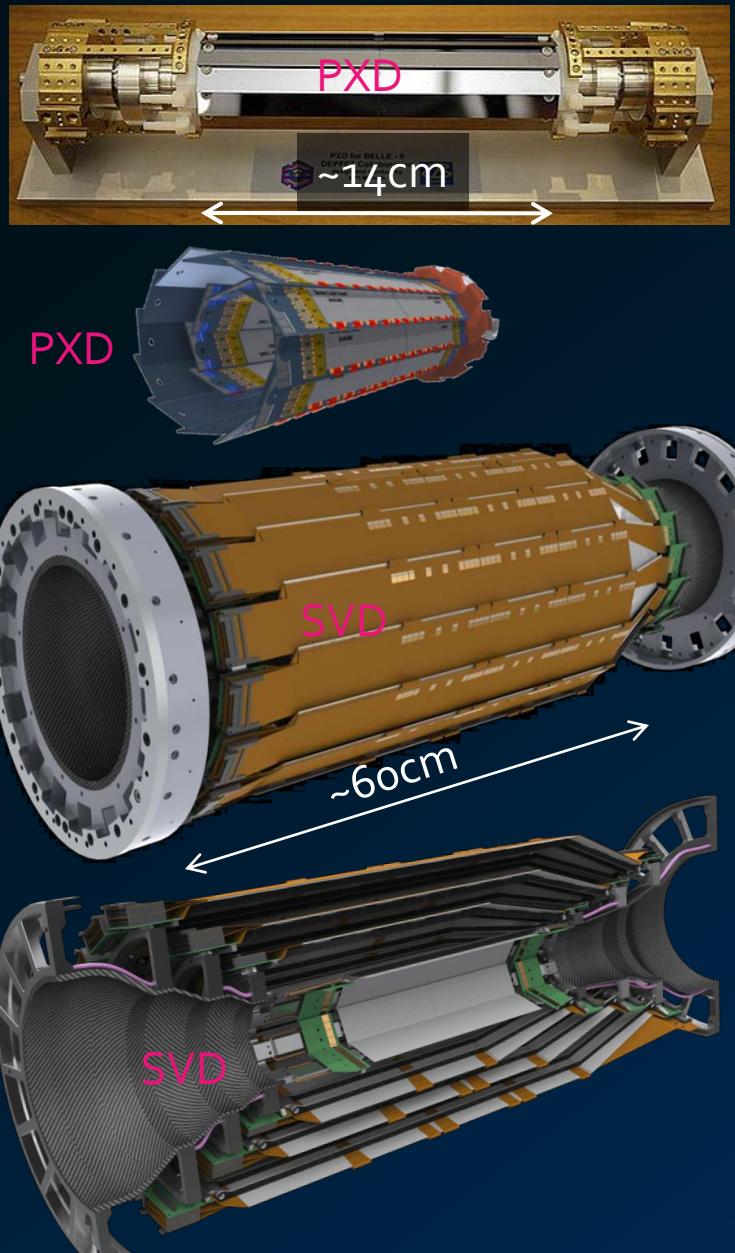
- ~7m high,
- ~10m long,
- ~1500 tons

Belle II Vertex Detector VXD = PXD + SVD



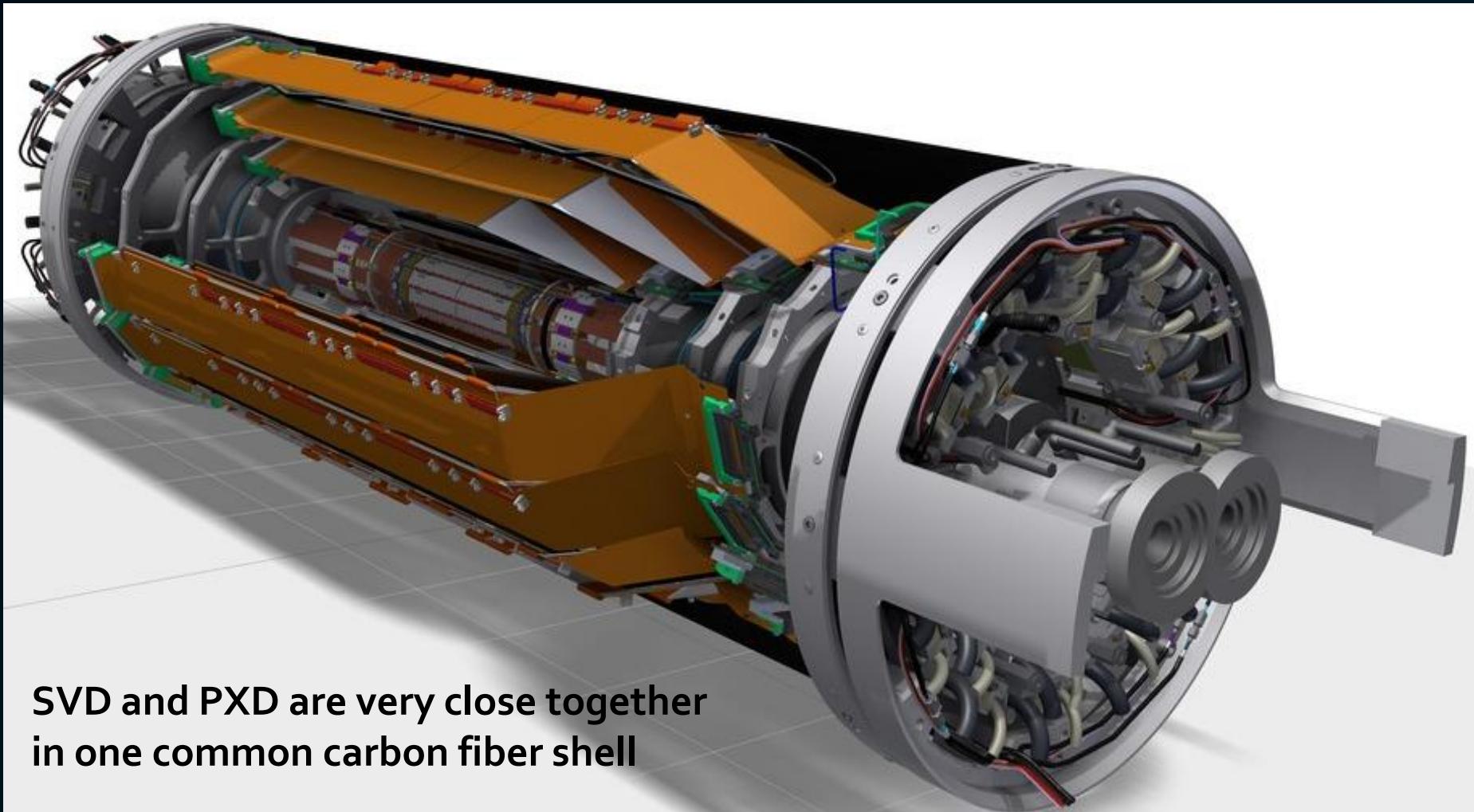
Belle II Vertex Detector

- **Pixel Detector (PXD)**
 - 8M pixels
 - 2 layers at $r = 14, 22$ mm
 - Excellent spatial resolution ($\sim 15 \mu\text{m}$)
 - Coarse time resolution ($20 \mu\text{s}$)
- **Silicon Vertex Detector (SVD)**
 - 4 layers DSSD at $r = 38, 80, 104, 135$ mm
 - Good resolution: ~ 12 (p) and 25 (n) μm ,
but ambiguities due to ghosting
 - Excellent time resolution (~ 3 ns)



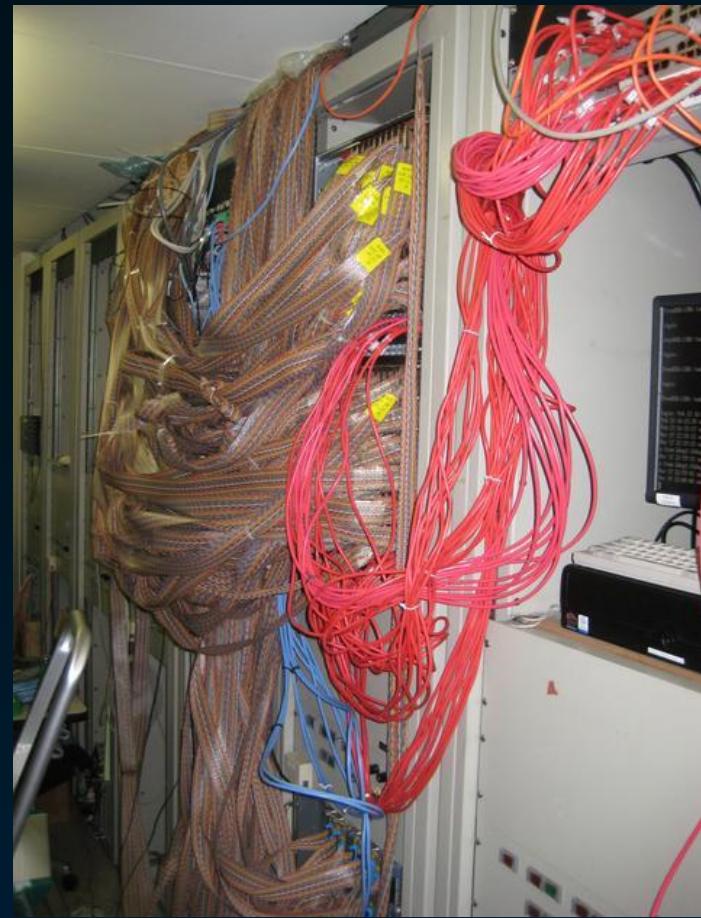
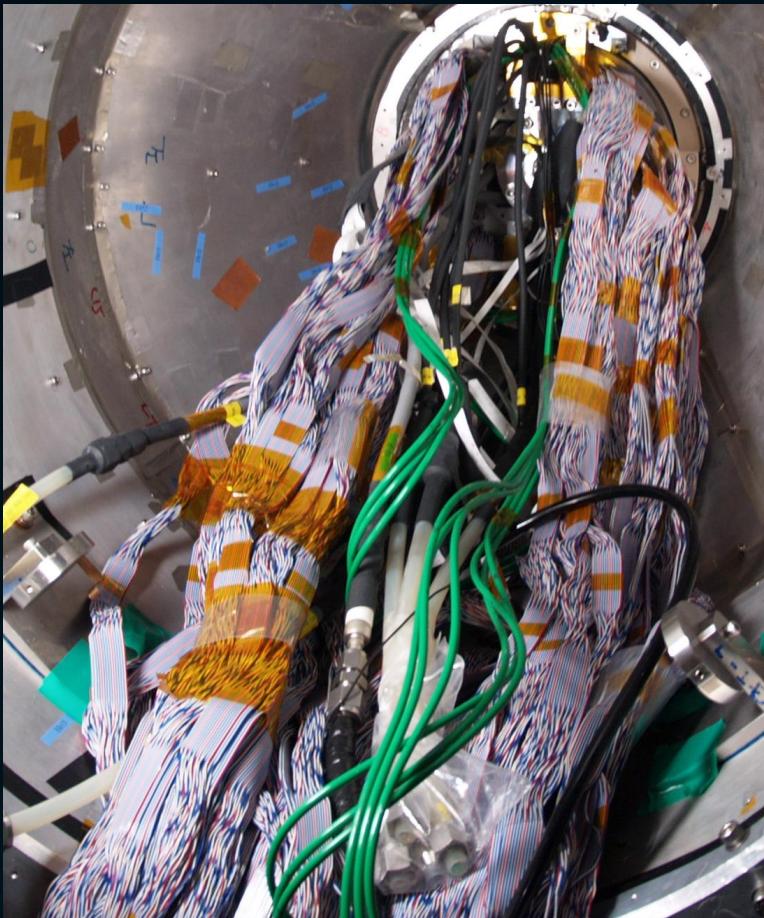
Combined they give a very powerful device!

Belle II Vertex Detector VXD = PXD + SVD



**SVD and PXD are very close together
in one common carbon fiber shell**

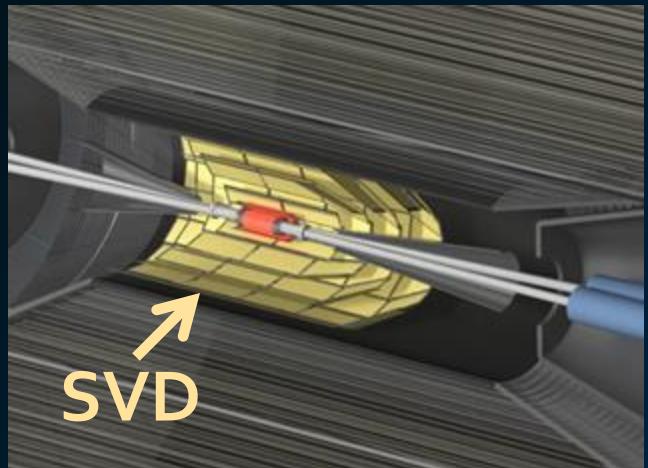
Belle I Readout Cabling



Belle I only had SVD Detectors, no PXD.

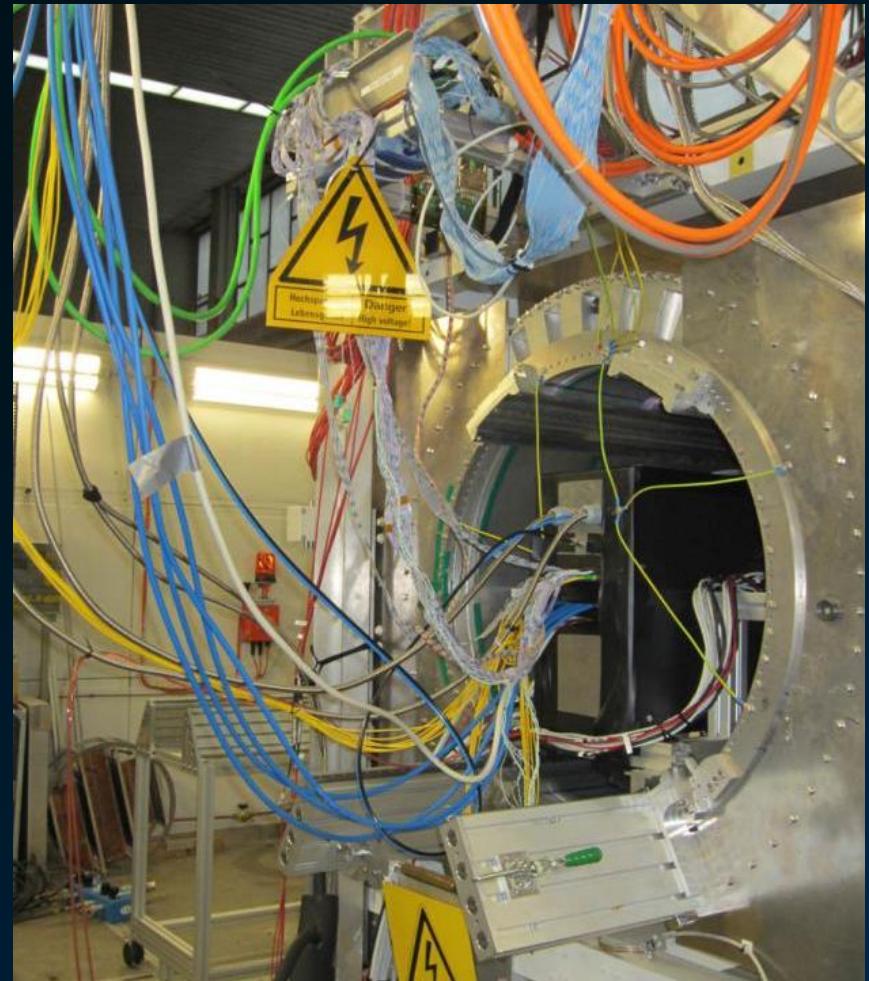
Belle II will be much more complex: SVD + PXD, sharing same cable tunnels.

- **Belle II - Introduction**
- **SVD EMC Tests**
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First Combined SVD/PXD Beam Test 2014-01

- SVD installed alone worked perfectly
- PXD installed → Excessive noise problems in SVD
- SVD Noise was even present with PXD switched off
- Problems have been somehow diminished to a fairly working level by grounding some points to the magnet housing...
- There has no very serious EMC research been done before.



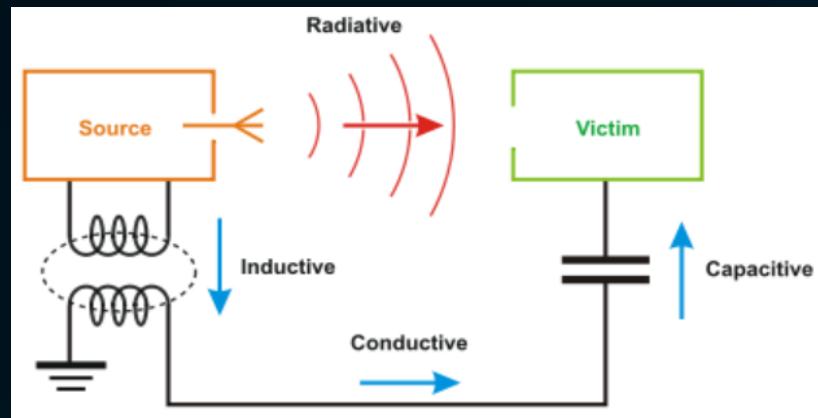
EMC Basics

Noise Coupling Mechanisms:

- Conductive Coupling
 - Common Mode
 - Differential Mode
- Inductive /Magnetic Coupling
- Capacitive Coupling
- Electromagnetic/Radiative Coupling
 - Distance more than a wavelength

Noise Measurement methods:

- Susceptibility/Immunity Testing
(by injecting noise)
- Emissions Testing
(by measuring own noise output)

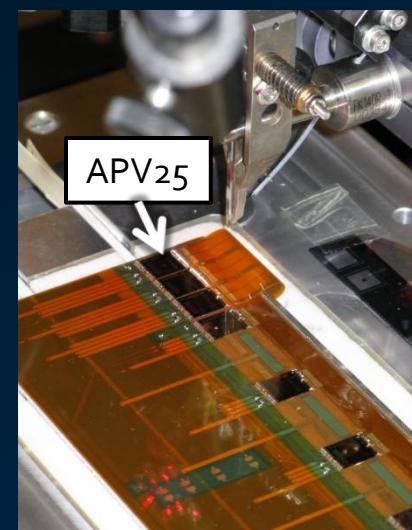
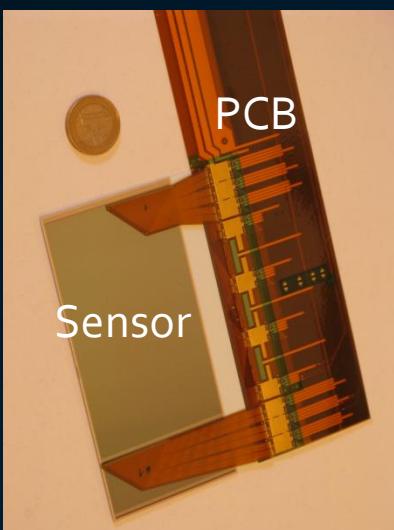
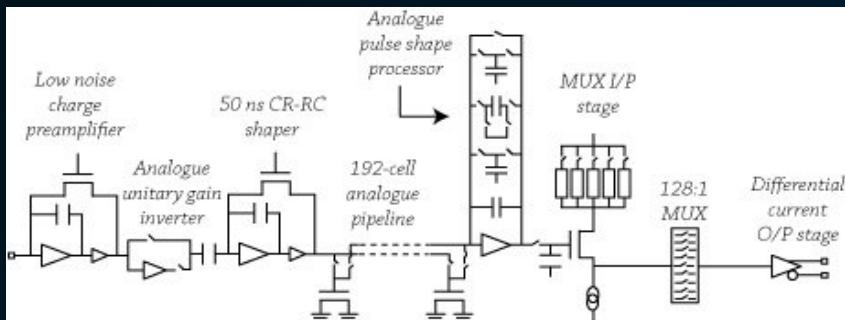
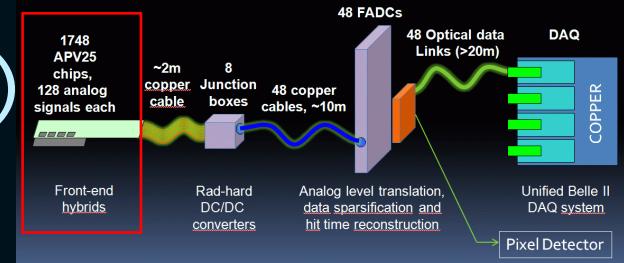
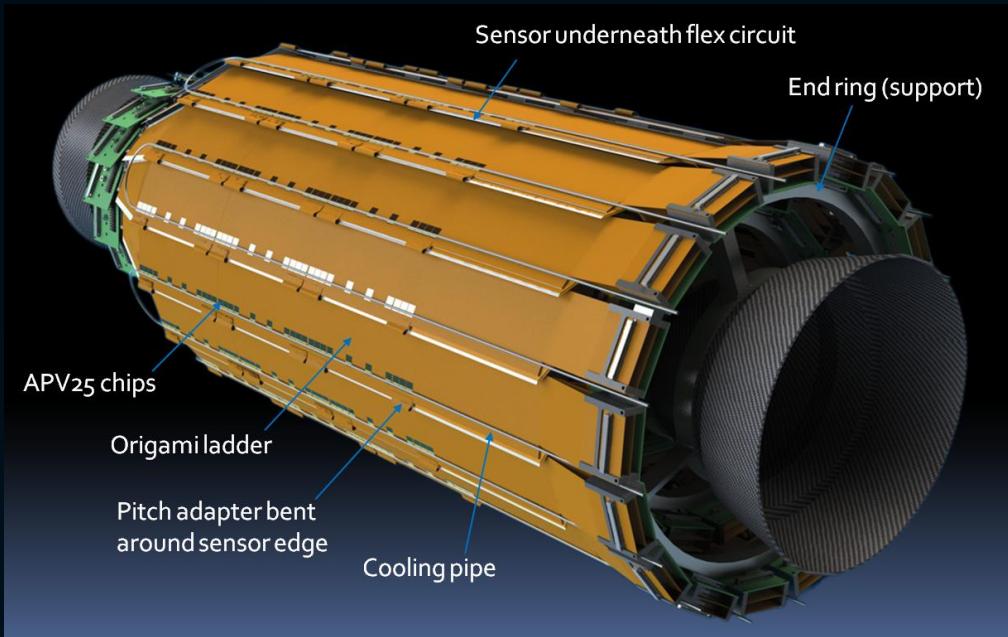


Corrective actions:

- Grounding
- Shielding
- Filtering
- Diminishing the source
- Avoiding of wire loops, antenna structures, ...
- Electrical separation
- Spatial separation
- less noisy components
- ...

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APV25 Front-End Chip (1748x)



- 128 channels per chip
- Analog input for each silicon strip
- Amplifier, Analog pipeline,
- Time multiplexed Analog LVDS output
- Power: 1.25V and 2.5V, total 350mW

SVD Data Readout and Power Supply

Radiation: ~ 10 Mrad, Magnet.: 1.6T

Front-end hybrids
with 1748x
APV25-chips,
128 analog
channels each,
on 172 sensors.

~2m
copper
cable

8x Junction
boxes with
rad-hard
DC/DC-
converters

copper
cables, ~17m,
time multiplexed
analog voltages

48x FADC
in 4 crates.

48x Optical data
Links (>20m)

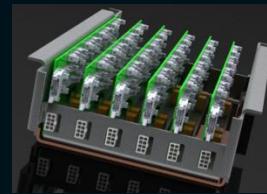
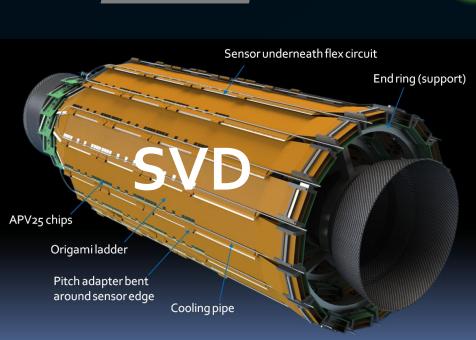
Data Acquisition
(DAQ)

COPPER

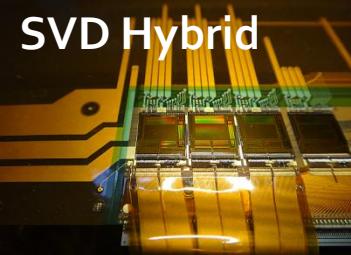


Power Supplies

Pixel Detector
(DATCON)



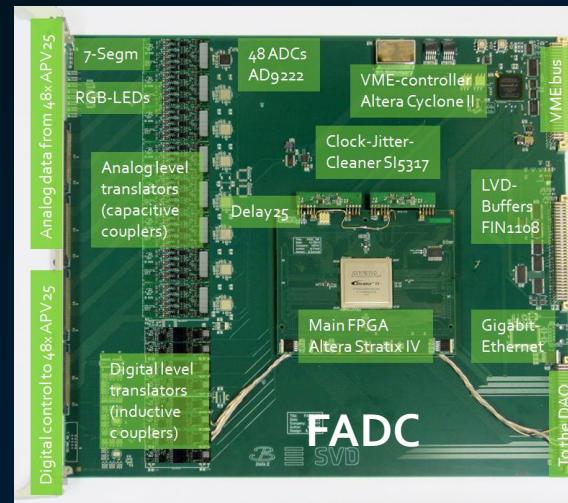
Junction Box



SVD Hybrid



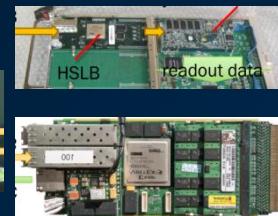
Cabling



FADC

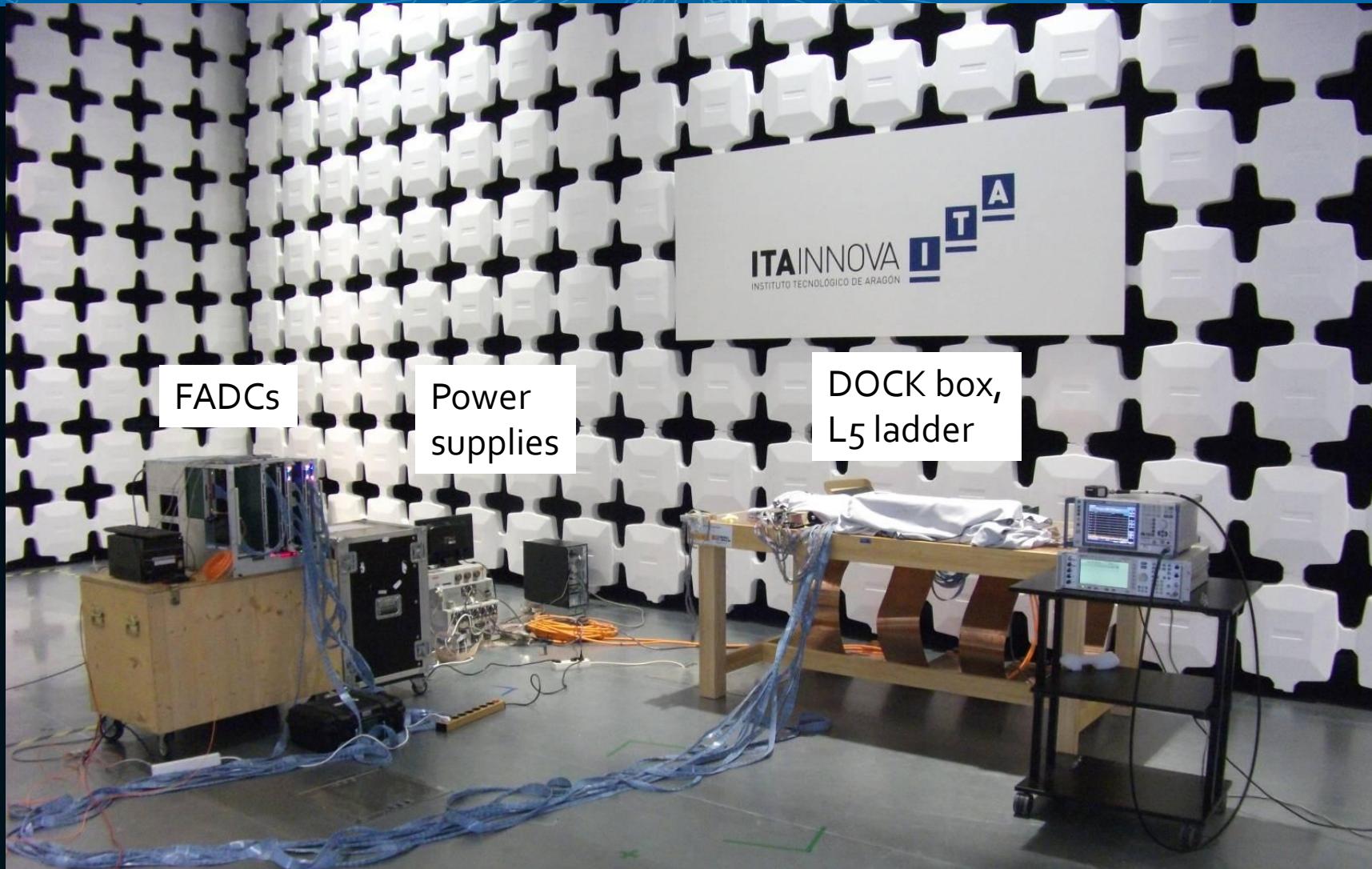


FTB



DATCON

COPPER



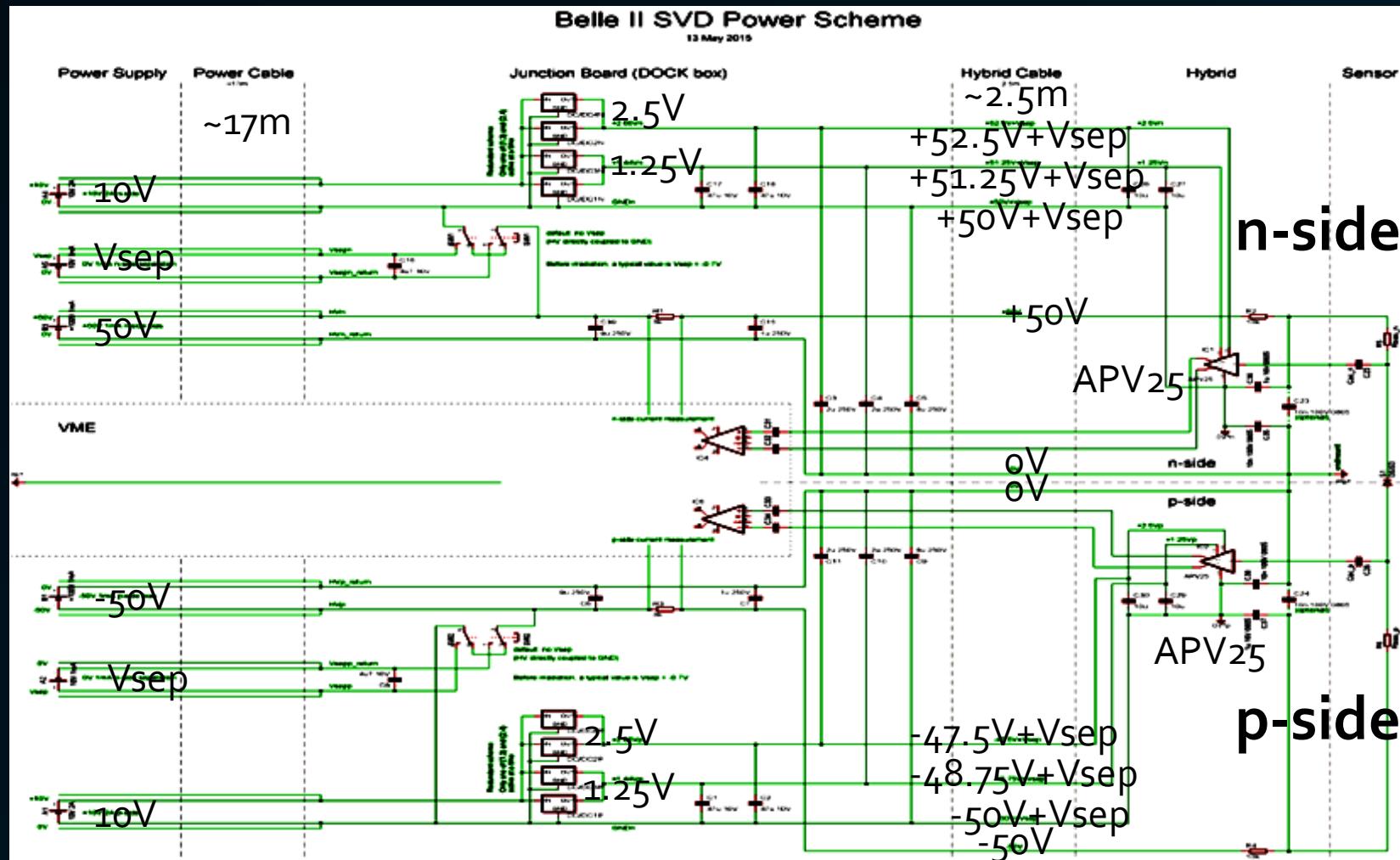
End of May 2015: EMC Measurements at ITA, Zaragoza / Spain.



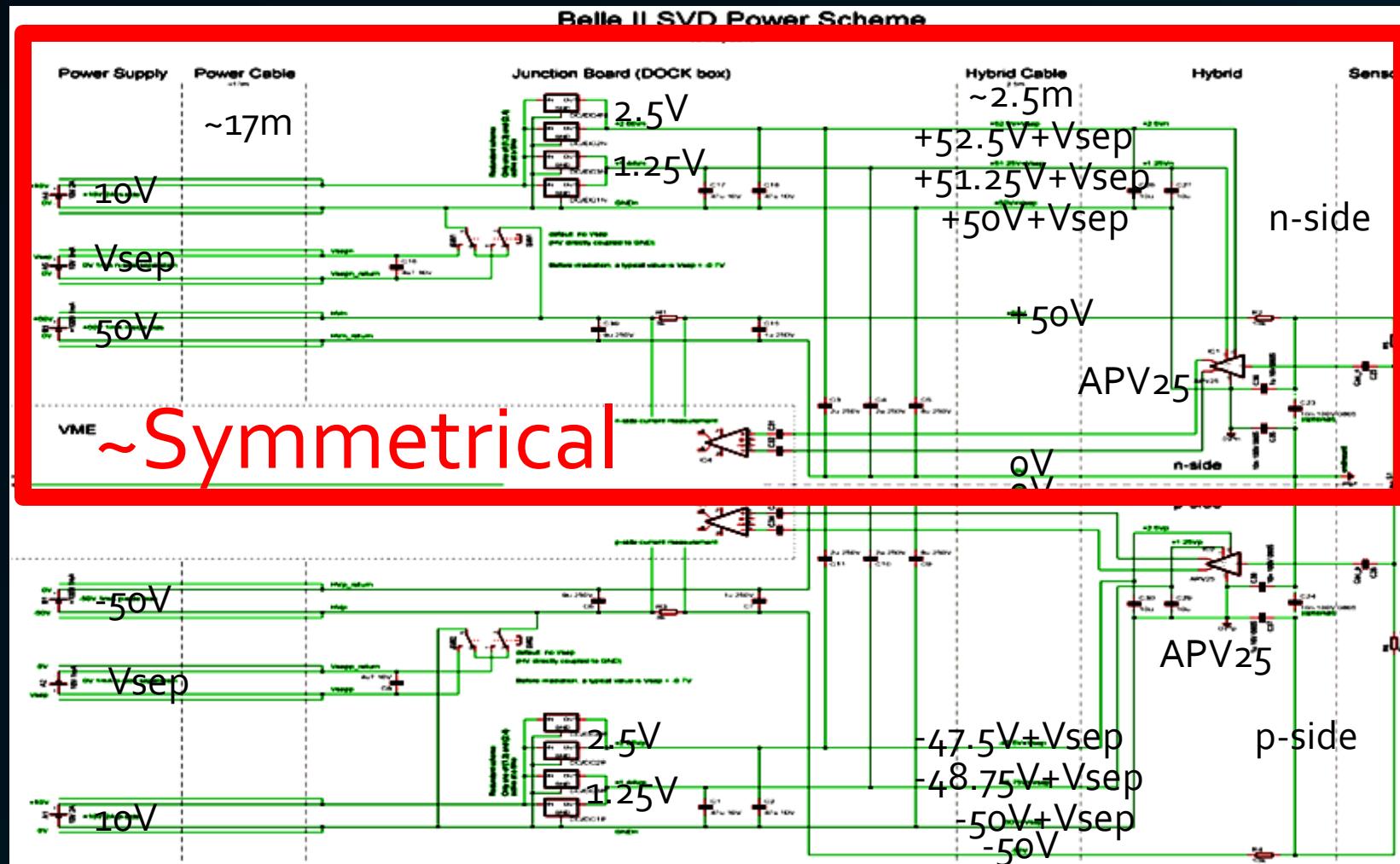
Device under Test: SVD Layer 5



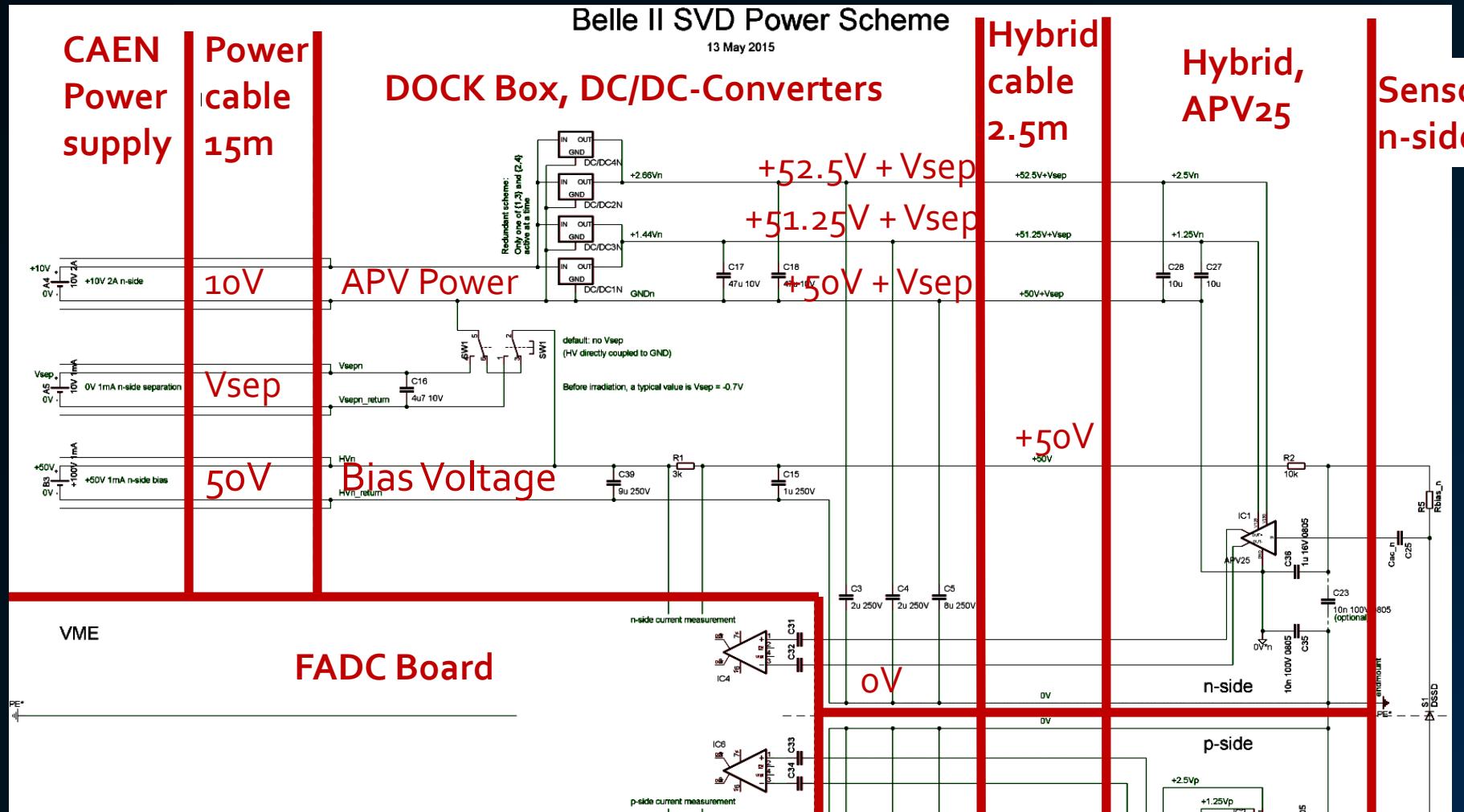
SVD EMC Tests – Power and Grounding Scheme



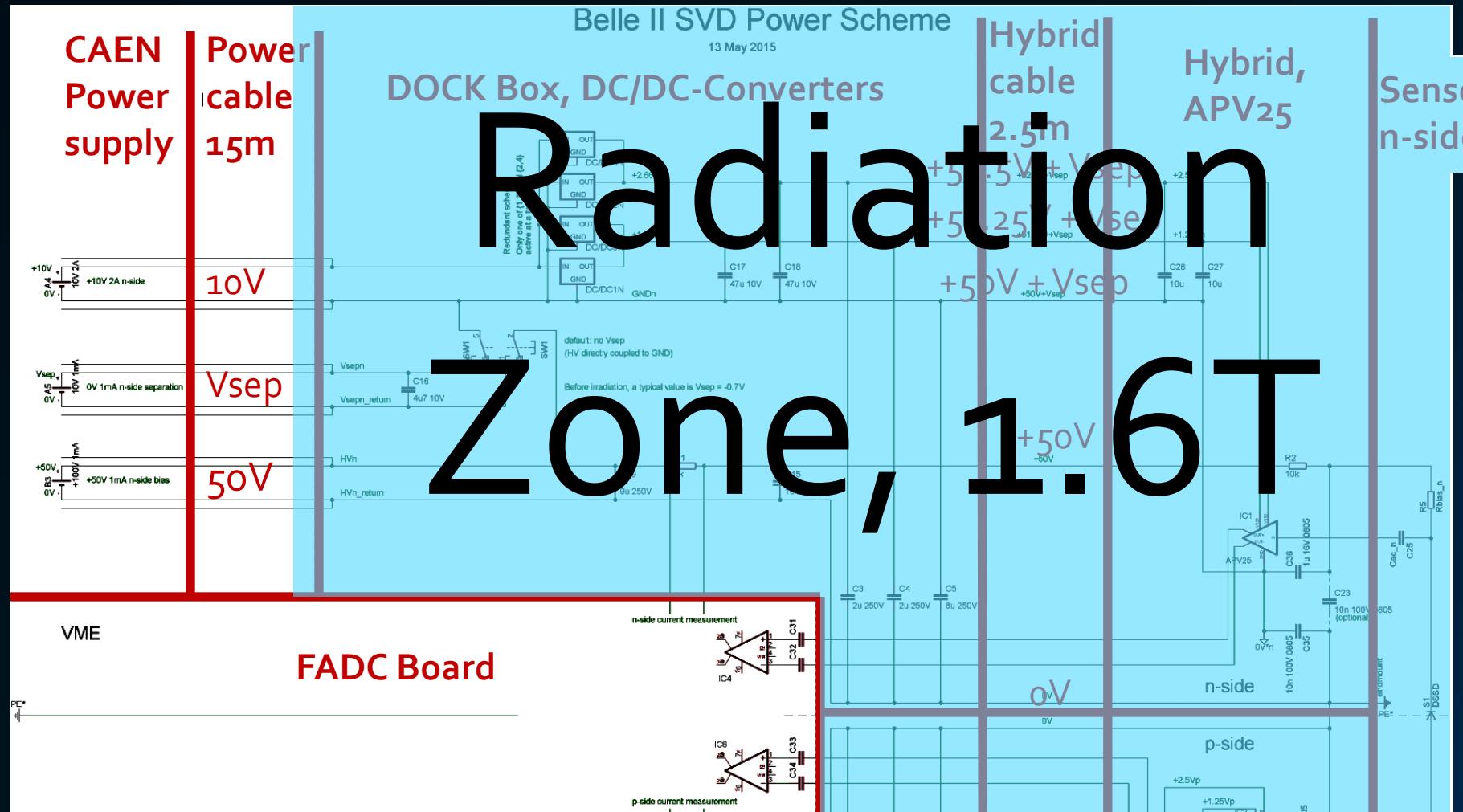
SVD EMC Tests – Power and Grounding Scheme



SVD EMC Tests – Power Scheme (Detail)



SVD EMC Tests - Power Scheme (Detail)

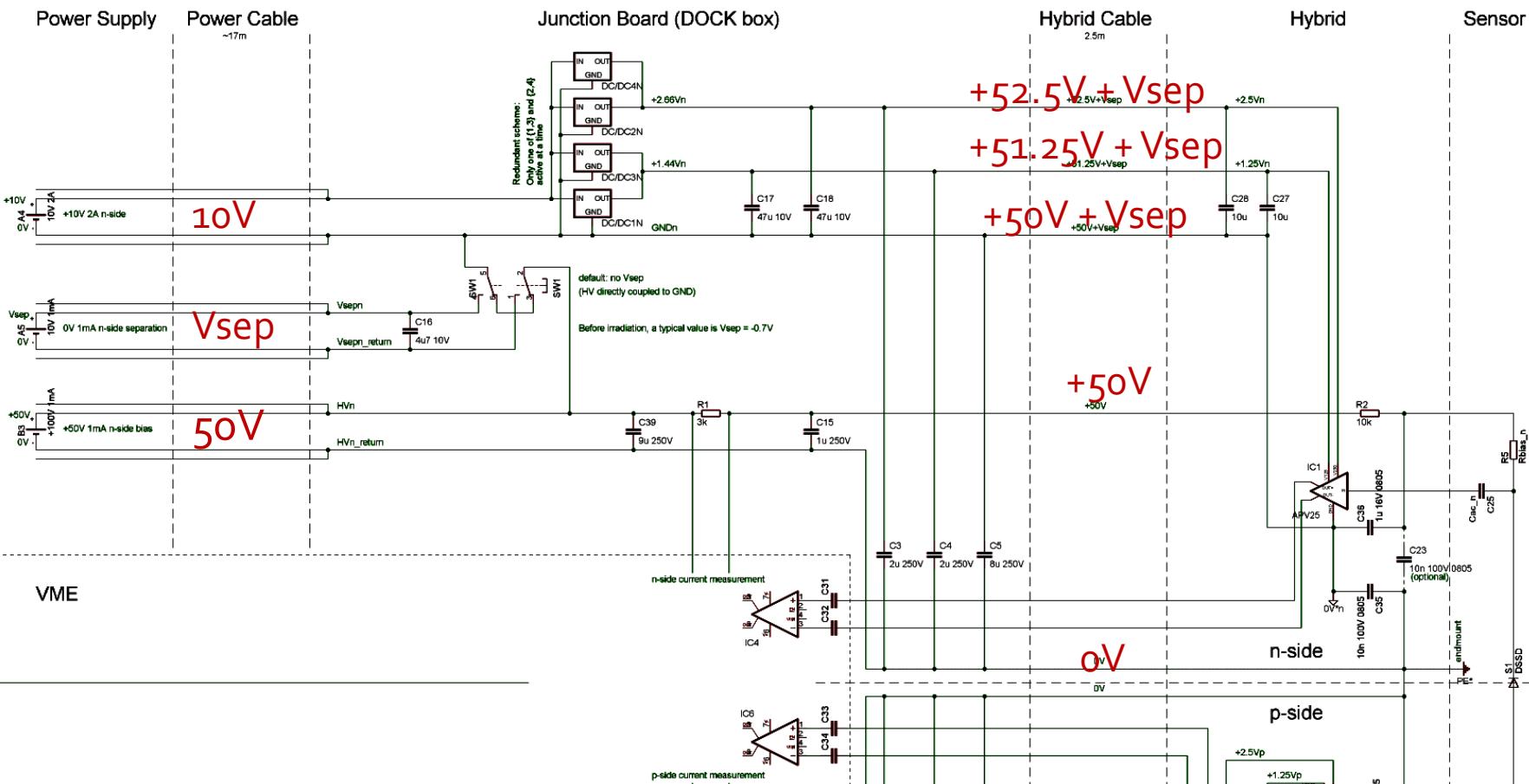


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SVD EMC Tests – APV25 Sensitivity

Belle II SVD Power Scheme

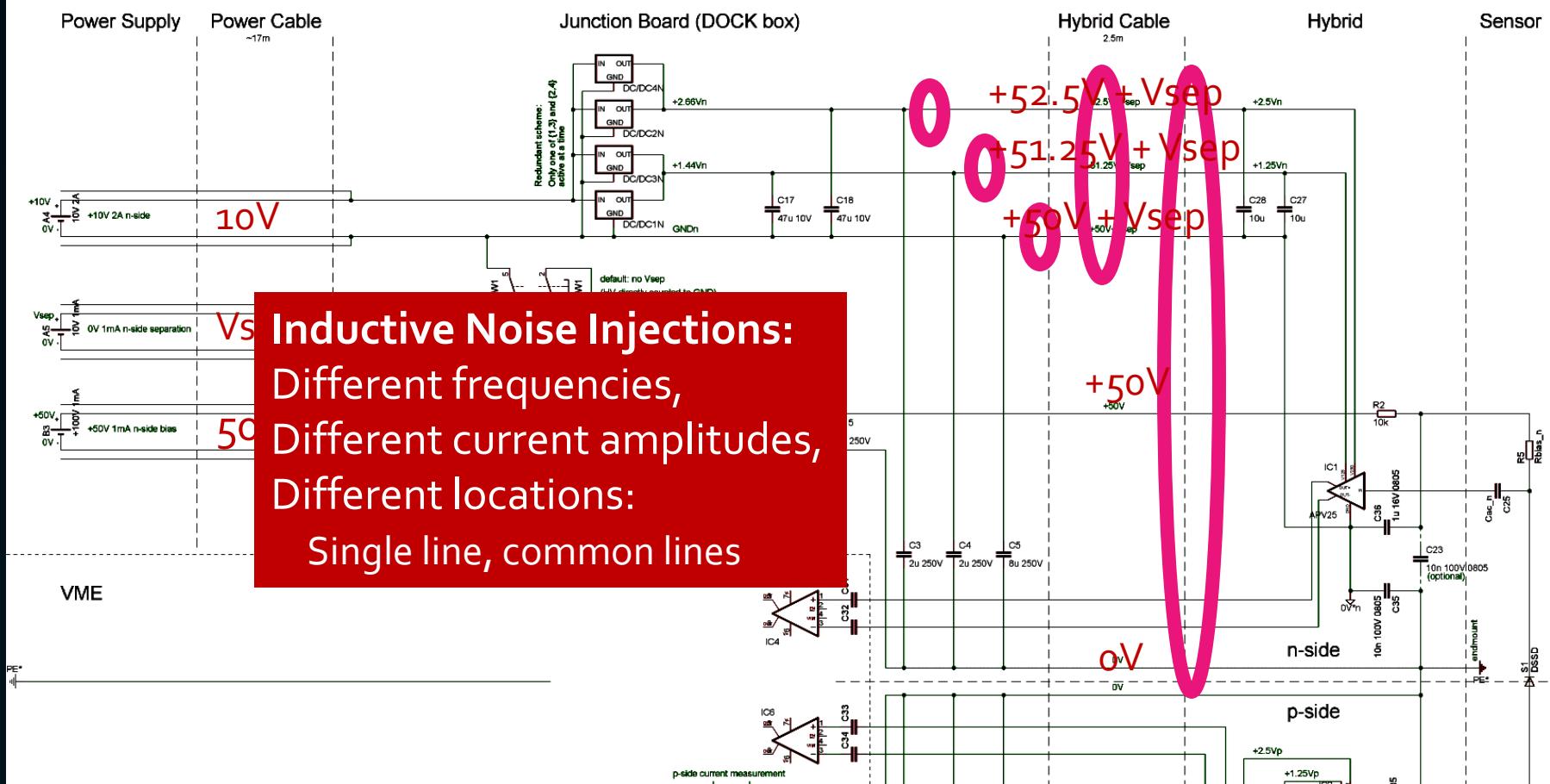
13 May 2015



SVD EMC Tests – APV25 Sensitivity

Belle II SVD Power Scheme

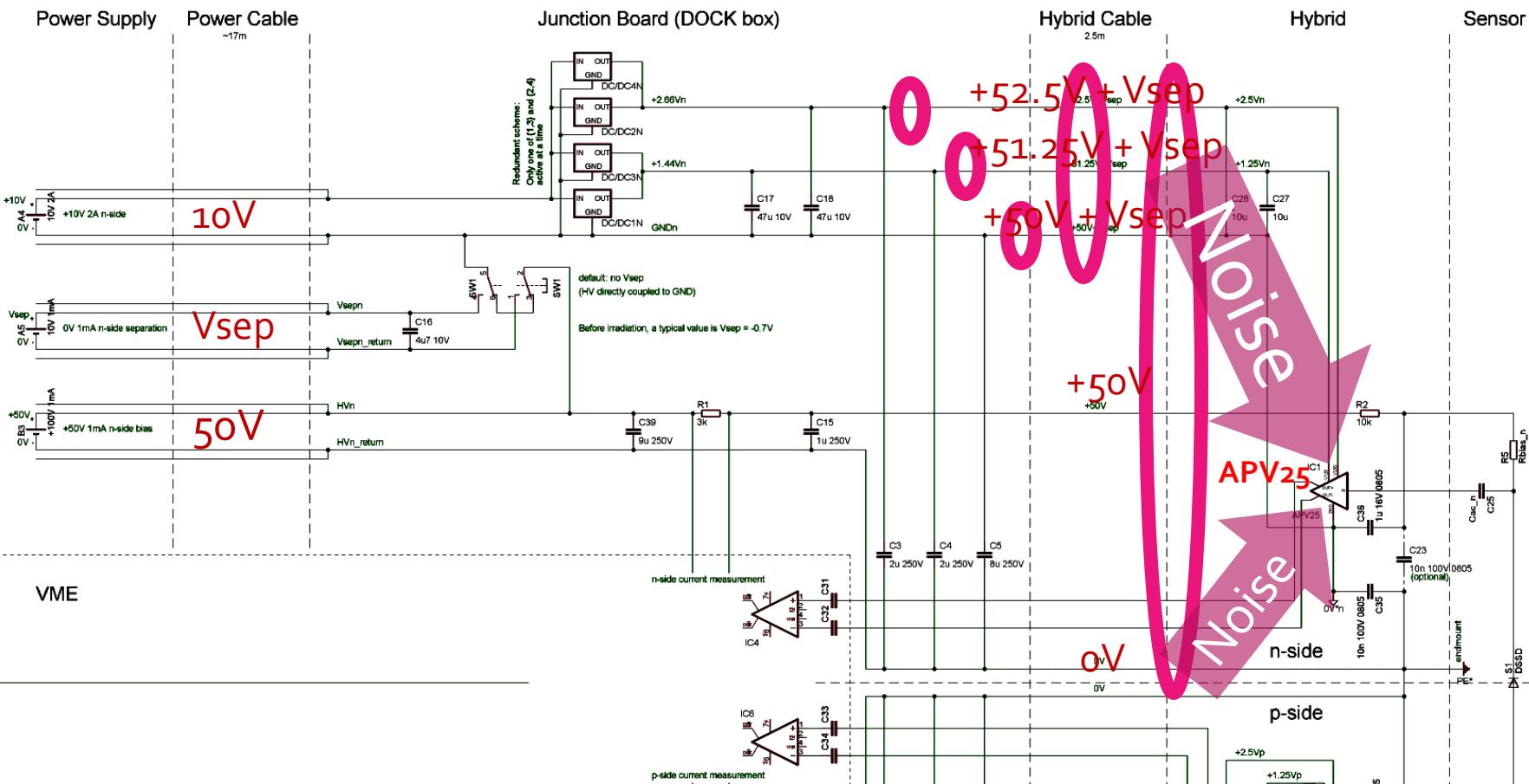
13 May 2015



SVD EMC Tests – APV25 Sensitivity

Belle II SVD Power Scheme

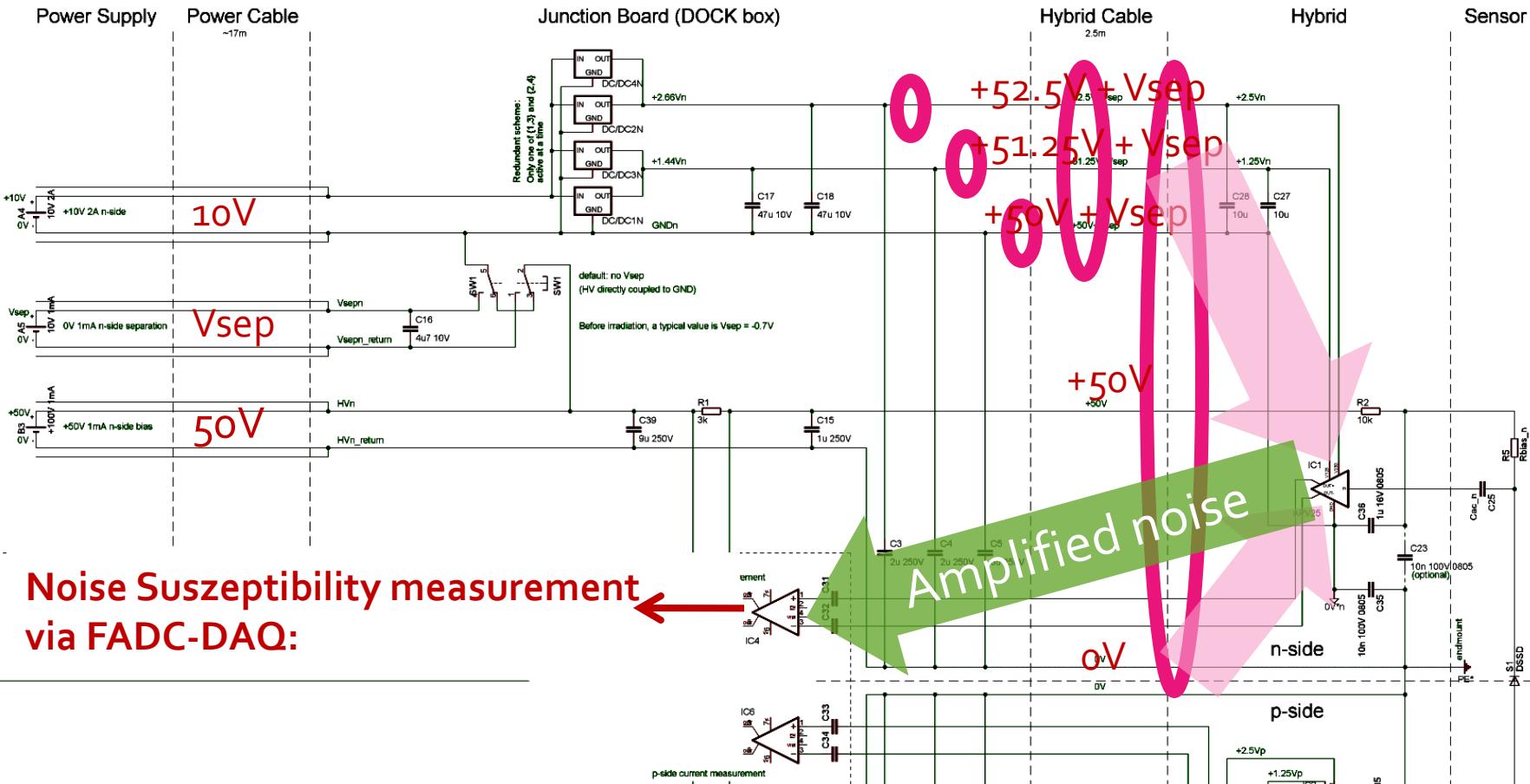
13 May 2015

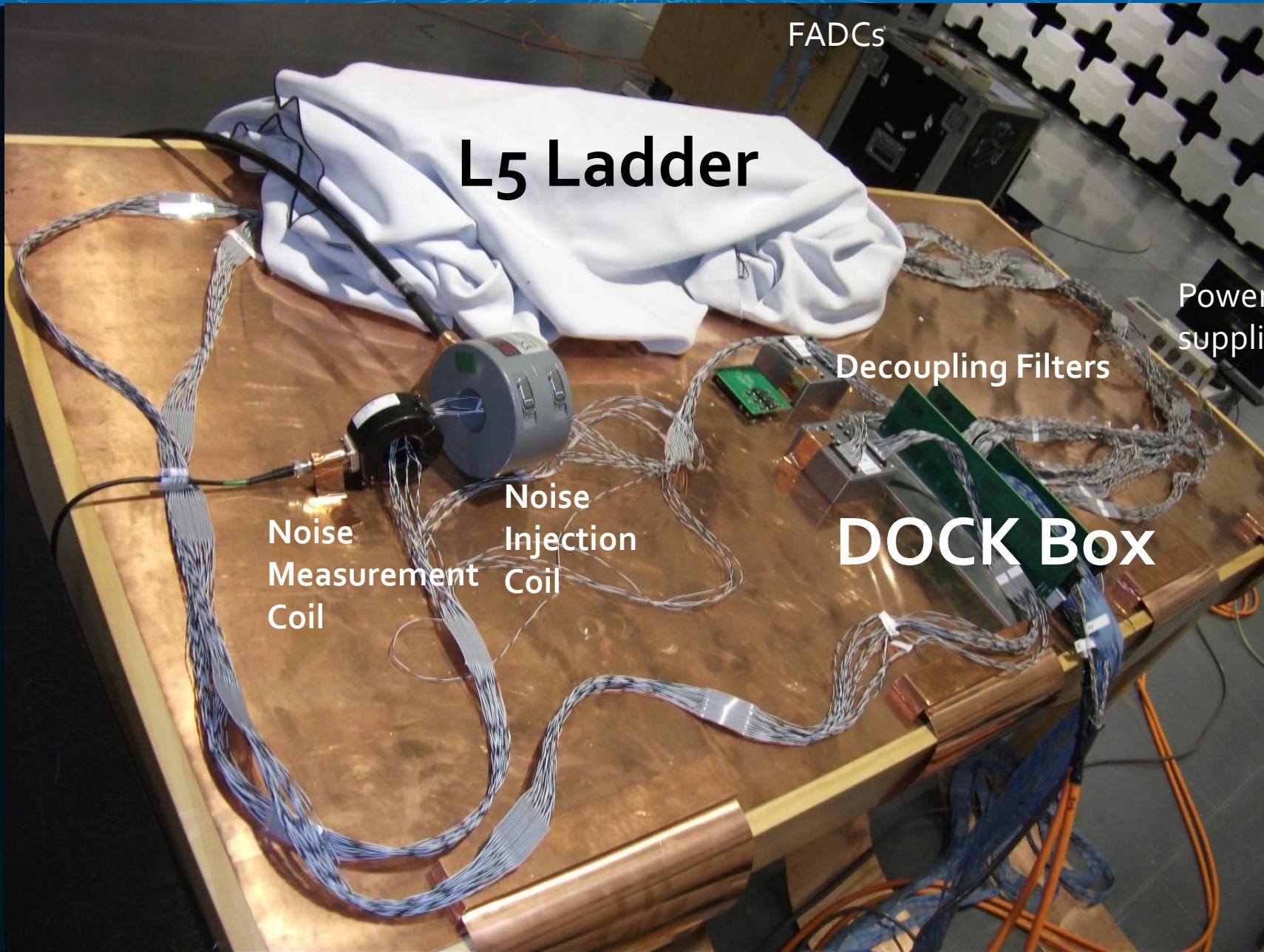


SVD EMC Tests – APV25 Sensitivity

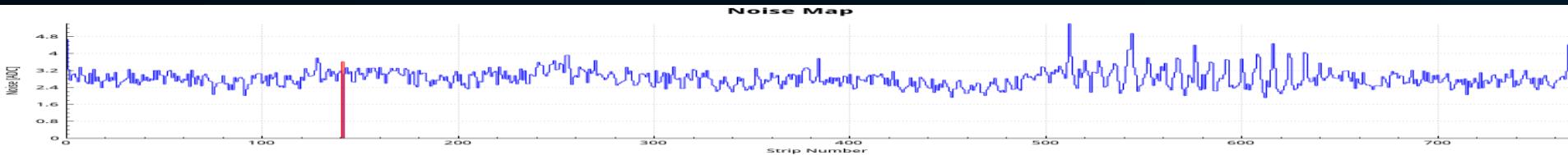
Belle II SVD Power Scheme

13 May 2015

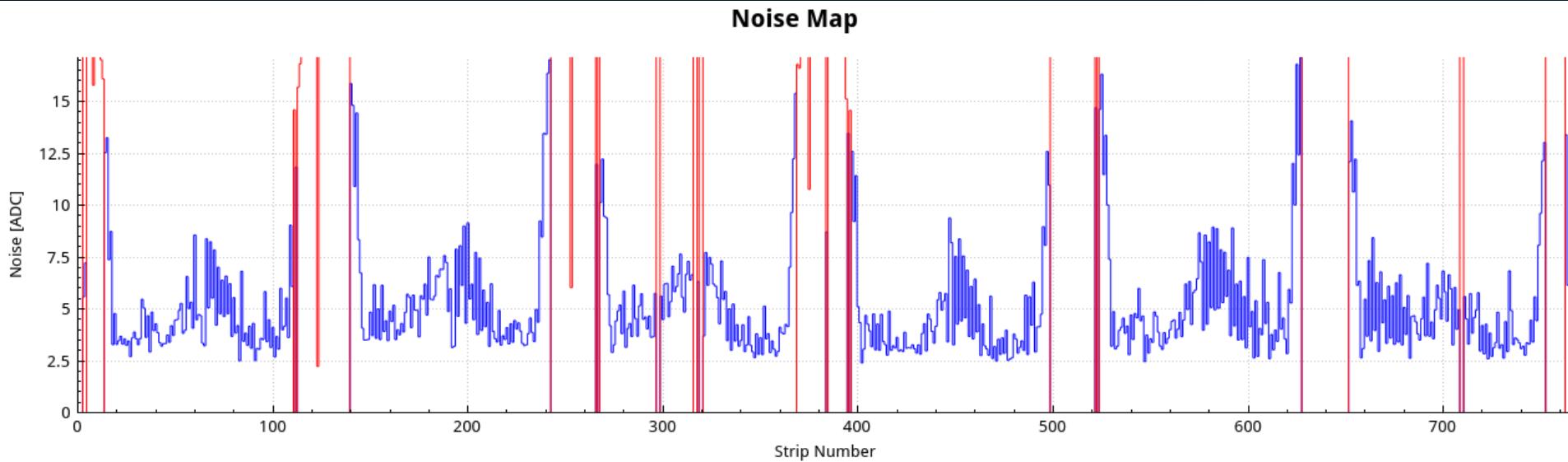




SVD EMC Tests - APV25 Sensitivity



backward sensor, p-side, without induced noise



backward sensor, p-side, with 0.5mA @ 200kHz of induced CM Powerlines noise

Data of all SVD readouts can be seen at <http://elog.hephy.at/electronics/>

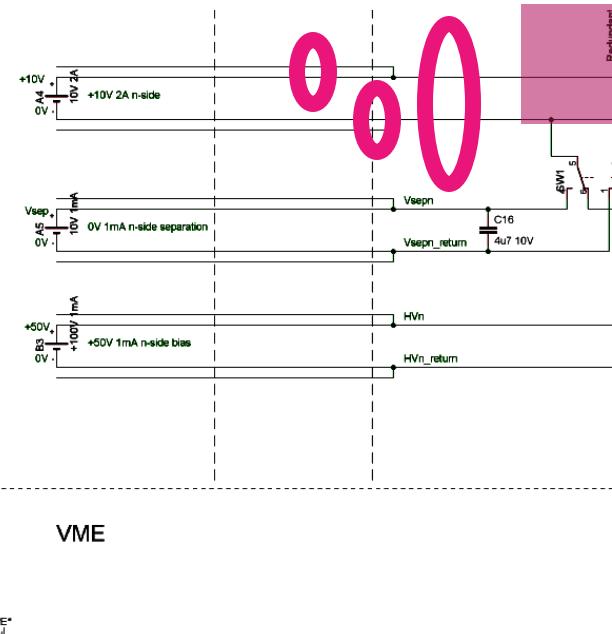
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SVD EMC Tests – DC/DC-Sensitivity

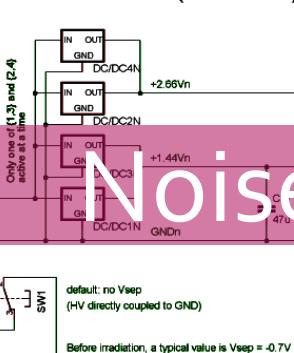
Belle II SVD Power Scheme

13 May 2015

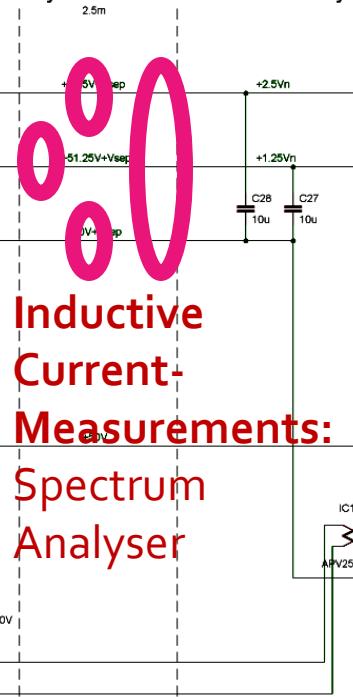
Inductive Noise Injections:
Different frequencies,
Different current amplitudes



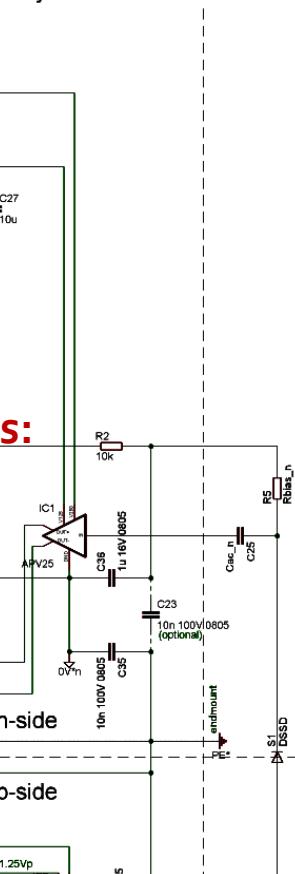
Junction Board (DOCK box)



Hybrid Cable

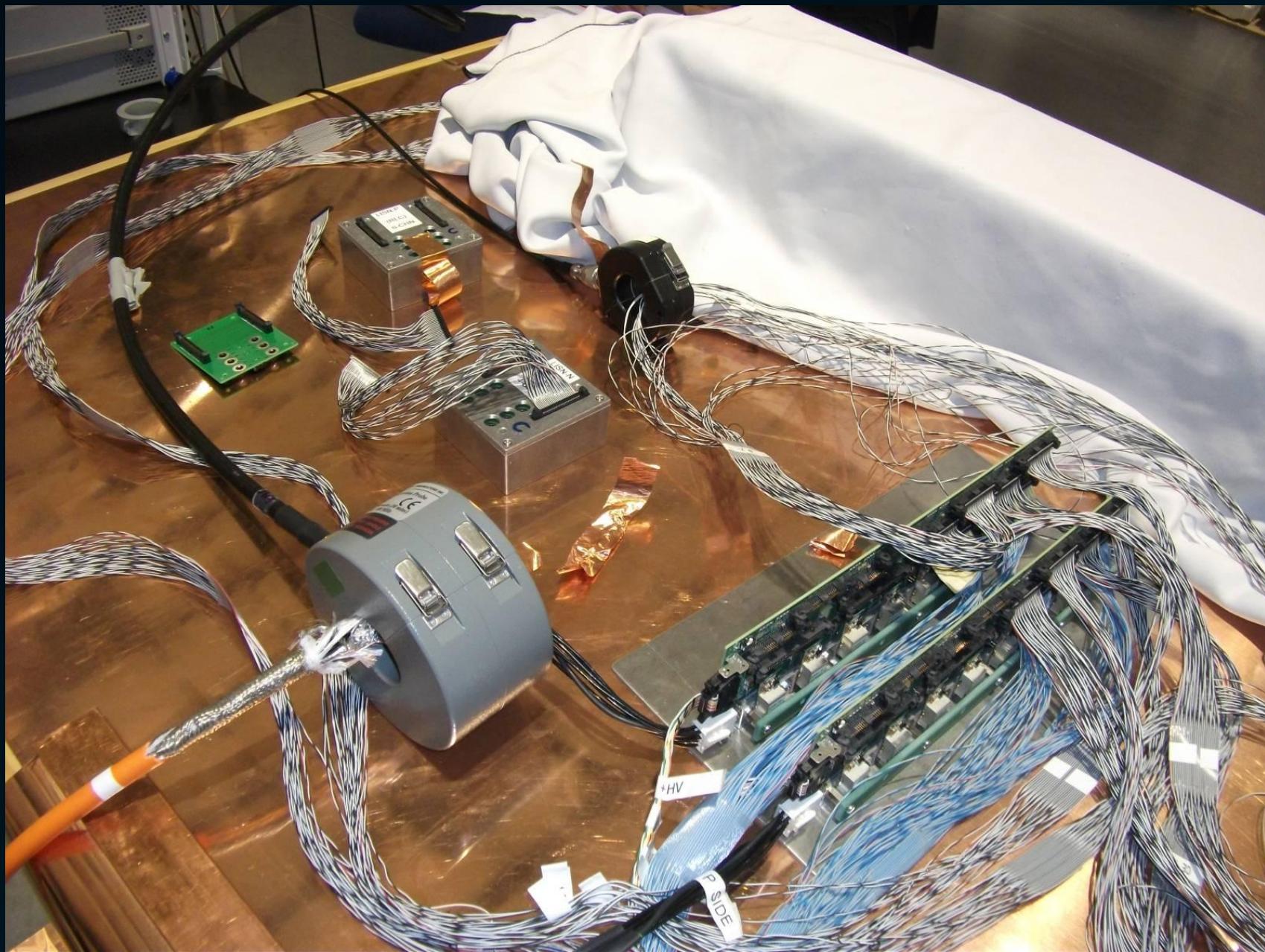


Hybrid



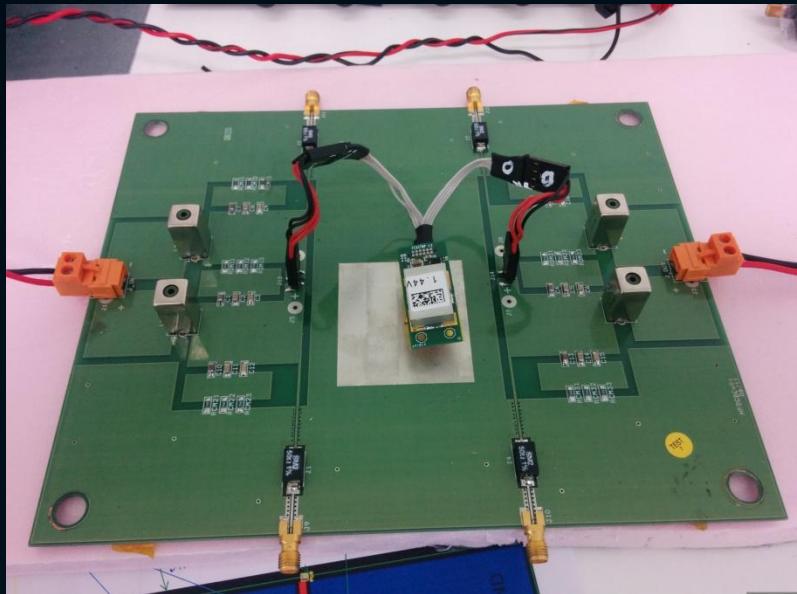
Noise

Inductive
Current-
Measurements:
Spectrum
Analyser



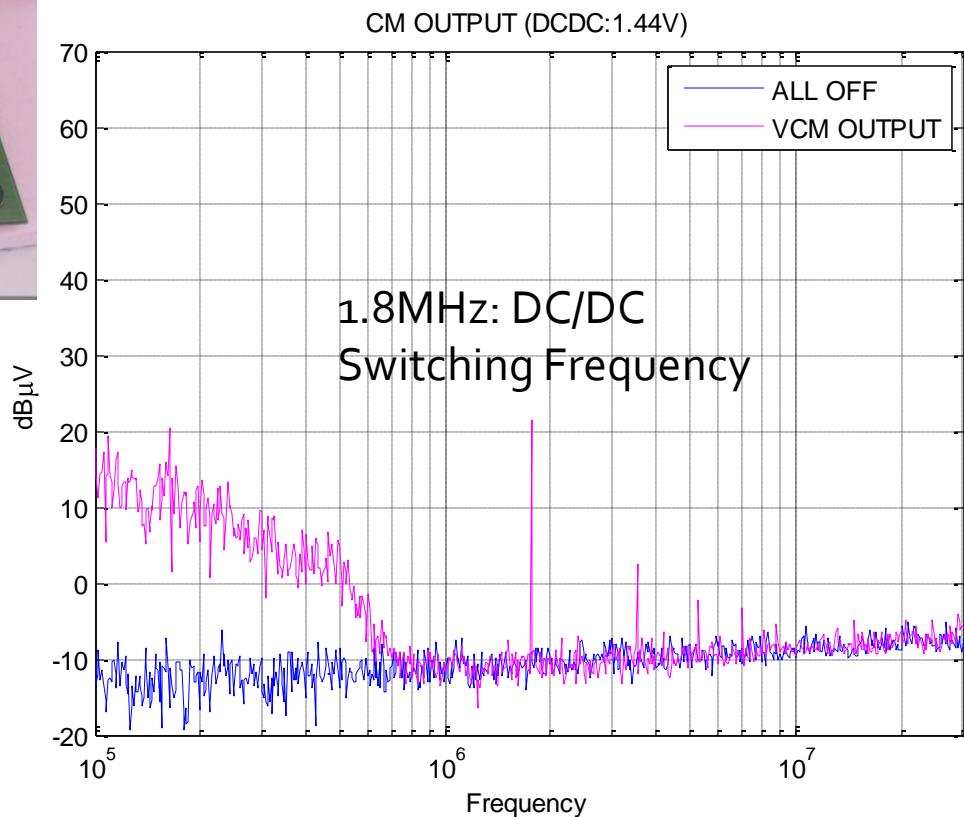
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SVD EMC Tests – DC/DC conducted Emission

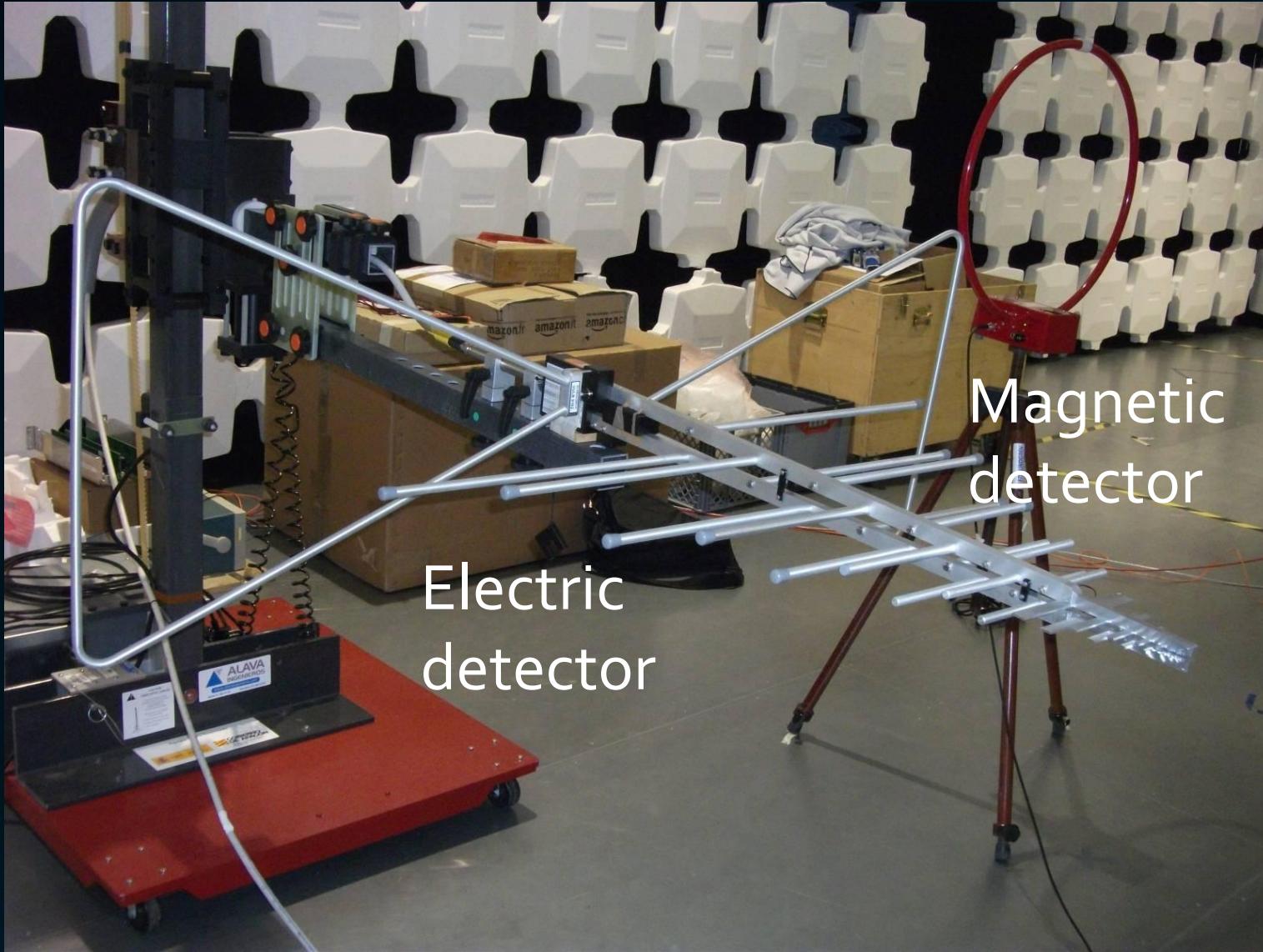


**Full characterization for
100kHz...30MHz, Load 1.5Ω ,
Input 10V:**

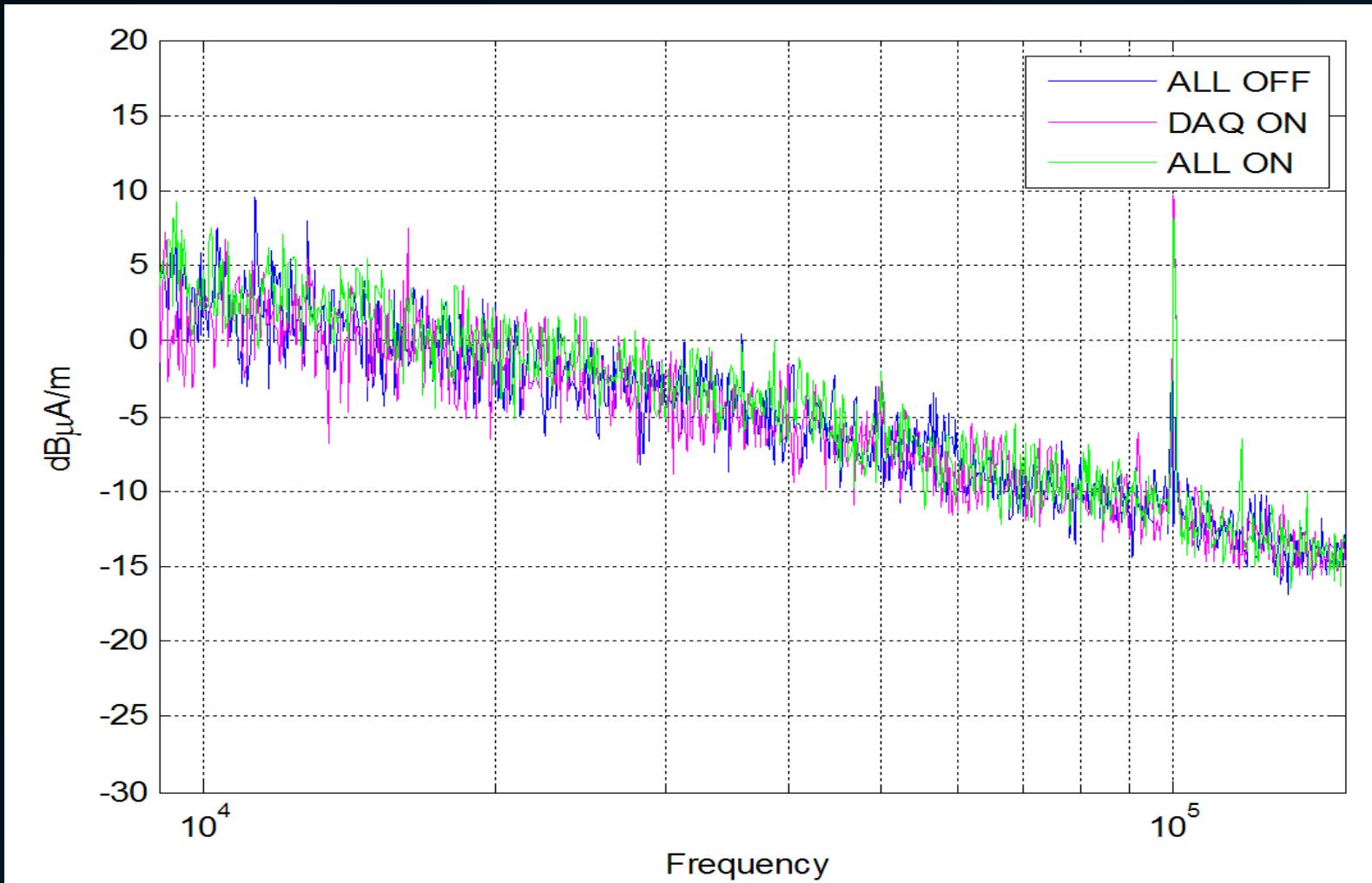
- 1.44V DC-DC
- 2.88V DC-DC
- Common Mode
- Differential Mode
- Input Current Plots
- Output Currents Plots



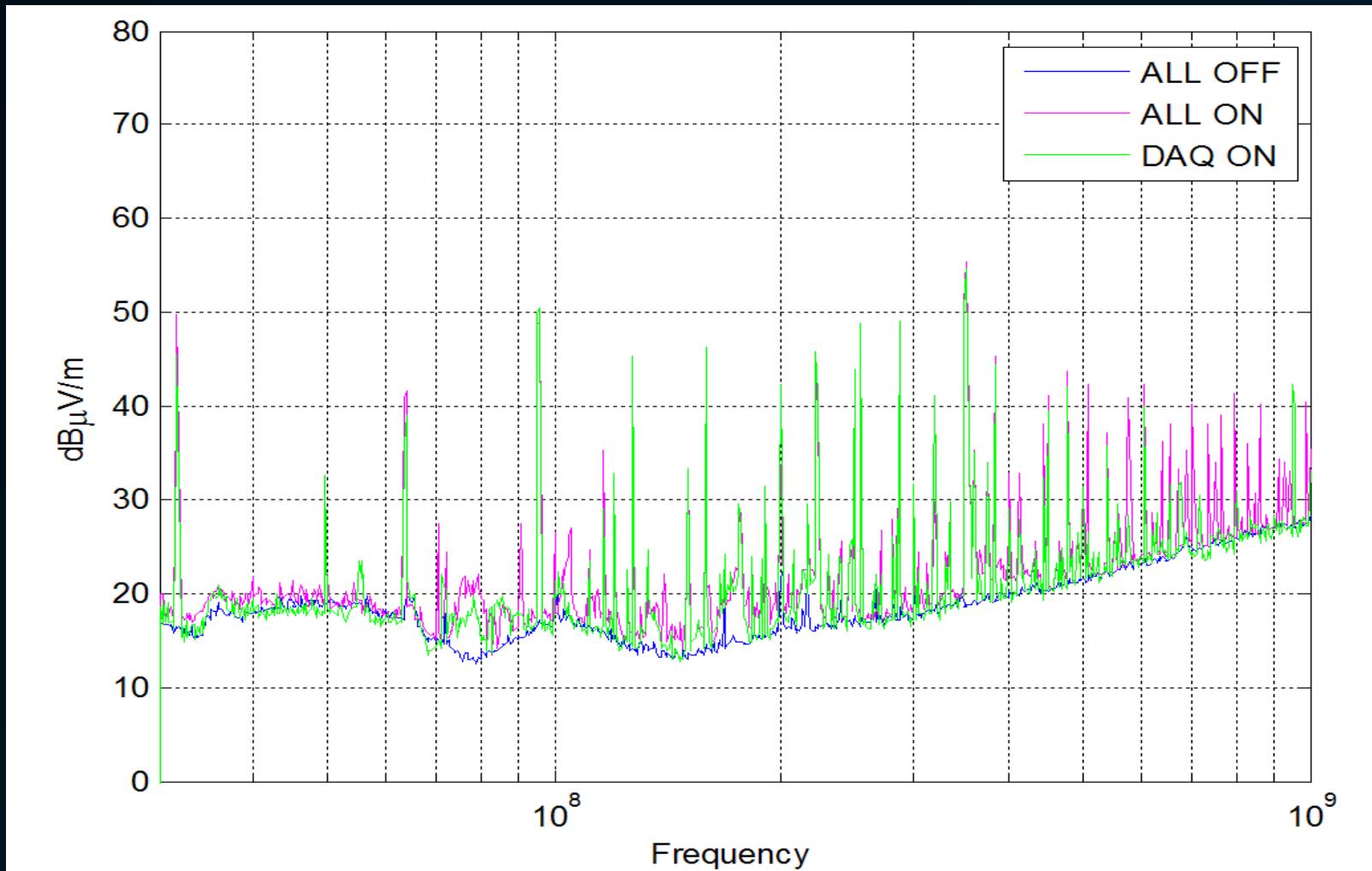
SVD Electric and Magnetic Emissions



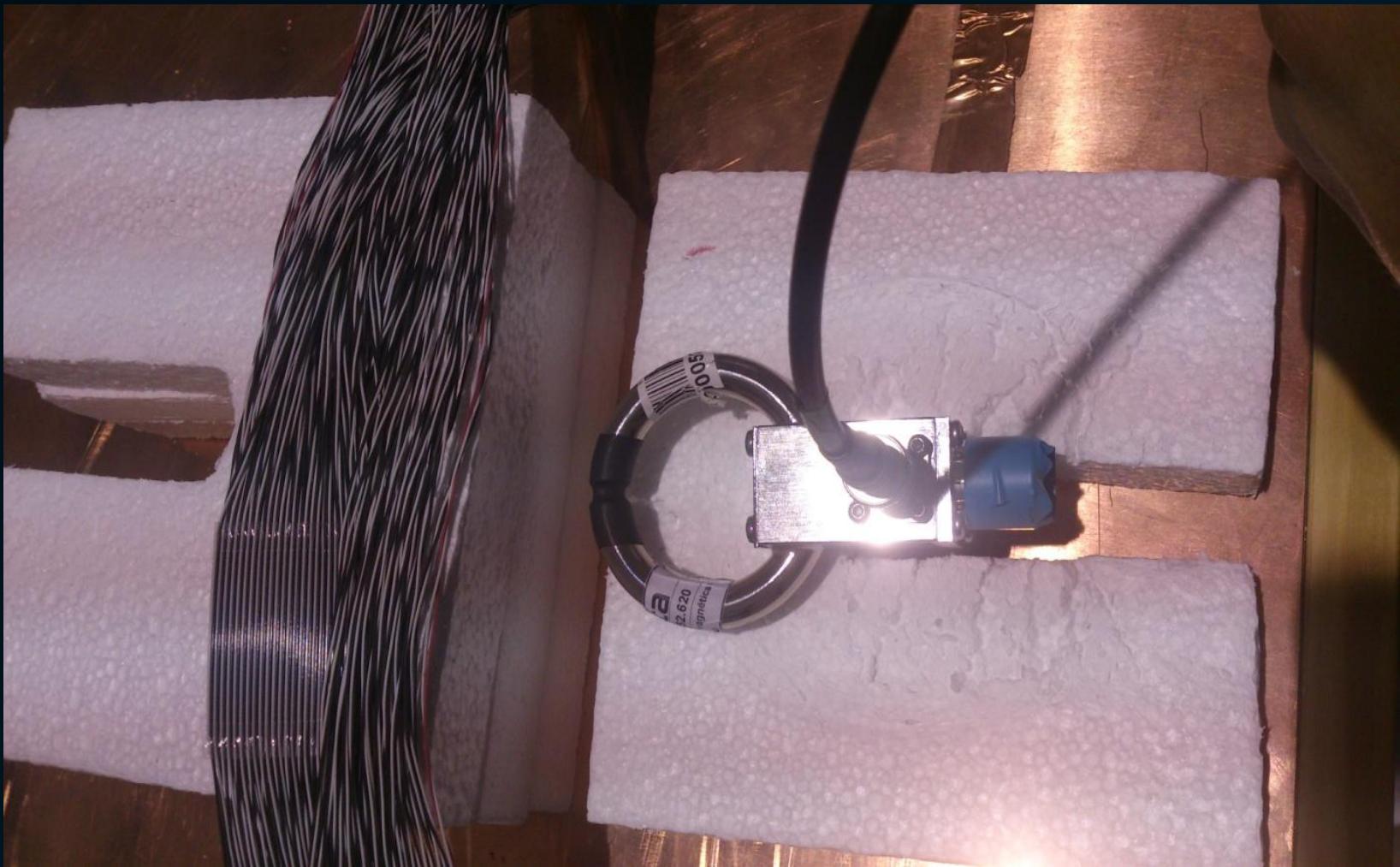
Magnetic Field emission (3m distance).
Far below any level to be concerned of.



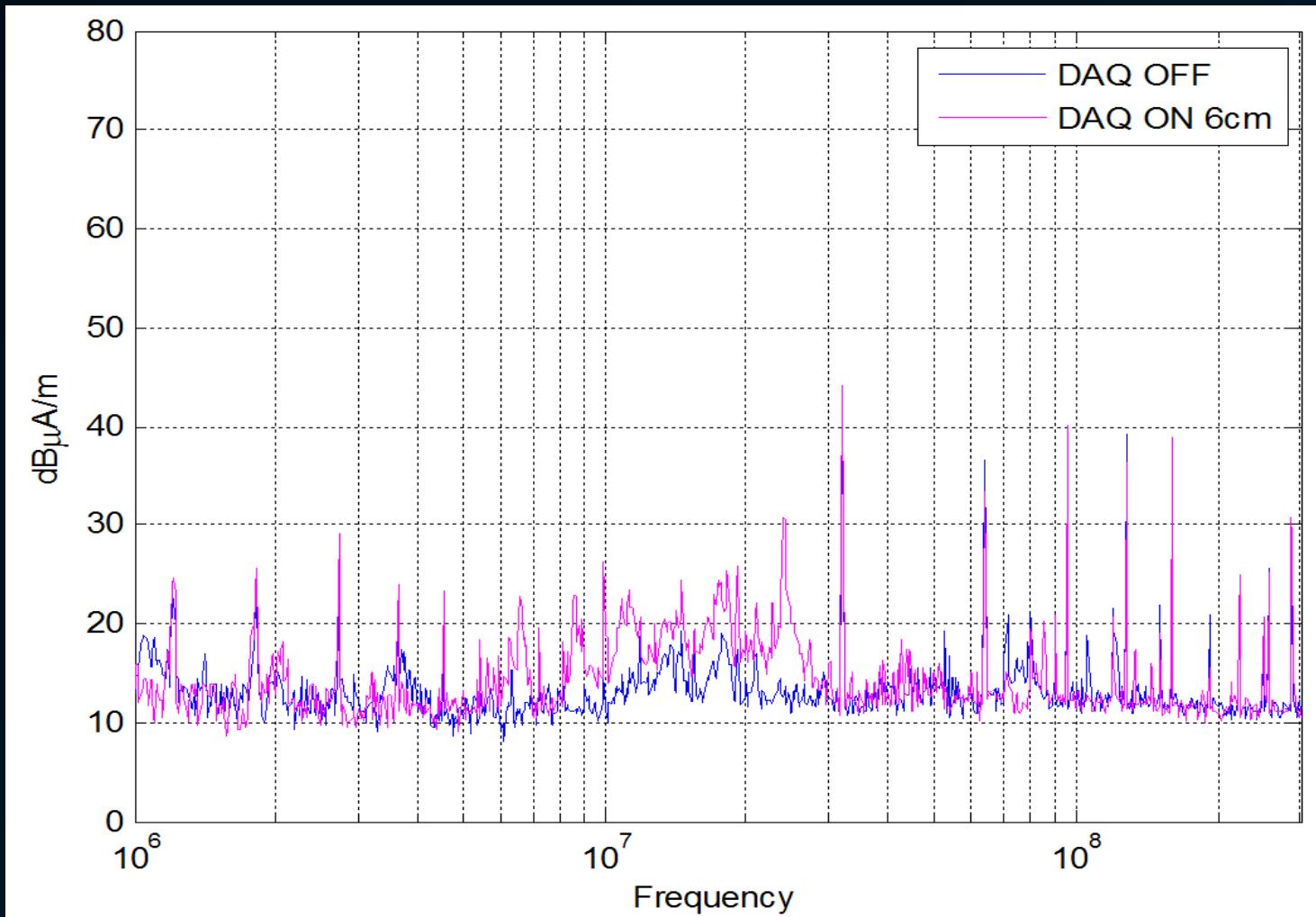
Electrical emission (3m distance).
DAQ dominates, but also very low.



Near magnetic Field emission of the cables (2cm, 4cm, 6cm)

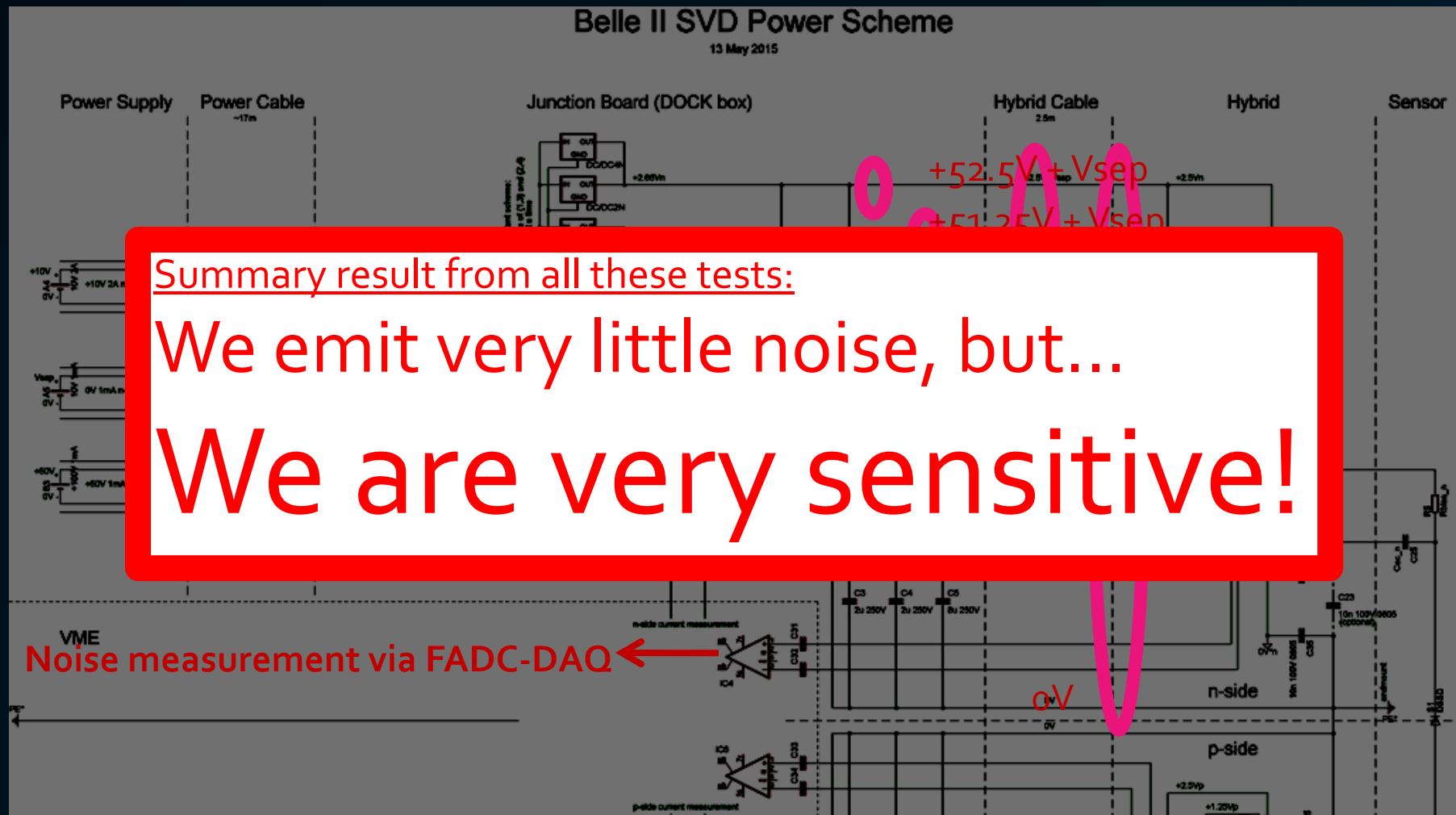


Near magnetic Field emission of the cables (6cm). Very low emission.



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SVD EMC Tests – First conclusions

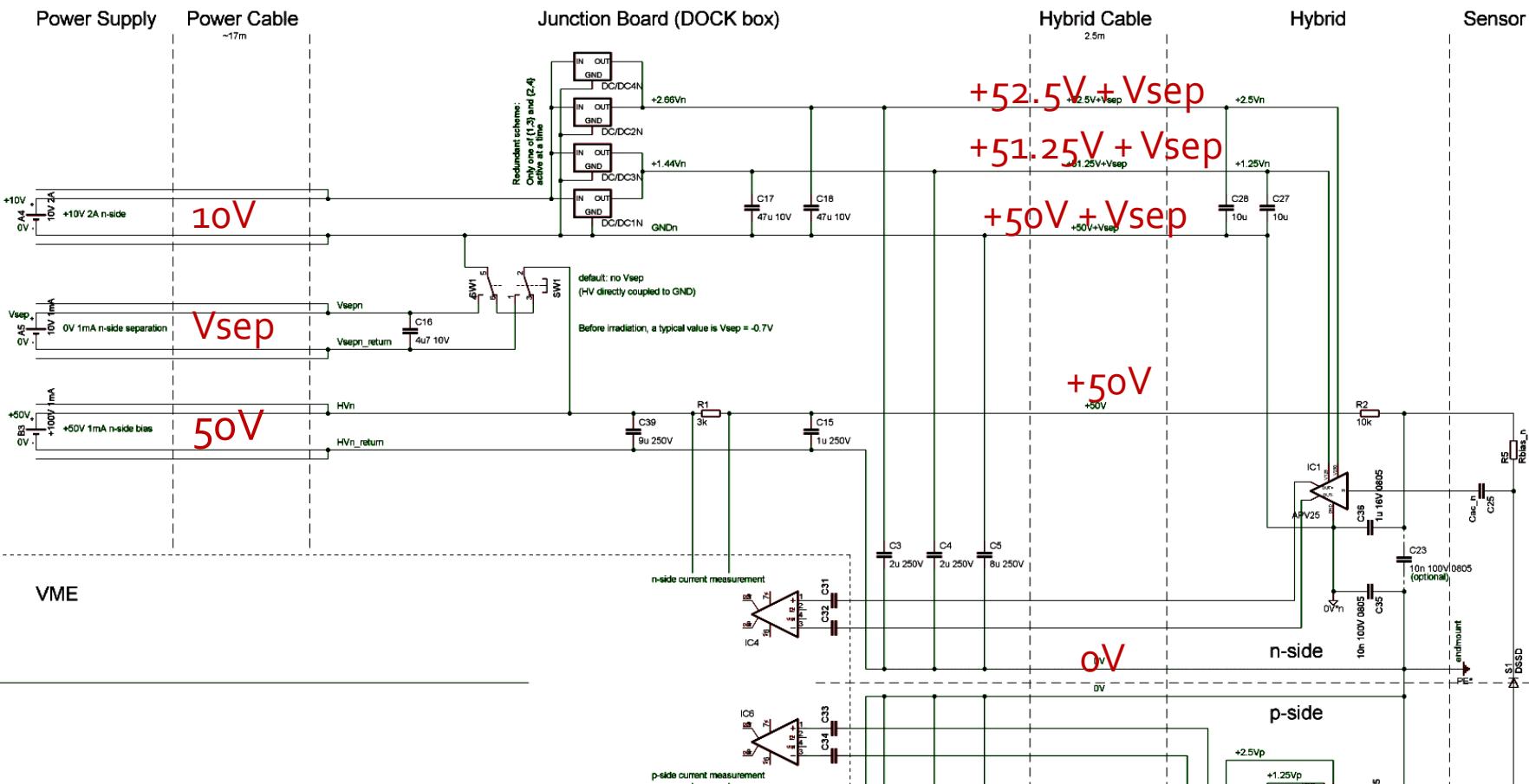


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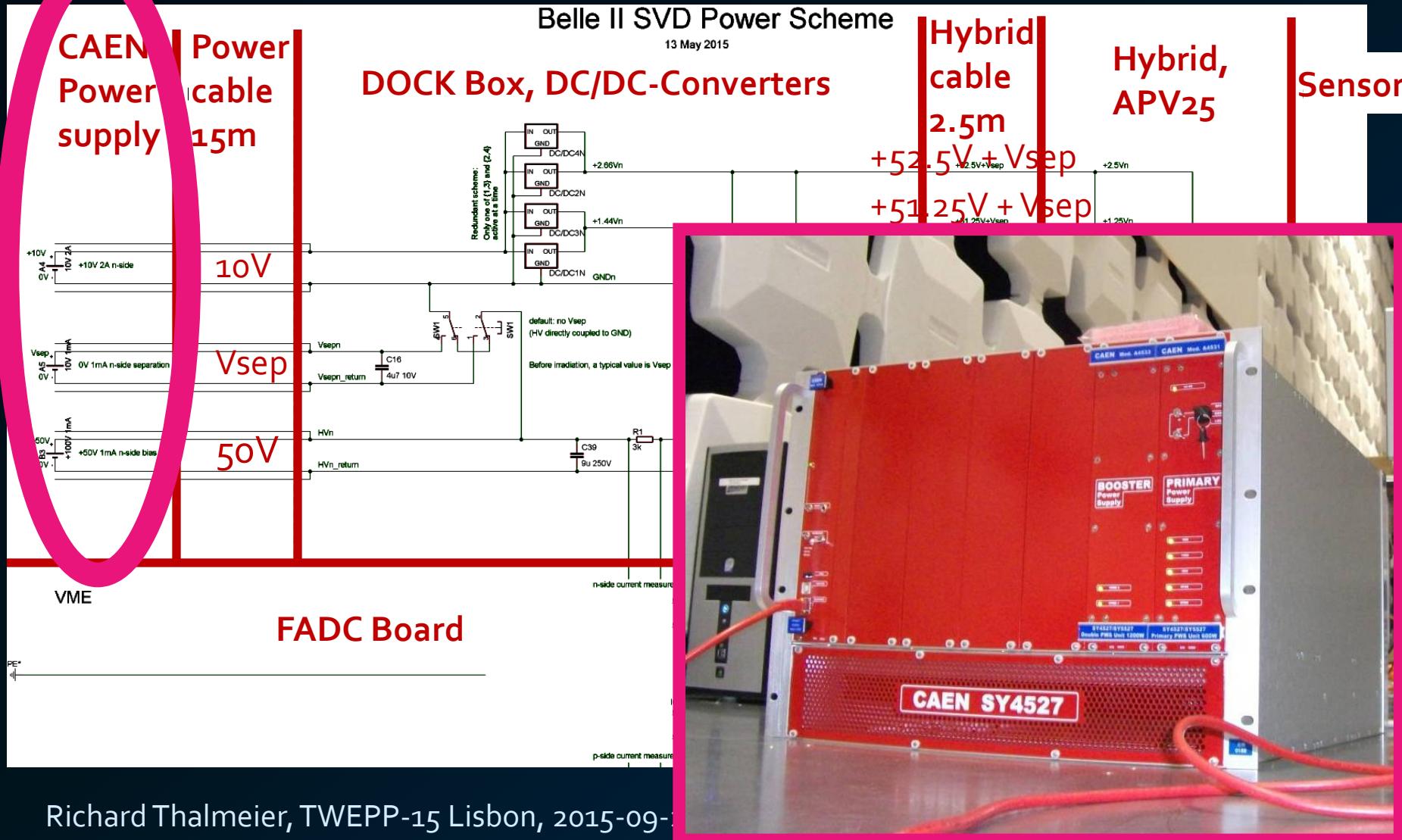
SVD EMC Tests – CAEN Supply

Belle II SVD Power Scheme

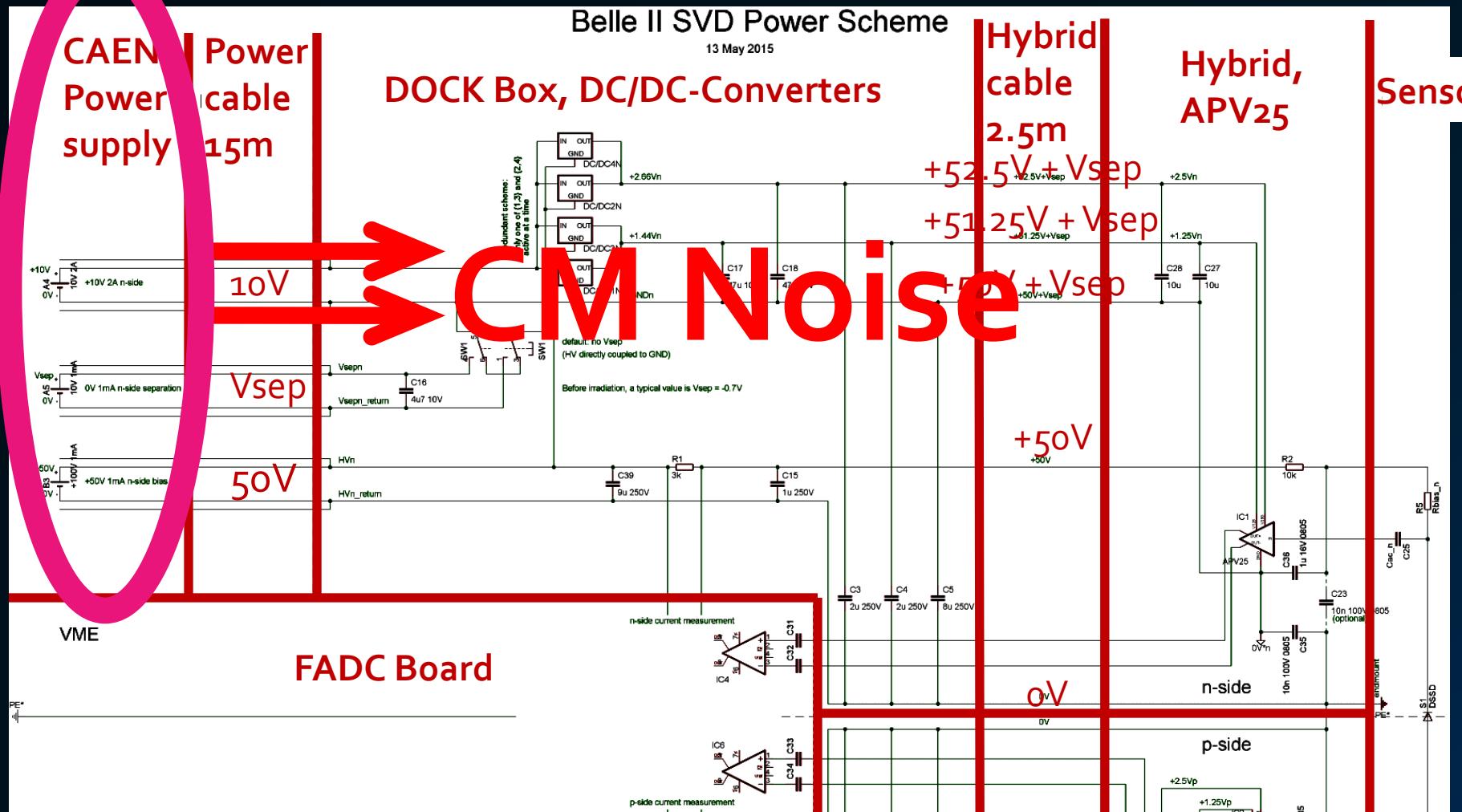
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SVD EMC Tests – CAEN Supply



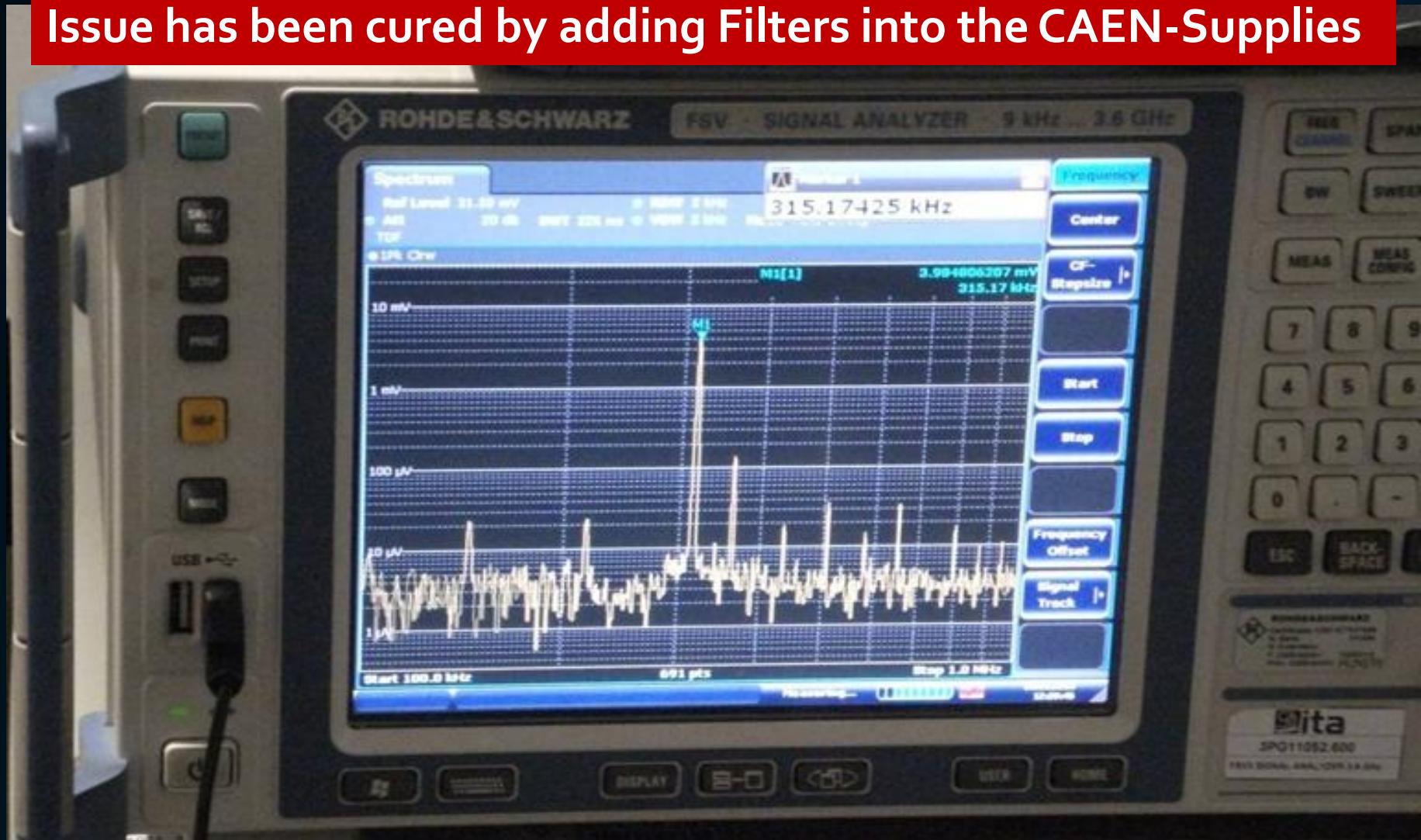
SVD EMC Tests – CAEN Supply



FADC System starts to struggle at 0.5mA.

CAEN-Supply: Common Mode Noise @10V: 315kHz, >4mA!

Issue has been cured by adding Filters into the CAEN-Supplies

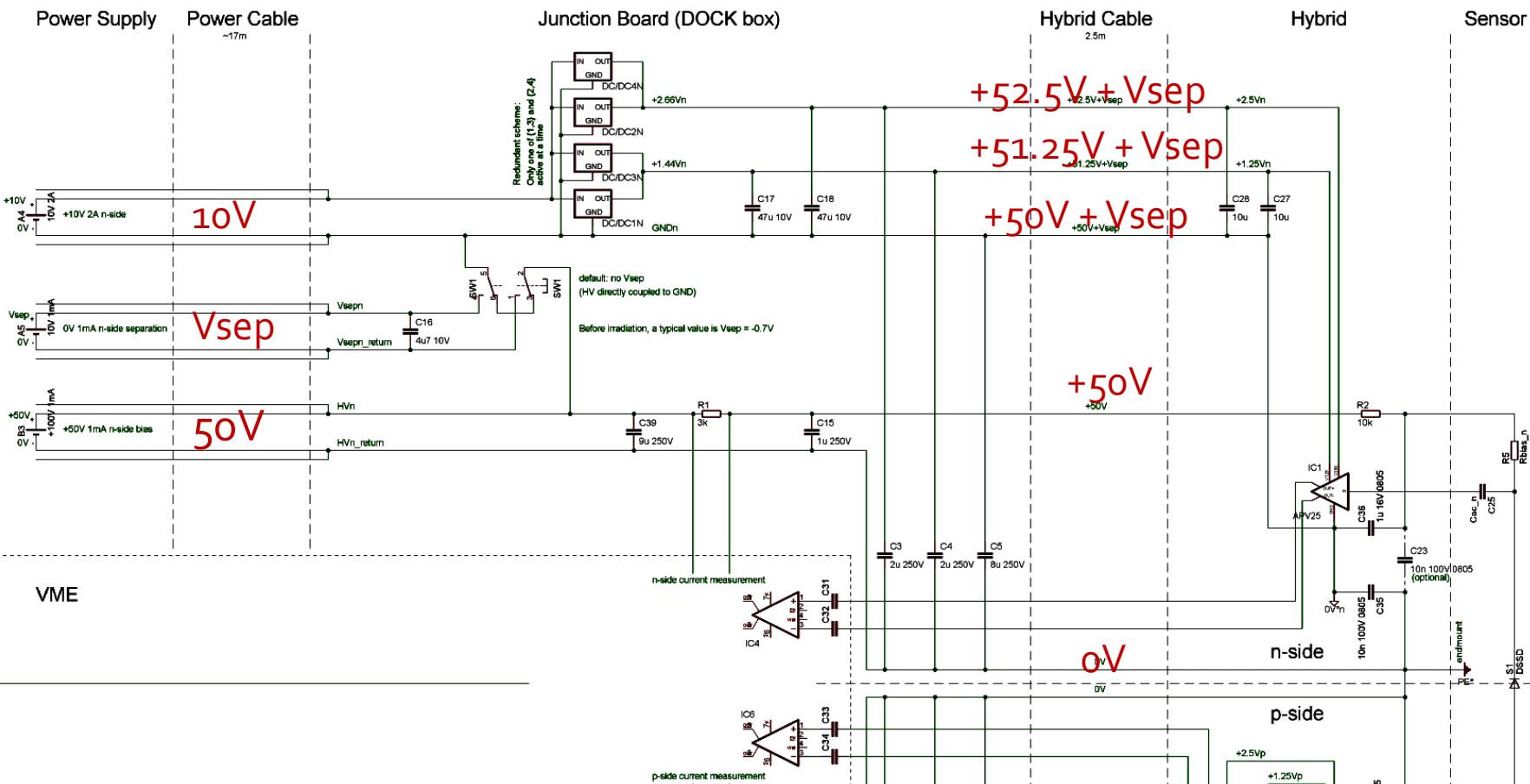


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SVD EMC Tests – Bias Capacitor

Belle II SVD Power Scheme

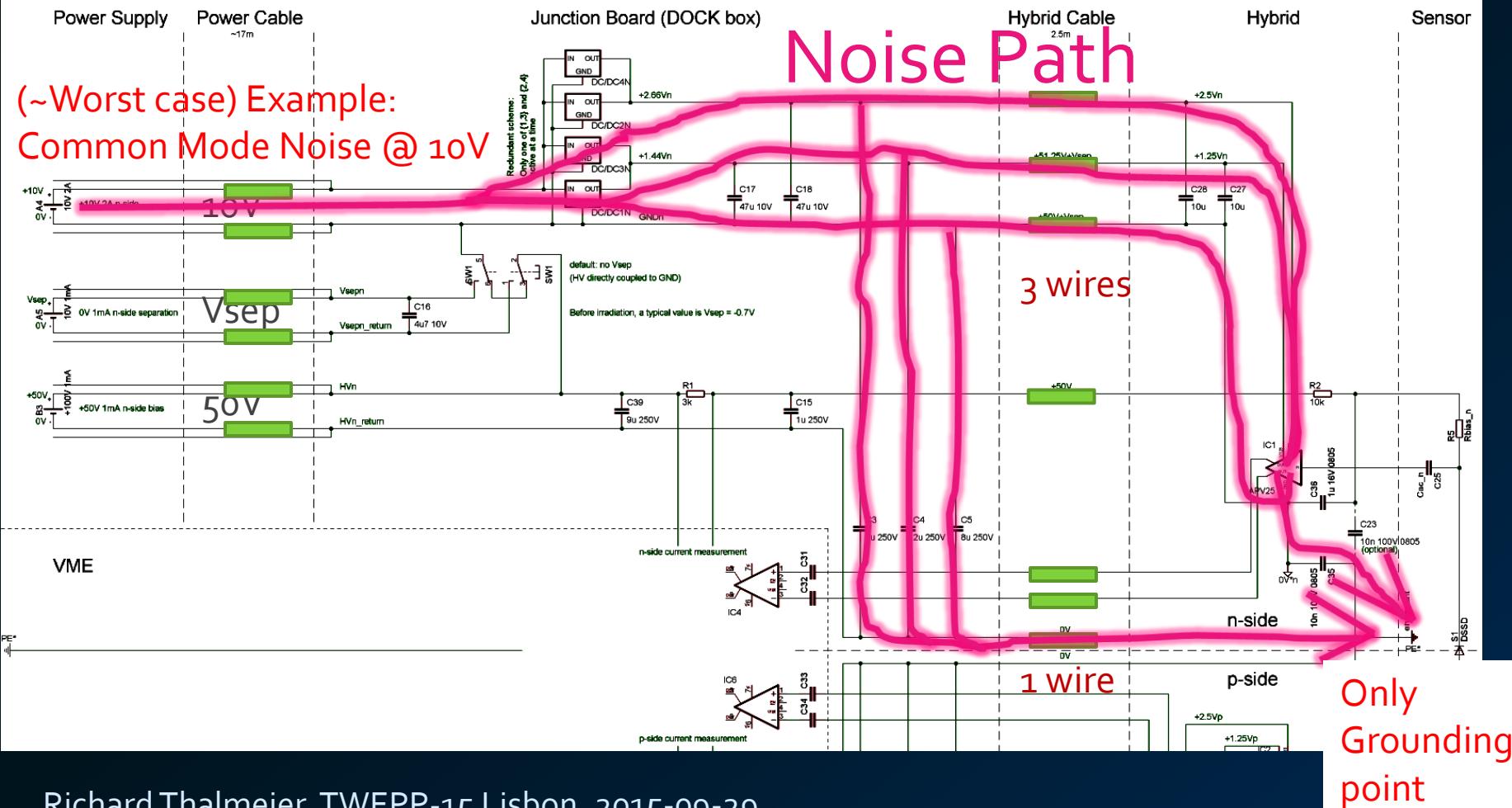
13 May 2015



SVD EMC Tests – Bias Capacitor

Belle II SVD Power Scheme

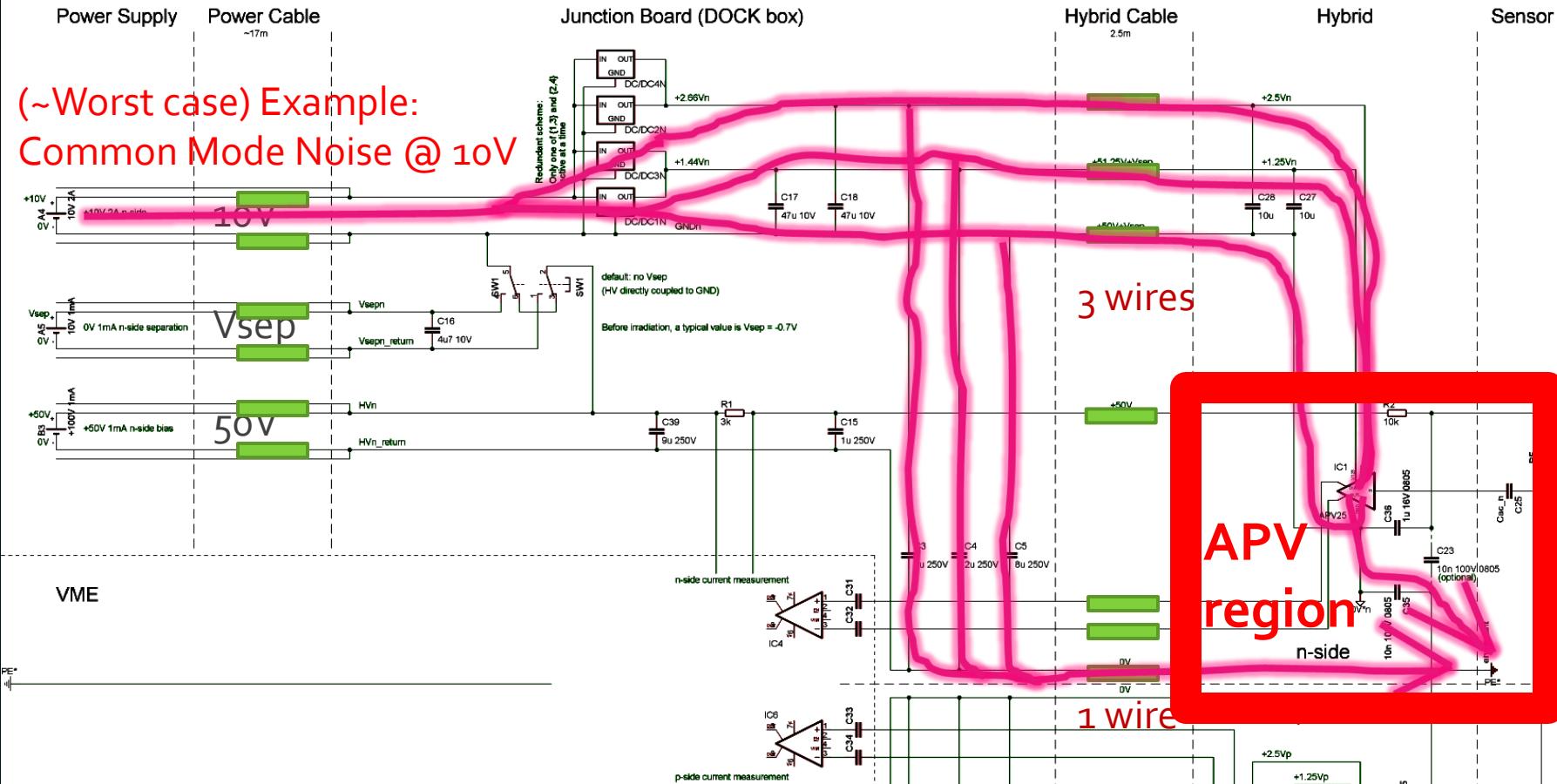
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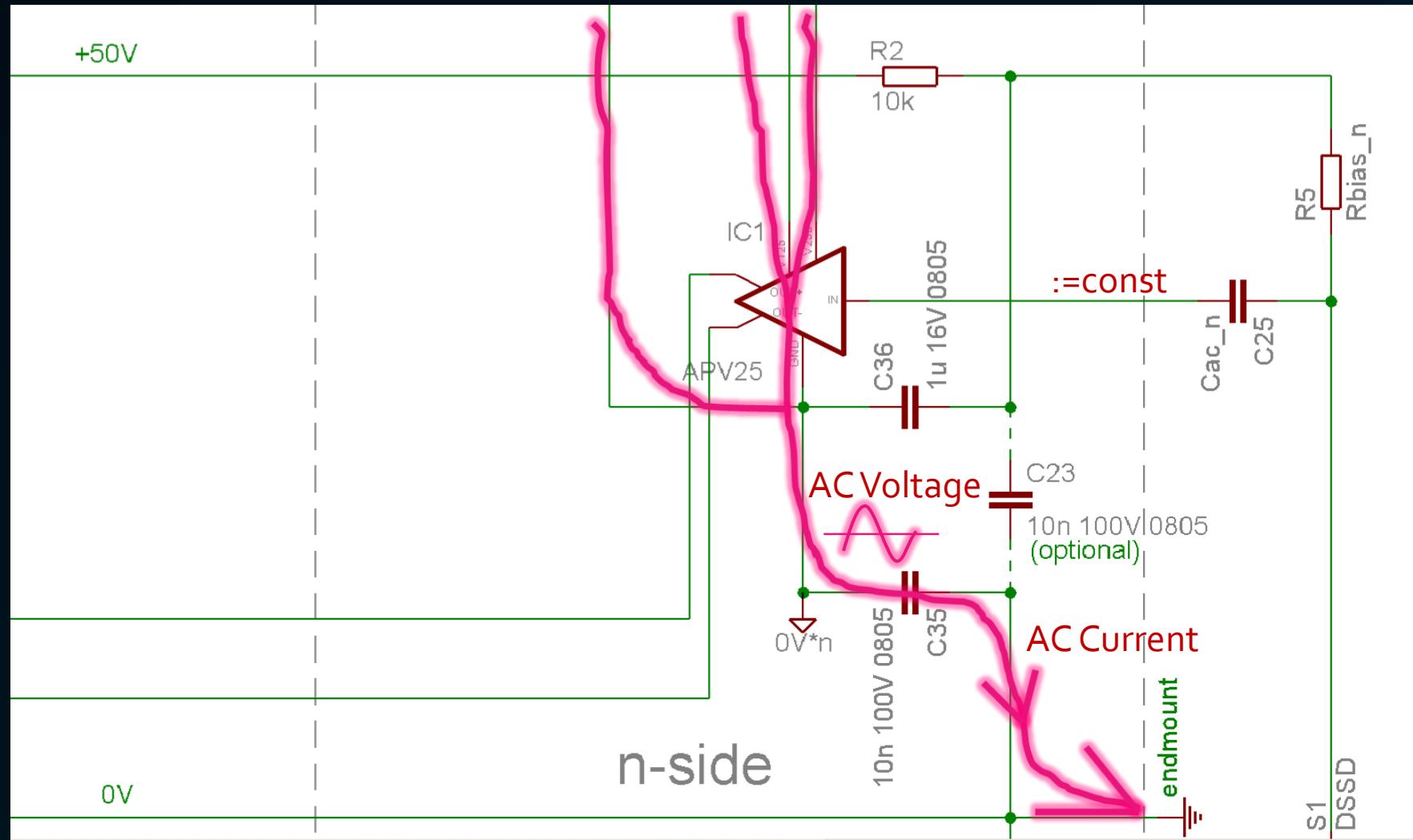
SVD EMC Tests – Bias Capacitor

Belle II SVD Power Scheme

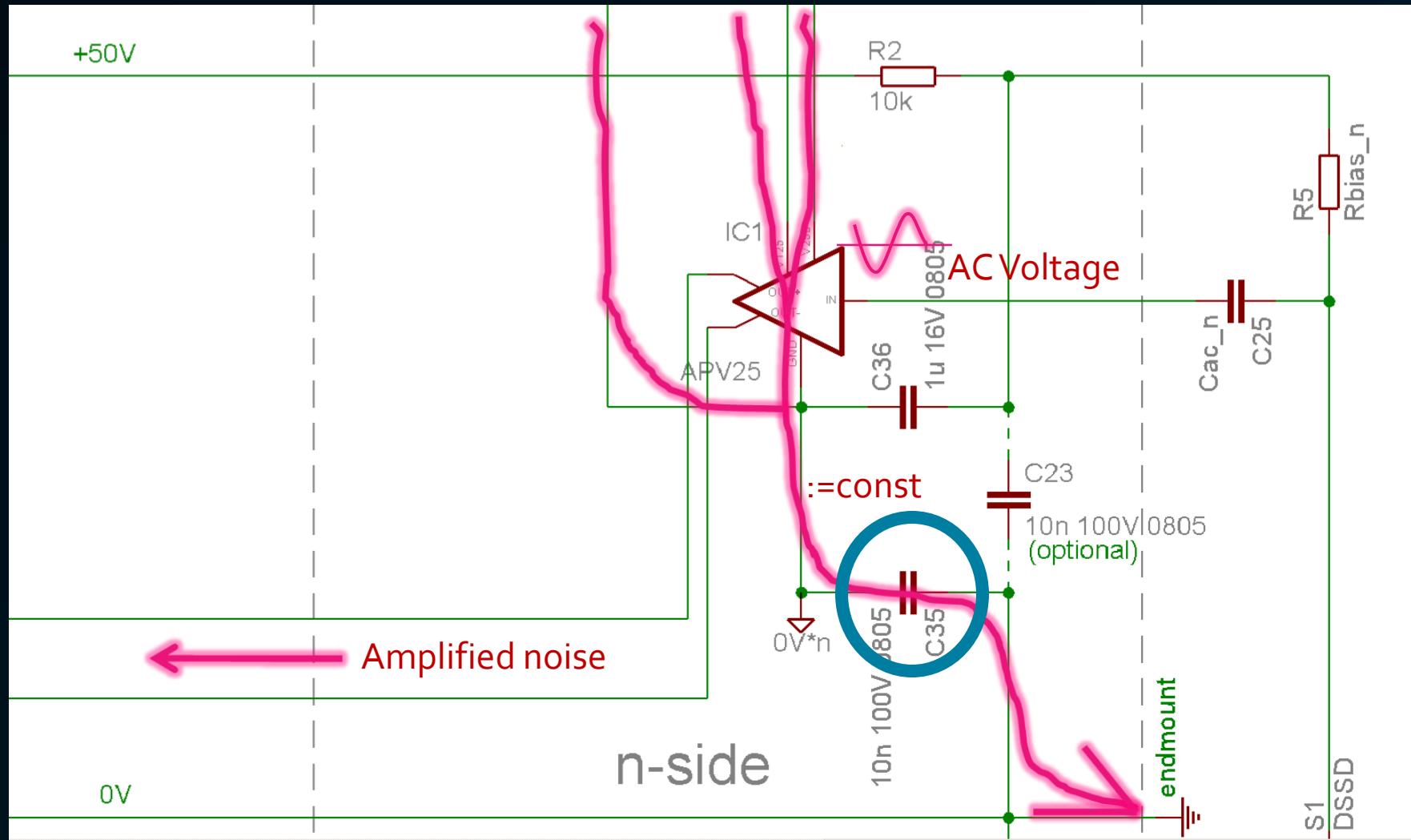
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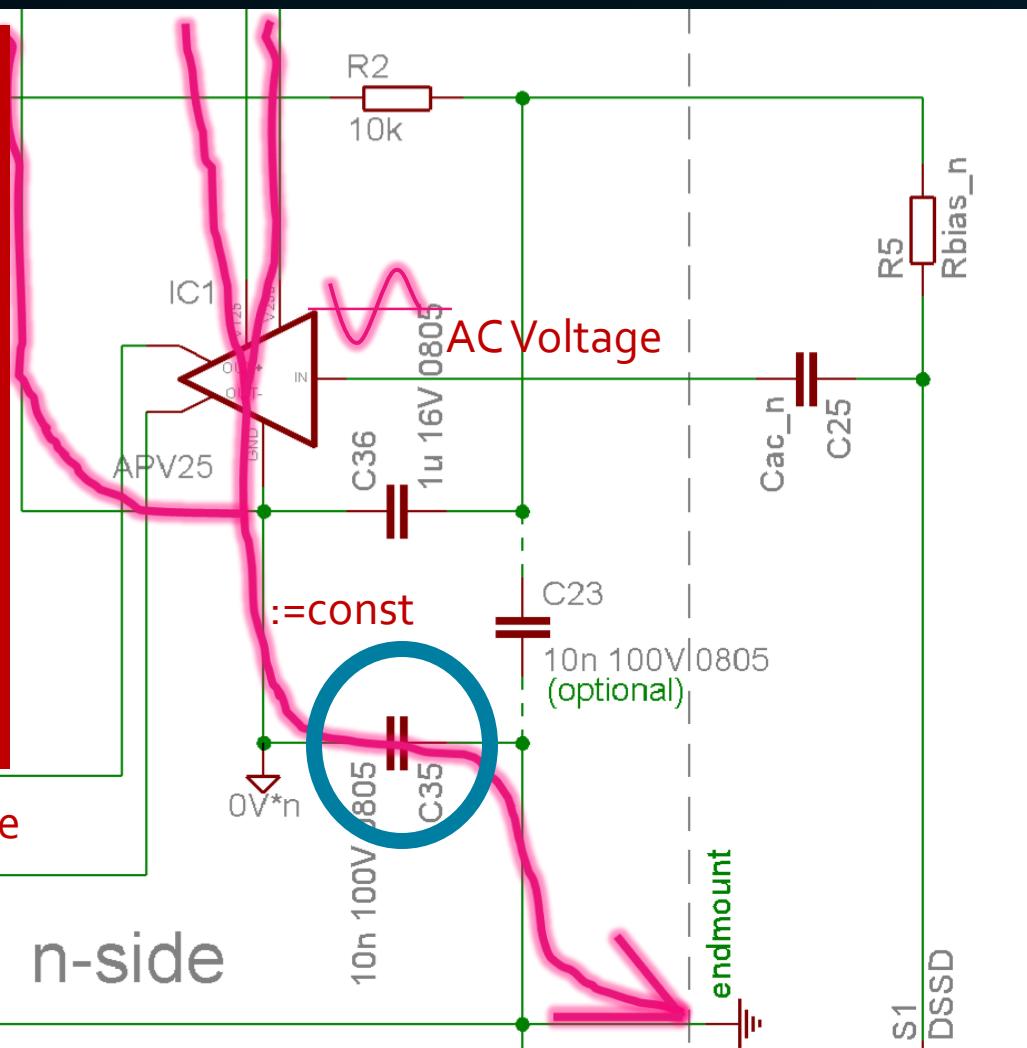
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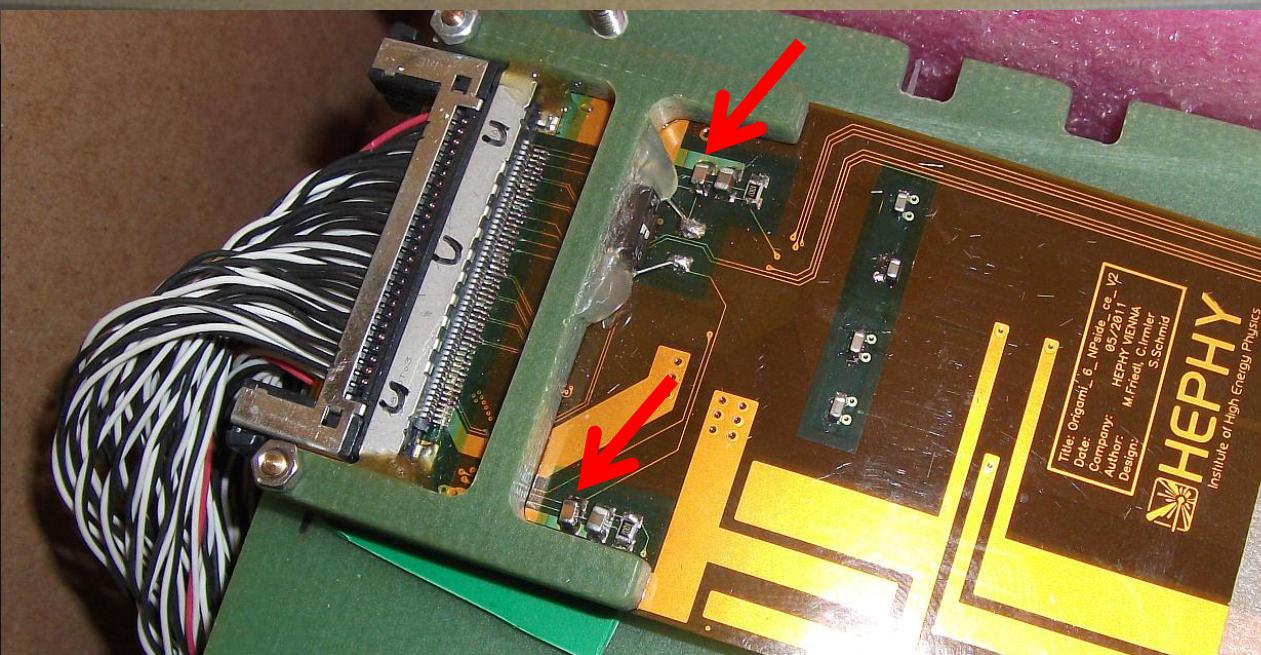


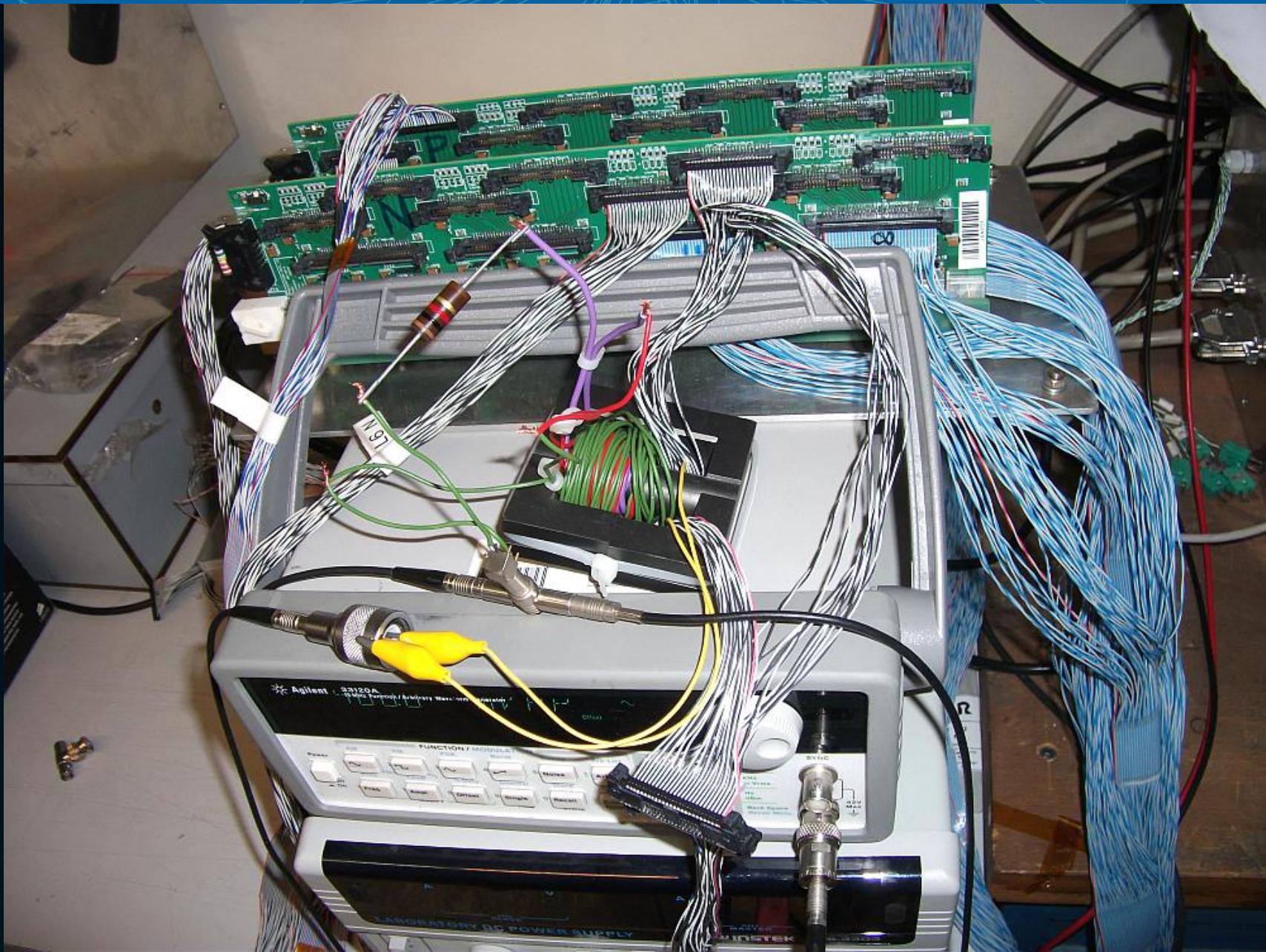
SVD EMC Tests – Bias Capacitor

Any AC Voltage on C₃₅ acts as Noise Input for the APV25. And gets amplified. Consequently, C₃₅ will be changed from 10nf → 100nF.

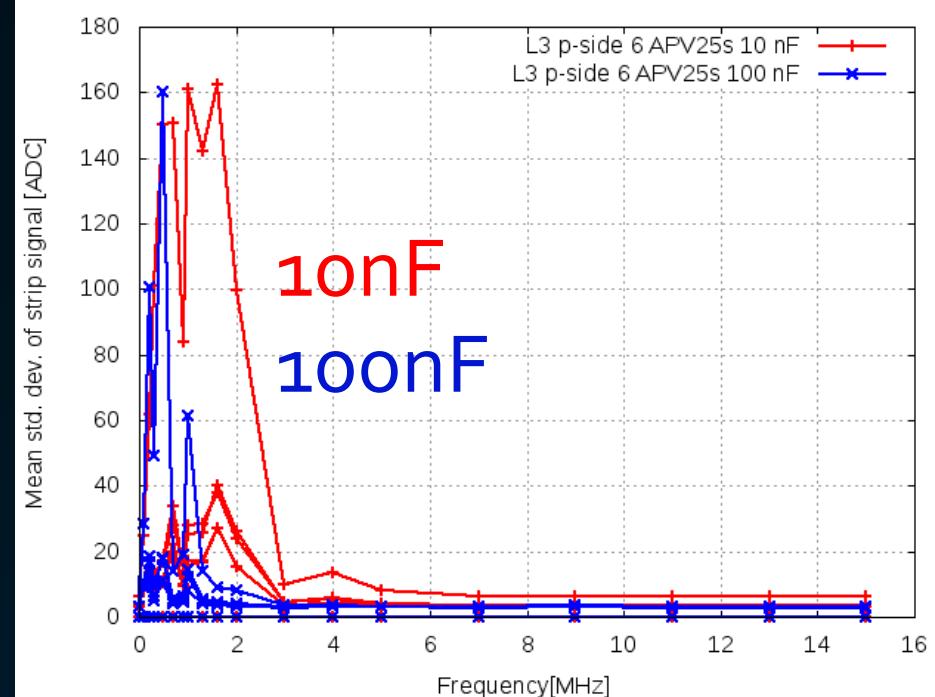
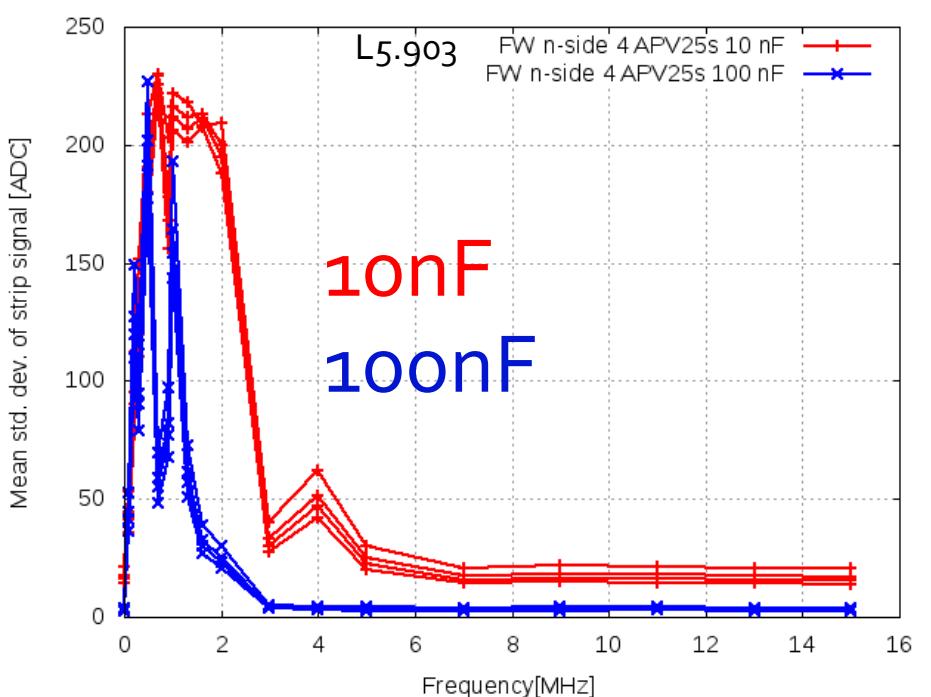
Amplified noise







SVD EMC Tests - Bias Capacitor



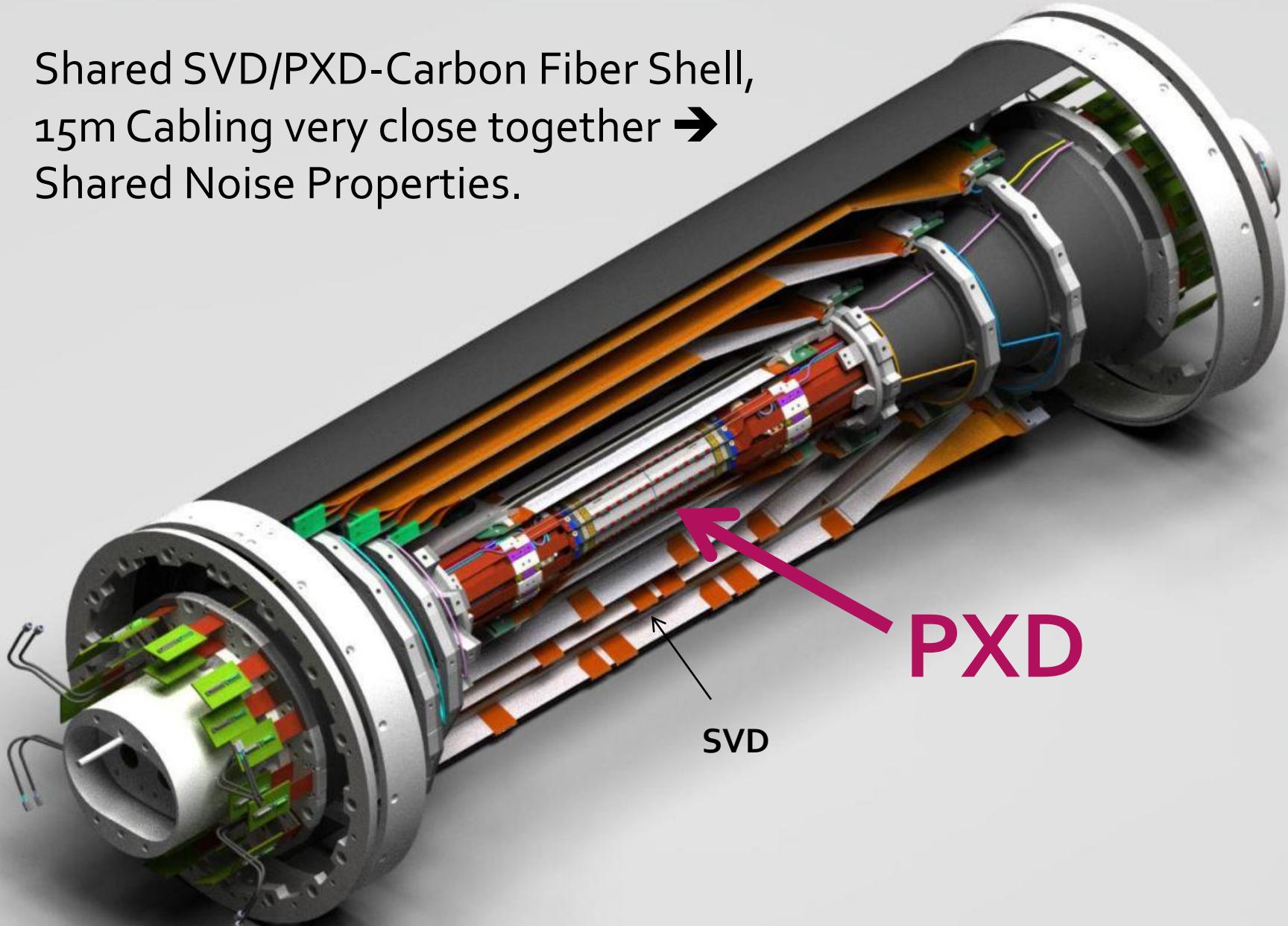
Chip average Strip RMS noise (without CMC) vs. noise frequency; Noise Injected in n-side

Big improvement particularly above 1MHz. Up to factor 10

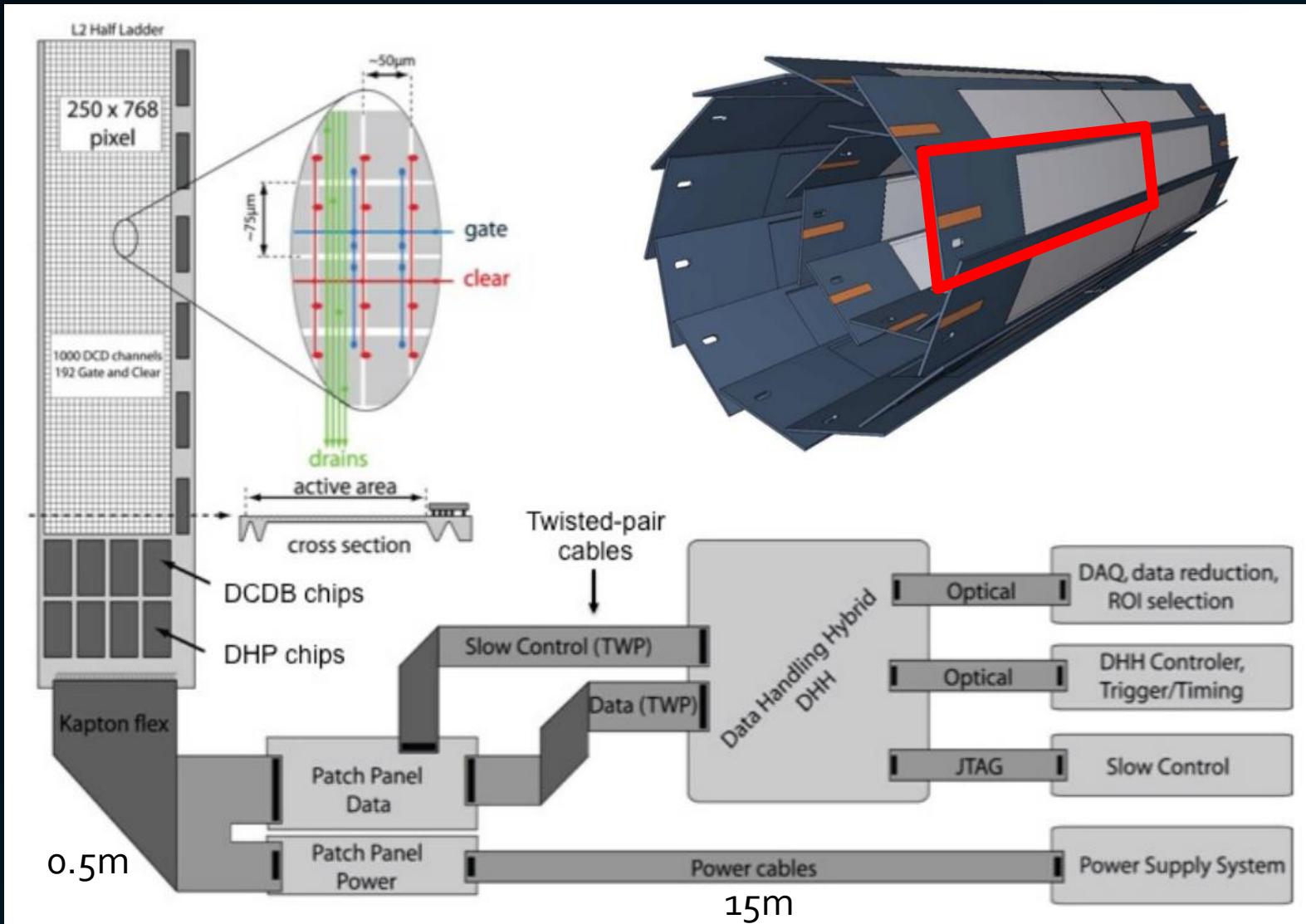
- **Belle II - Introduction**
- **SVD EMC Tests**
- **PXD Power Cable Studies**
- **Conclusions and Outlook**



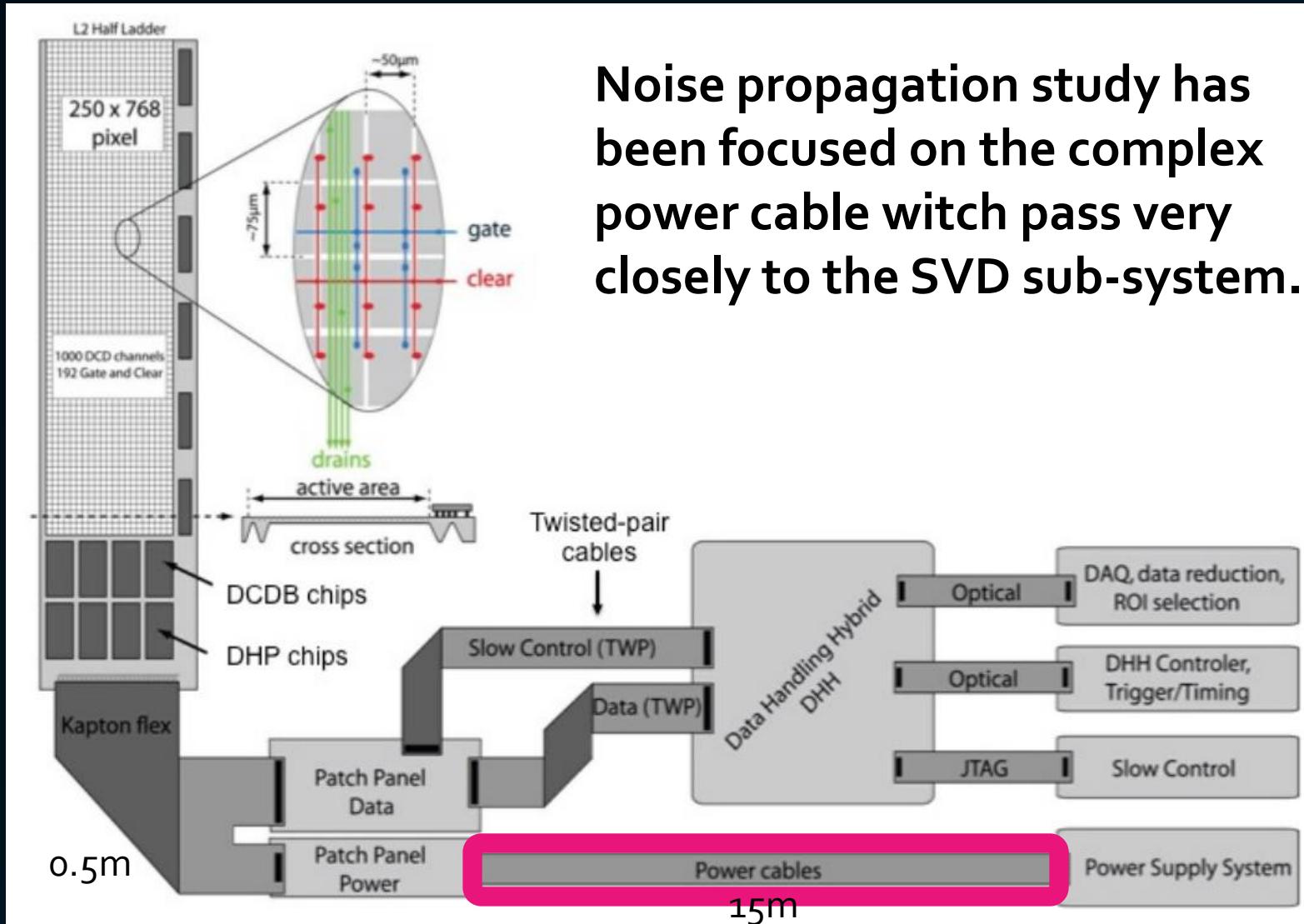
Shared SVD/PXD-Carbon Fiber Shell,
15m Cabling very close together →
Shared Noise Properties.



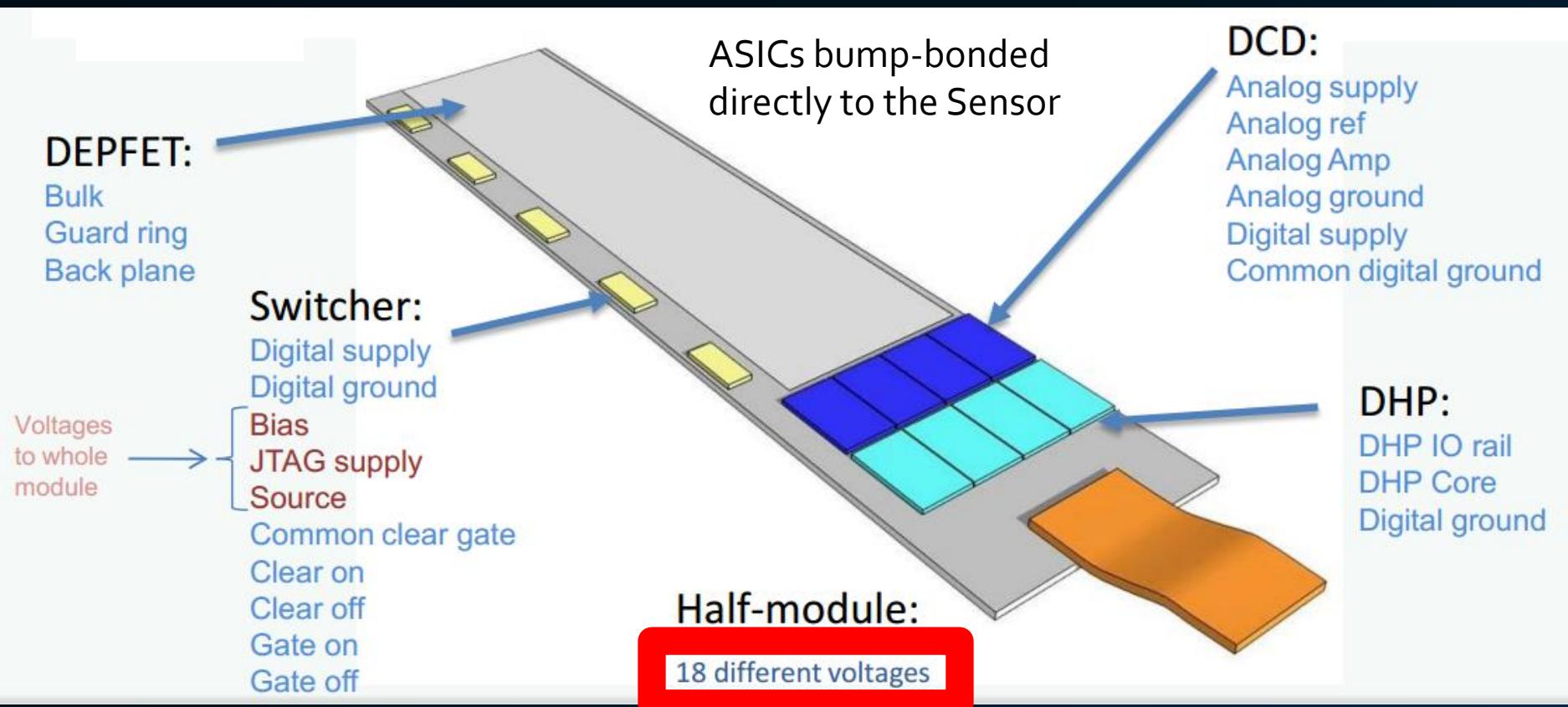
PXD Frontend and Power Supply



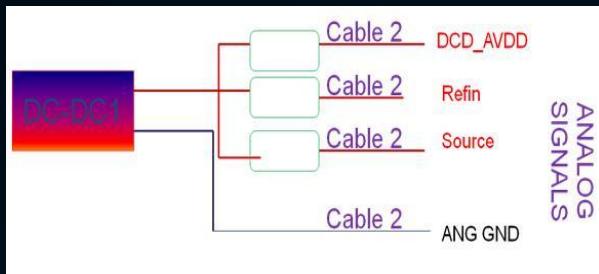
PXD Frontend and Power Supply



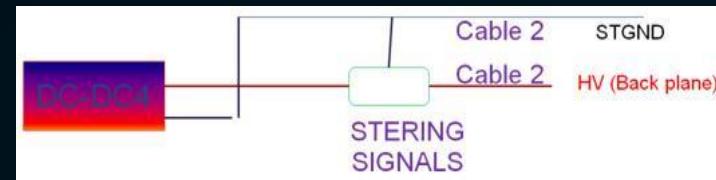
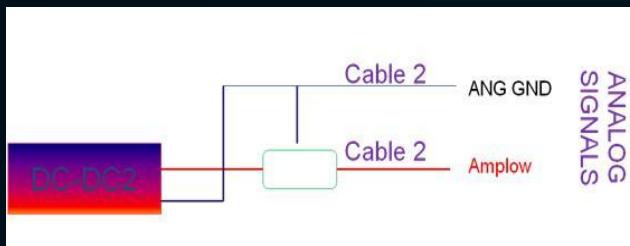
PXD Voltage Requirements



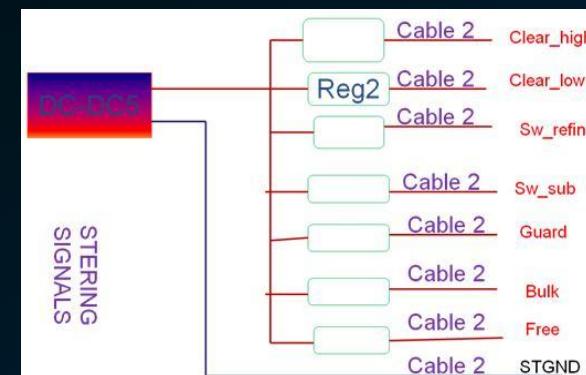
PXD Power Supply: 6x DC-DC, 2 cables



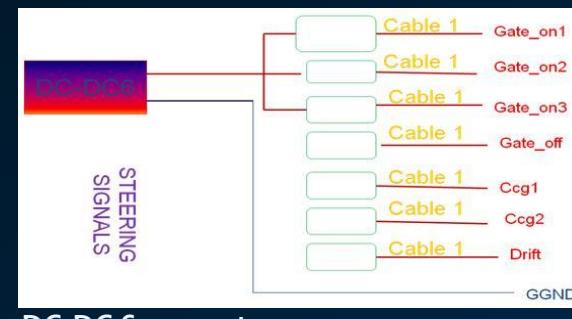
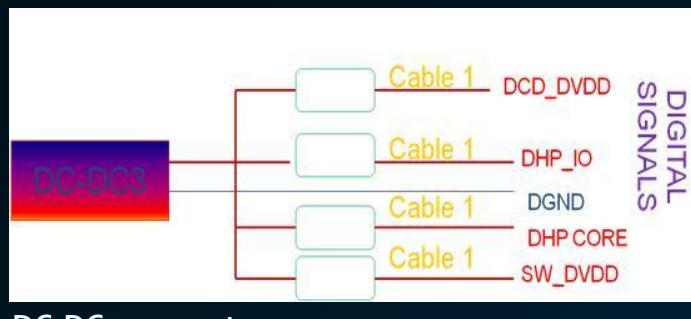
Common power return



Common power return



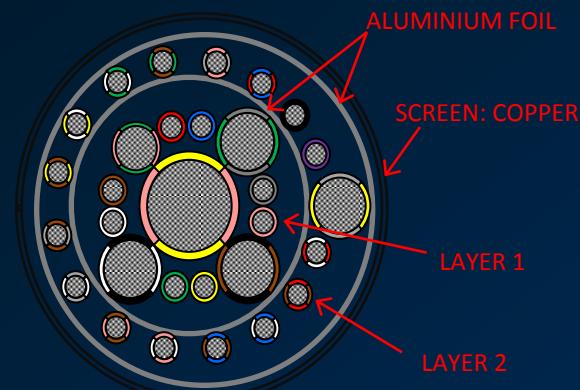
Power
Cable 2



Power
Cable 1

PXD Power Cable

- The power cable is a very complex cable (30 conductors)
- Hybrid cable used for digital and analogue signals:
Power, Bias & Sense.
- Construction:
 - Layer 1: 1x14AWG + 1x20AWG +
3X18AWG + 4X2X26AWG
 - Wrapping Aluminium foil to layer 1
 - Layer 2: 1x18AWG + 8X2X26AWG
 - Wrapping Aluminium foil to layer 2
 - Screen: tinned copper foil

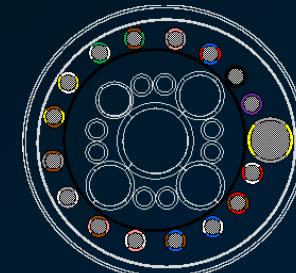


PXD Power Cable Noise Propagation

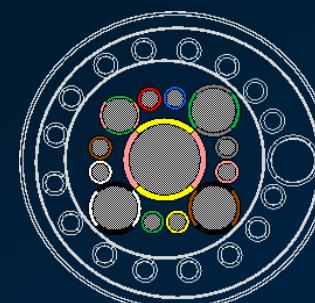
- Cable performance has been evaluated using Multi-conductor Transmission Line Theory (MTL).
- The MTL model divided the cable into 3 systems
- Assumptions:
 - Propagation is in Transverse electromagnetic mode (TEM)
 - R,L,C,G line parameter matrices per length unit
 - Voltages & Currents are vectors
- A MATLAB program has been developed in order to solve numerical MTL equations.
 - Parameters have been validated with real measurements



External system



Steering system



Analog/
Digital system

PXD Cable Measurement & matrix calculation

L, C and R matrix measurements

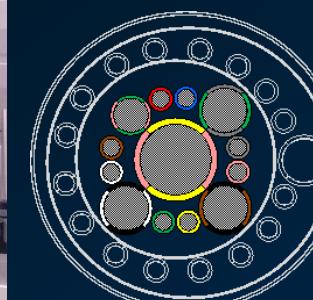
- External system: 1×1 Matrix for each L,C,R
- Steering system: 18×18 Matrix for each L,C,R
- Analogue/Digital system: 13×13 Matrix for each L,C,R



External
system

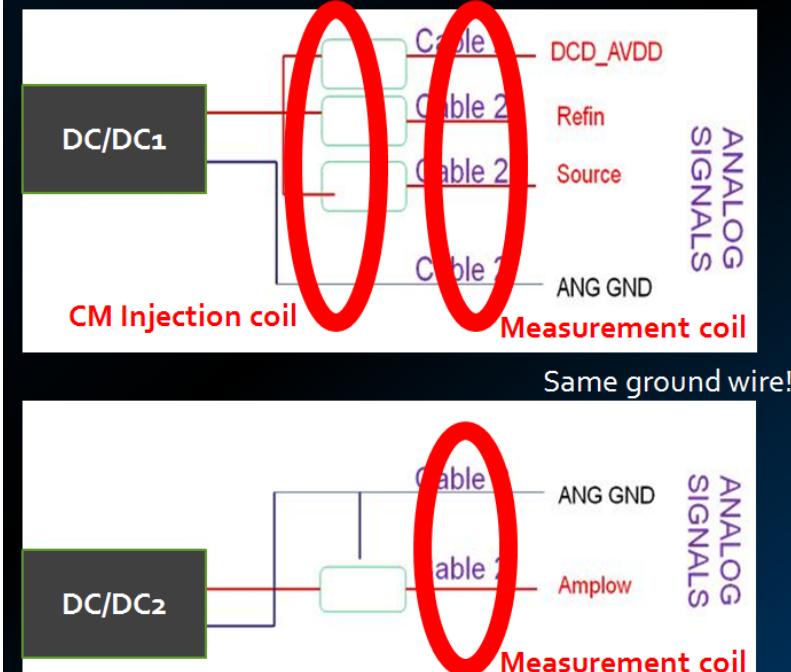
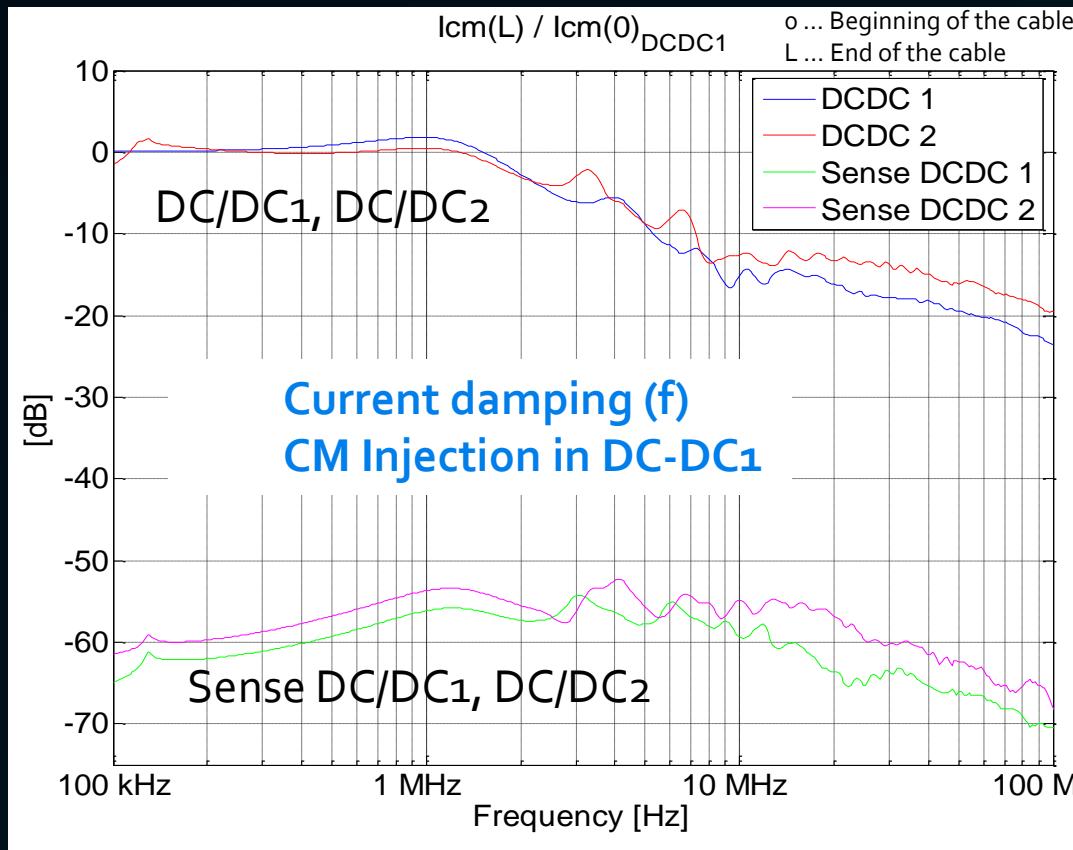


Steering
system



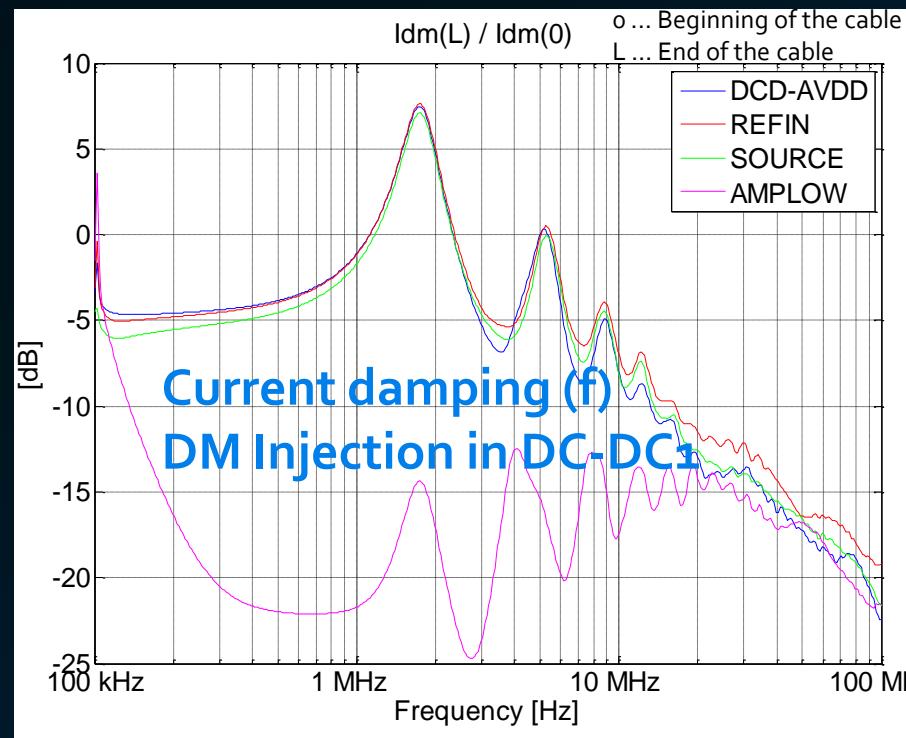
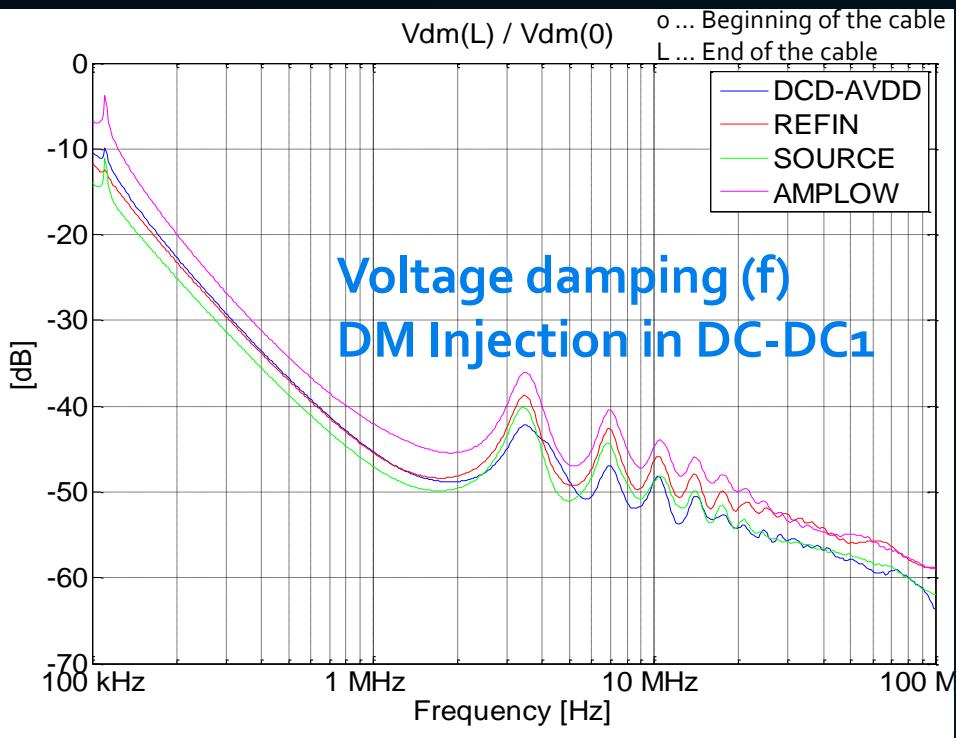
Analog/
Digital
system

Common Mode (CM) Noise from the PS

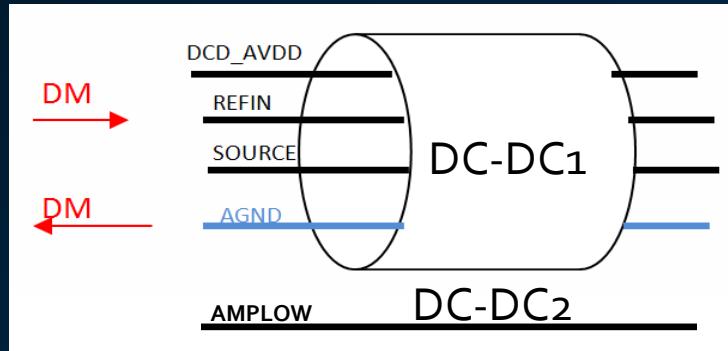


- Sense lines have low noise coupling due to the high impedance
- DCDC₁ to DC-DC₂ / DC-DC₂ to DC-DC₁ have similar noise coupling because of the common power return

Diff. Mode (DM) Noise from the PS (ripple)



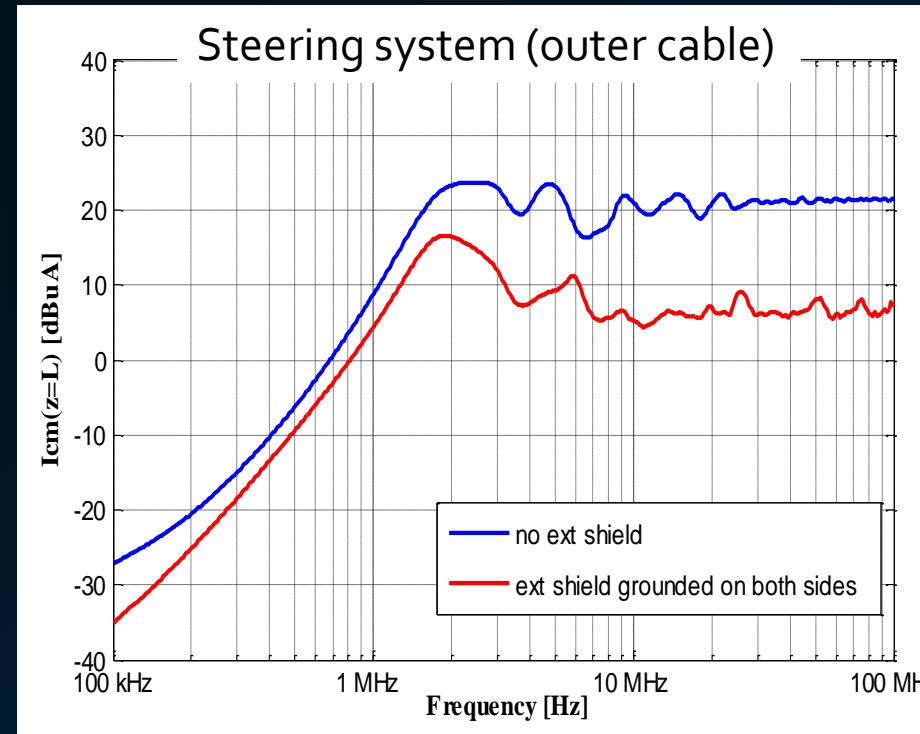
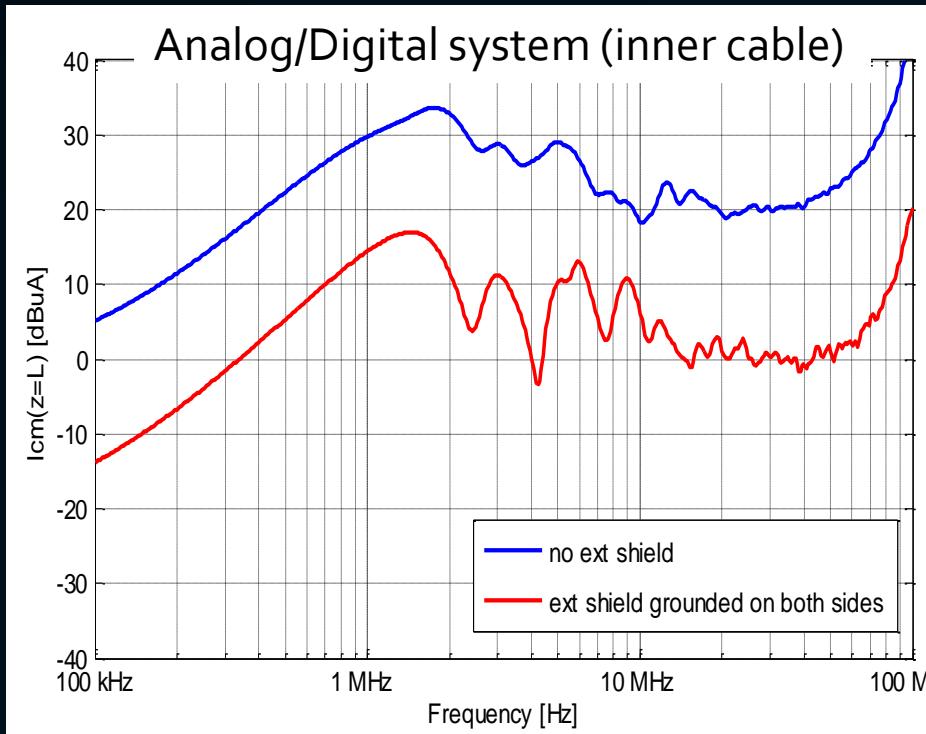
- Voltage is well attenuated due to DM capacitors
 - Similar voltage in complementary lines because of the Common return
- Current can even be amplified on some frequencies, but almost no radiation is expected due to return path compensation (twisted pair)
 - Similar DM noise distribution in common lines
 - low DM currents are expected in other systems in LF



Shield Currents and Shield Connections

Simulated antenna injection (1V/m) into the cable.

How should the shields be connected? On no end? On one end? On both?



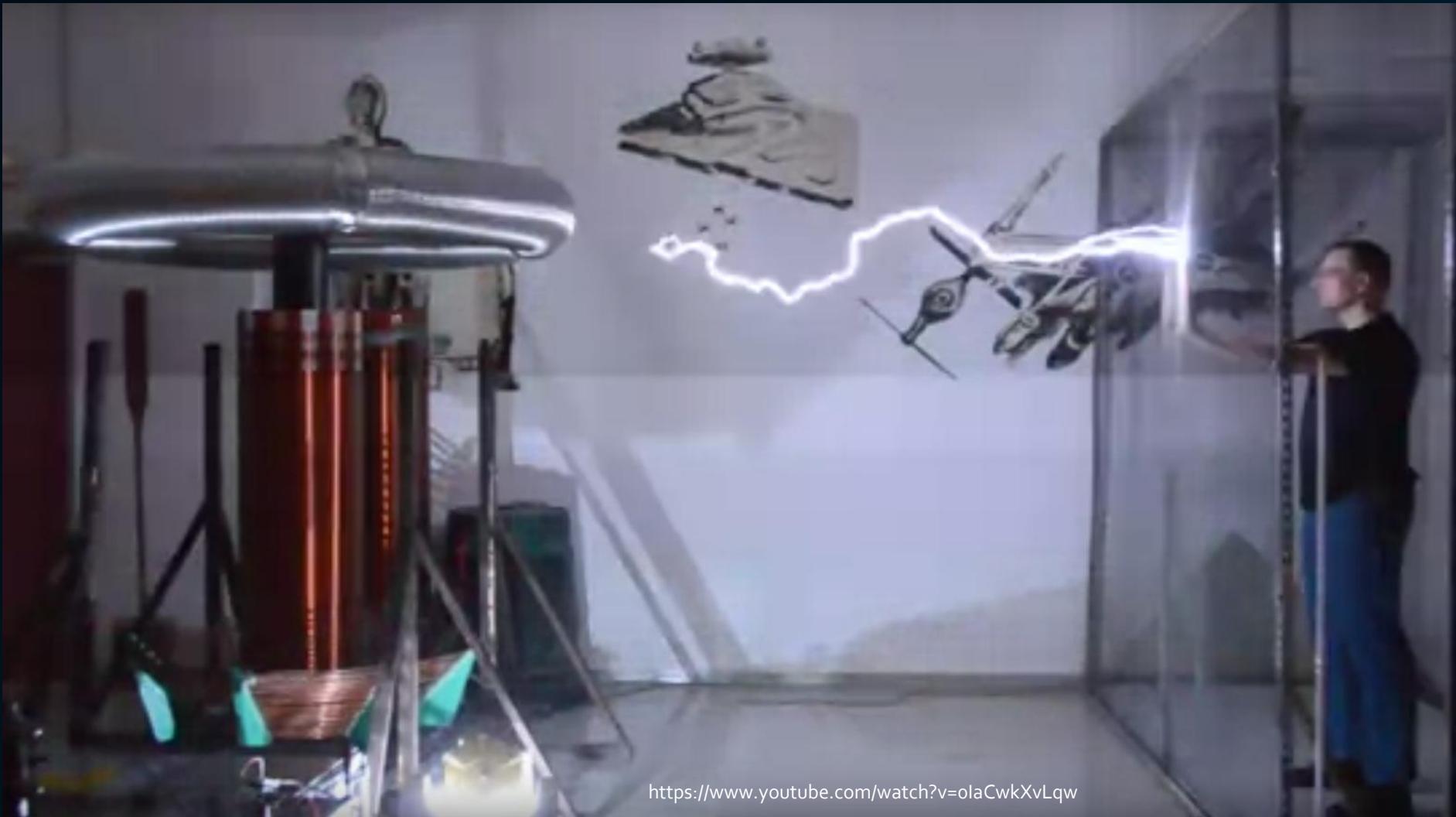
Outer shield connected to both ends improves the immunity to external fields.

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Conclusions and Outlook

- SVD emits very low noise
- SVD is very sensitive to external noise
- SVD EMC tests greatly helped to improve the noise immunity and to improve the power supplies
- PXD power cable has been systematically characterized
 - useful for further tests of SVD together with PXD
- PXD System will be measured - like it already happened with the SVD - at ITA Zaragoza in January 2016
 - very important to know which frequencies the SVD will get
- Combined PXD/SVD beam test at DESY Hamburg in April 2016

The End... Thanks for your attention ☺



<https://www.youtube.com/watch?v=olaCwkXvLqw>