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EMC Studies for the Vertex Detector of the Belle II Experiment

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The upgrade of Belle II experiment plans to use a vertex detector based on two different technologies. DEPFET pixel (PXD) technology and doubleside silicon microstrip (SVD) technology. The vertex electronics are characterized by the topology of SVD bias that forces to design a complex grounding and the complex topology of the PXD power cable bundle that may introduce some noise inside vertex area. This paper presents a general overview of the EMC issues present in the vertex system, based on EMC test on SVD prototype and a study of noise propagation in the PXD cable bundle based on MTL theory.

Summary

A new vertex detector based on two different technologies is planned to be installed in Belle II experiment at the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan. The proposed vertex detector consists of several modules and Front End electronics (FEE) arranged cylindrically in 6 layers around the interaction point. The first two layers are based on DEPFET pixel technology whereas the last 4 layers are based on double side micro strip technology.

SVD sub-detector consists of 172 doublesided silicon sensors. A total of 1748 readout chips (APV25) process and send the analog signals over 15 meter long copper cable to A/D Converters (FADC) located on top of the Belle II detector structure. From the FADCs the data are then sent out by optical fibers to the central DAQ. The SVD system is powered by several power supply units located on the top of Belle II. These units supply the HV(50V) required to bias the sensors and the LV(10V) to power the FEE. The HV line feeds directly the sensors whereas the LV is distributed to a Dock box located 3 meters away from the SVD FEE. At that location DCDC converters transform the 10V into the 2.5V and 1.25V required to operate the APV25.

On the other hand, the read-out and control ASICs of the PXD sub-detector will be bump bonded on the rigid edges of the DEPFET substrate whereas in the region of the active pixel matrix the substrate will be thinned down to 50 μ m. The front-end electronics (FEE) is subdivided into three different ASIC types which require around fifteen different voltages to operate. This power is provided by a set of power units located 20 meters away from the detector using a very complex cable with more than 30 wires (shielded and unshielded) bundled all together, which pass very close to the SVD sub-system.

This paper presents a general overview of the EMC studies that have been carried out in the vertex detector in order to define the electronics integration key parameters that minimize the noise level present inside vertex volume. Two complementary studies are presented. One focused on the noise issues present in the PXD cable based on MTL models, and another focused on the evaluation of the SVD grounding topology based on EMC tests.

The PXD simulation studies will help to define the noise level present in the vertex area due to noise coupling among the PXD cable bundle as well as the noise propagation through it. The second study shows the susceptibility test performed in the SVD in order to characterize the immunity of SVD system to the noise presented in the vertex volume. This set of tests has been performed in the EMC laboratory at ITAINNOVA. This is the first time that a HEP detector has been tested inside a semianechoic chamber.

The outcome of this study will provide information to address the effect of noise running through PXD cables on noise immunity levels required for SVD FEE.

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