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High speed readout solution for single-pixel-photon counting ASICs

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We present a flexible, high speed readout system for the high-frame-rate photon-counting ASICs. The solution was implemented in an ASIC with 128 x 256 pixel matrix with dual 14-bit counter pixels, in 130 nm CMOS technology. In the presentation the details of the architecture and the test results will be shown. Currently the ASIC runs stable with 200 MHz input clock, while the tests with 500 MHz clock frequency and DDR mode are ongoing.

Summary

The bottleneck in high-frame-rate photon-counting ASICs is the readout system, which has to stream out of the chip substantial data volumes. For example, for the 128 x 256 pixel matrix with 14-bit counters a single frame size is 448 kbits, so to get the constant frame rate of 10 000 frames/s one needs a data link of 4.48 Gbps (not counting the protocol overhead). The concurrent requirement is keeping the power consumption low and limitation of the crosstalk to the analog part of each pixel.

We present a flexible solution for a readout system complementing the requirements given above. The solution was implemented in an ASIC with 128 x 256 pixel matrix with dual 14-bit counter pixels, in 130 nm CMOS technology. In the presentation the details of the architecture and the test results will be shown. Currently the ASIC runs stable with 200 MHz input clock, while the tests with 500 MHz clock frequency and DDR mode are ongoing.

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